

DC Linearity and Absorption Efficiency Enhancement by Introducing Photon-Trapping Microstructures into Avalanche Photodetectors

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ABSTRACT

The direct-current (DC) linearity of a photodiode is a parameter that indicates the direct proportionality between the input optical power and the output response current. This linear relationship defines the optical power range using which the performance limits of the photodiode control circuitry such as A/D conversion, trans-impedance amplifier, and quenching circuits are designed. Due to the absorption saturation and self-heating, the response current of the photodiode starts to saturate at higher optical power. A narrow absorber region in state-of-the-art photodiodes (avalanche and PIN photodiodes) results in an early absorption saturation in addition to a reduction in absorption efficiency. We present a photon-trapping microstructure (PTMS) equipped-avalanche photodiodes (APD) to enhance the absorption efficiency and DC linearity. We have fabricated a mesa-based APD using complementary metal oxide semiconductor (CMOS)-compatible processes. We present a DC current-voltage comparison of APDs in the dark and under the illumination of a wide wavelength range varying from 640 nm to 1100 nm. The fabricated PTMS-equipped APDs exhibit $5\times$ increase in the external quantum efficiency as opposed to that of a flat device and a 70 unit multiplication gain. Further, the PTMS-equipped APDs demonstrate an increased linearity of 106.04 dB in comparison to 104.83 dB linearity in the flat device. The introduction of PTMS, despite the reduction of net-absorber volume, enables a uniform spread of the input illumination power by bending the light laterally and results in increased absorption efficiency and DC linearity.

Keywords: Avalanche photodetectors; CMOS compatible detector; DC linearity; Ultrafast detectors

1. INTRODUCTION

Photodetectors are employed in a variety of disciplines including medicine, astronomy, and communications.^{1–3} The rapidly evolving optoelectronic applications demand constant enhancement in the speed and absorption efficiency at a reduced operating power of the photodiode at low manufacturing cost. Along with the high speed, the photodiodes are desired to exhibit a linear increase in the illumination current with increased optical power, a.k.a, the direct current (DC) linearity. Impact-ionization-governed avalanche photodiodes (APD), attributing to their intrinsic multiplication gain, have demonstrated exceptionally high electromagnetic (EM) wave absorption efficiency (EQE: external quantum efficiency) and speed.^{4–8} Reducing the absorber layer thickness has further been shown to enhance the response time of the device.^{9,10} However, with the reduced absorber layer thickness, the volume available for the EM wave absorption reduces, and as a result, the overall EQE reduces.

Photodiodes with high photo-current can be especially advantageous as this can reduce the need for additional amplifiers that can increase the cost and complexity of their implementation in larger systems.¹¹ However, a non-linear behavior of the photodiode with increased illumination power defines the upper limit on the photo-current. The linearity of a photodiode is influenced by: absorption saturation, space-charge screening, and self-heating of the device.¹² Space-charge screening occurs when excess generated carrier density collapses part of the electric field in this region. Carriers within a collapsed electric field will no longer be controlled by drift but will be governed by diffusion. This increases the risk of carriers recombining without being collected

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thereby contributing to the photo-current. Consequently, even though the ratio of carrier generation to optical power may remain linear, the observed relationship between photo-current to optical power manifests as non-linear.¹³ The absorption efficiency is another important design consideration for photodiodes. When it comes to enhancing the light-absorbing efficiency of photodetectors, the use of photonic crystals has greatly expanded the possibilities. E. Yablonovich, in his landmark 1987 paper, showed that by adding texturing to the surface of Si, the absorption could be enhanced by $4n^2$, where n represents the refractive index of the semiconductor.¹⁴ Following this, in 2010, S. Fan showed that by optimizing surface textures, the absorption could be enhanced significantly, potentially by $12n^2$ in solar cells.¹⁵

In our previous work, we have taken these insights and applied them to photodiodes. Structures explored include 1D micropillars,¹⁶ 2D micro walls,¹⁷ and photon-trapping (PT) microstructures.^{10,18–22} Introducing the surface microstructures remedy the impact of reduced absorber layer thickness on the EQE of the APDs. The group demonstrated that by adding these structures, additional propagation modes in the lateral body of the photodiode could allow light to propagate through the lateral body of the device. This can be used to enhance absorption beyond that of planar Si. Despite extensive research on the impact of PT microstructures on the photodiode performance parameters such as EQE and speed, its effect on the performance linearity remains unexplored.

In this work, we have studied the impact of photon-trapping microstructures on the linearity of the device. We have fabricated a flat and a PT-equipped APD to compare the impact of PTs on the linearity. We have demonstrated that introducing PT holes results in EQE enhancement. We have extended our inquiry to study the impact of PT-holes on the DC linearity of the device. Increased linearity will ensure a higher current-carrying

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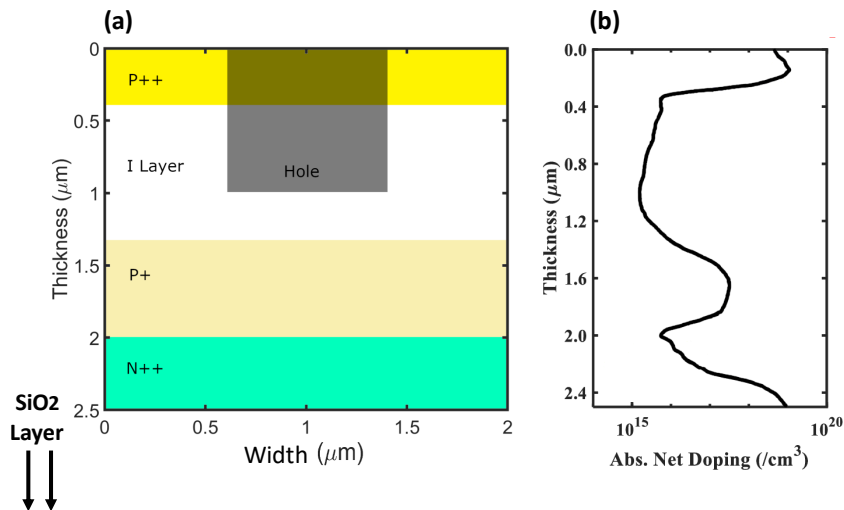


Figure 1. The doping of the wafer used for APD fabrication. (a) A simplified view of the wafer layers. The layer stack shown is on top of SiO₂. (b) SIMS data highlighting the doping profile of the APD wafer.

1.1 PT-holes introduction: Hindrance or assistance to the DC linearity?

We have studied in great detail the impact of introducing PT-holes into photodiodes on the responsivity and high-speed performance.^{7,9,10,18} However, it is still unsettled if a reduction in the absorber volume will decrease the DC linearity or if the lateral spread due to diffraction of the EM-waves will assist the DC linearity. To address this inquiry, we have characterized and compared the performance of flat and PT-equipped photodiodes under extreme illumination power (maximum power = 40 mW) and measured their linearity.

The sections going forward cover the details of the device design, fabrication, and extensive electrical characterization.

2. EXPERIMENTAL DETAILS

We have designed the doping profile of the wafer to enable a sub-10V breakdown in the finally fabricated avalanche photodiodes (APD). An illustration of the doping stack used in this work is presented in Fig. 1(a). The doping stack includes (listed from the top down) a p++ contact layer, an intrinsic π -layer, and a p+/n++ multiplication junction. These layers were epitaxially grown on a silicon-on-insulator (SOI) wafer. Figure 1(b) presents the secondary ion mass spectrometry (SIMS) depth profile of the doping stack. As evident from the SIMS profile, the π -layer is lightly doped with $2 \times 10^{15} \text{ cm}^{-3}$ unintentional doping. Both the p++ and n++ contact layers are highly doped with $2 \times 10^{19} \text{ cm}^{-3}$ doping concentration. Finally, the doping concentration of p+ region is $\sim 5 \times 10^{17} \text{ cm}^{-3}$.

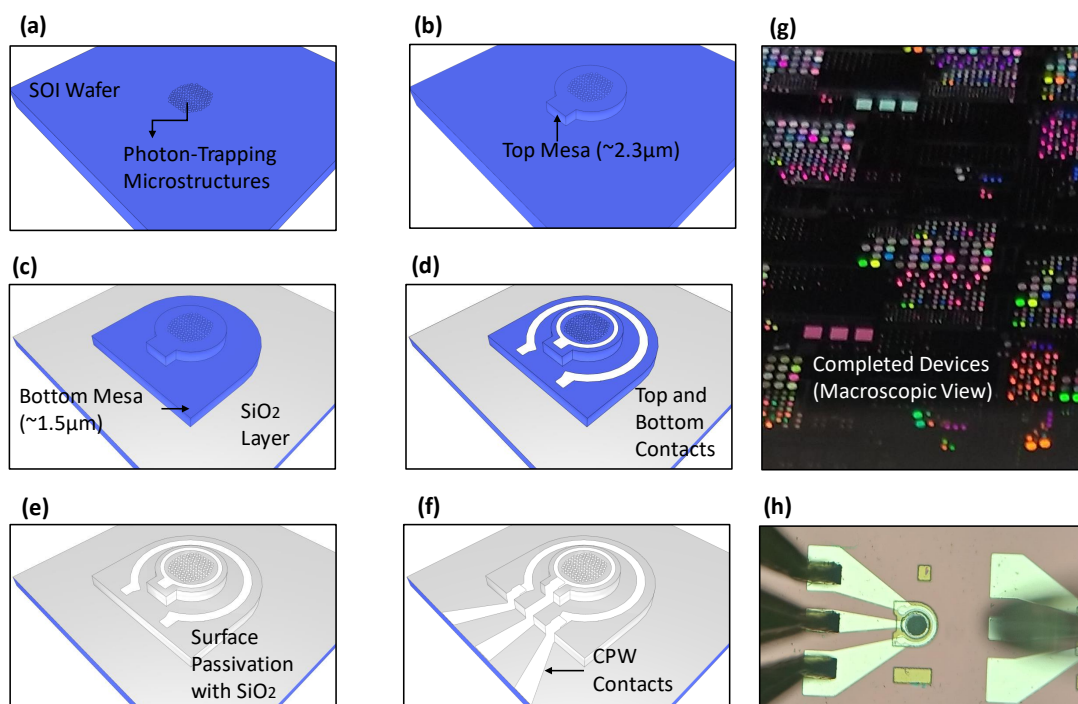


Figure 2. The steps of the fabrication process and the completed device. (a) The first process step of patterning the wafer surface with the photon-trapping microstructures. (b) Etching the top mesa. (c) The bottom mesa is etched around the top mesa, and down to the insulator layer of the SOI wafer. (d) Deposition of the top and bottom contacts. (e) The passivation step is done at this point to prevent shorting of the CPW contacts between the top and bottom mesas. It has the additional role of passivating the photon-trapping microstructures. (f) The deposition of the CPW contacts. (g) The macroscopic, true-color view of the completed dice. (h) A 20x magnified view of one device undergoing characterization testing.

The APD fabrication process steps are summarized in Fig. 2(a-f). The wafer is cleaned using a standard RCA silicon wafer cleaning process. The cleaned wafer is loaded in a plasma-enhanced chemical vapor deposition (PECVD) chamber for 200 nm thick SiO₂. After the SiO₂ deposition, the PT holes are patterned using the ASML Stepper lithography system. The patterned holes were transferred on the SiO₂ layer by etching the SiO₂ using an inductively coupled plasma reactive ion etching (ICP-RIE) system. Using the etch-SiO₂ as a hard mask, the PT holes are transferred on the silicon wafer by etching the silicon in an ICP-RIE chamber. Further, in alignment with the PT holes, a top mesa is patterned and etched using an ultra-violet lithography system and an ICP-RIE system, respectively. The top mesa is etched deep enough to expose the bottom n++ contact layer. Next,

in alignment with the top mesa, a bottom mesa is patterned and etched using the same process. Once, both the mesas are defined, an aluminum-based metallization is performed in an electron-beam evaporator system. We have performed a surface passivated process to reduce the impact of surface states and dangling bonds on the dark current performance of the APD. Finally, we have patterned and formed co-planar waveguide (CPW) contacts for high-speed operation. A further detail of the APD fabrication process can be found in our previous work.¹⁰

Figures 2(g-h) showcase micrographs of the fabricated devices. The colorful picture is captured by exposing

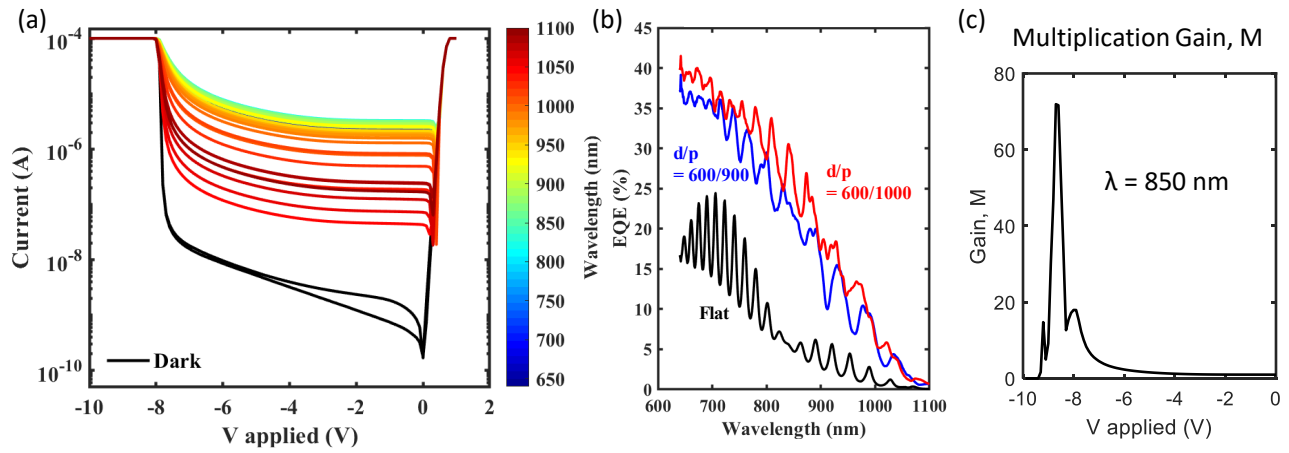


Figure 3. (a) The DC IV characteristics measured from the PTMS-equipped APD device in the dark and under illumination by varying the illumination wavelength from 640 nm to 1100 nm. A sub-10V breakdown voltage is showing an alignment with the design.¹⁰ (b) The external quantum efficiency (EQE) trend comparison between the flat versus PTMS-equipped APDs highlights the EQE enhancement with the introduction of PTMS. (c) The multiplication gain, M calculated for the PTMS-equipped APD at a fixed illumination wavelength of 850 nm.

At first, we captured the DC IV performance of the fabricated APD in the dark and under illumination for a range of wavelengths varying from 640-1100 nm and a fixed illumination power of $10 \mu\text{W}$ as shown in Fig. 3(a). The fabricated devices undergo a breakdown at ~ 8.0 V in alignment with the doping design. Based on the wavelength, response current, and power, we have estimated the external quantum efficiency (EQE) of the device. Figure 3(b) presents a comparison of EQE among the flat and PT-equipped APDs. Introducing the PTs has resulted in a significant increase in the EQE of the APD. Further, we have presented the multiplication gain profile captured for 850 nm illumination wavelength in Fig. 3(c). We have demonstrated a gain, M of 80 units.

To measure the DC linearity of these devices, we have used a *QPhotonics QSP-975-10* laser to enable us with a high. Due to losses in the optical fibers, we have monitored the input current values for each laser power as measured from a power meter near the output of the multimode lensed fiber tip. After collecting the calibrated laser power, the power meter was switched out with the devices under test. The measurements are performed with utmost care to avoid any mishap and prevent the miscalibration of the measurement setup. We have compared the response current of a flat and PT-equipped APD under the illumination of 975 nm wavelength for a range of illumination power varying from 0 to 40 mW. Figures 4(a-b) showcase the high response current captured from flat and PT-equipped APDs. The PT-equipped APD results in a higher current for the same illumination power due to an increased absorption enhancement as anticipated. Further, we have compared APD current response with the illumination power for flat and PT-equipped APDs at a fixed reverse bias of 1 V, as shown in Fig. 4(c).

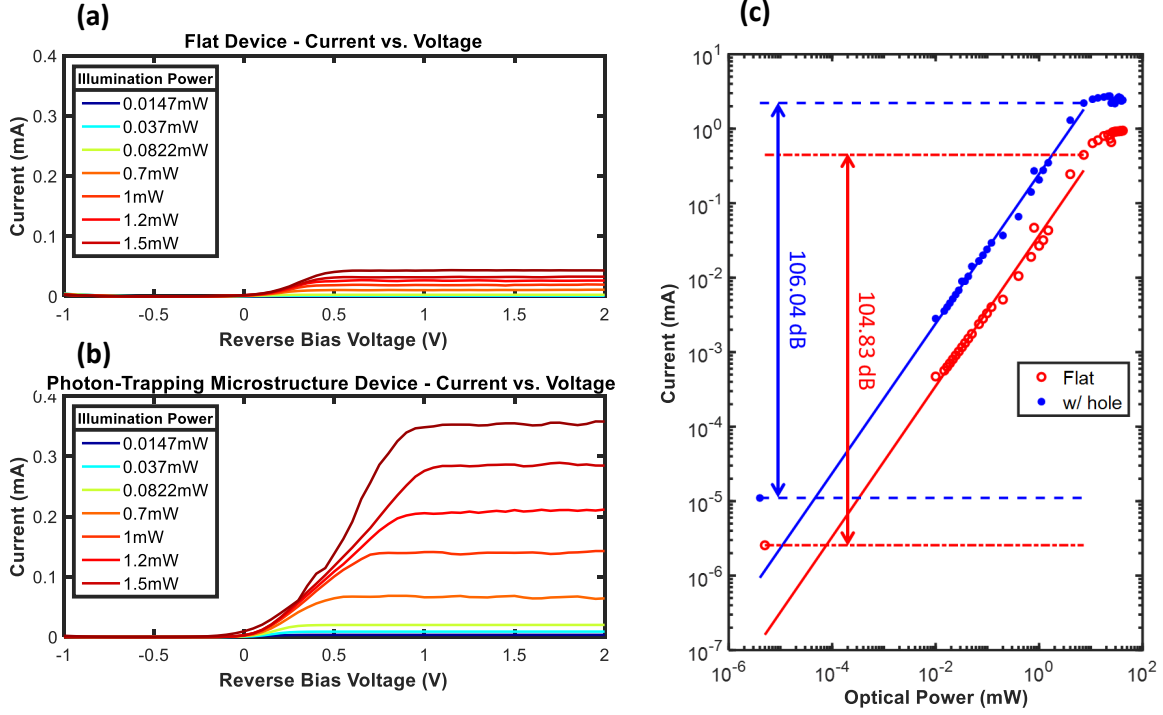


Figure 4. (a) A representative sample of I-V reverse bias data from the flat device. (b) A representative sample of I-V data collected from the device with photon-trapping microstructures under a reverse bias voltage. It can be seen from comparing 2(a) and 2(b) that the device with photon-trapping microstructures has significantly greater photocurrent from the same amount of incident light. (c) A comparison of the current vs. optical power lines plotted on the log scale. By the slope of these lines, the linearity can be determined.

The logarithmic representation of response current and power highlights a linear increase in current with illumination power on a log-log plot. Both flat and PT-equipped APD display a linear trend over a broad range of illumination power. However, in PT-equipped APDs, the linearity experiences an increase from 104.83 dB in flat APDs to 106.04 dB due to electromagnetic wave diffraction and lateral propagation.

Keeping aside the diffraction of EM-wave, a reduction in the absorber layer volume results in an early absorption saturation, i.e., a lower DC linearity. That is the PT-equipped APDs, with their reduced absorber volume should exhibit a lower DC linearity as opposed to the flat device. However, increased diffraction of the EM-waves not only compensates for the carrier saturation in the reduced absorber volume but supersedes the absorption saturation limits and results in higher DC linearity. These PT-equipped devices can be further optimized to enable further enhancement in the DC linearity.

4. CONCLUSION

We design an avalanche photodiode with sub-10V breakdown voltage. To enhance the absorption efficiency, we have introduced photon-trapping microstructures (PTMS) into the APDs. We present a detailed DC IV characterization of the fabricated APDs to demonstrate the illumination sensitivity for a wide range of wavelengths varying from 640 nm to 1100 nm. We show a significant enhancement in the absorption efficiency over the entire range of wavelengths by introducing the PTMS into the APDs in comparison to that of the flat device. Further, we have performed a DC linearity study, and show the DC linearity increases from 104.83 dB to 106.04 dB with the introduction of PTMS into the APDs. This increased linearity ensures uniform absorption in the device for up to 10 mW of optical power.

ACKNOWLEDGMENTS

This work was supported in part by the UC Davis Engineering Dean's Collaborative Research (DECOR) award, the National Institute of Biomedical Imaging and Bioengineering NCIBT grant # 1-P41-EB032840-01, and the National Science Foundation Award Number 2117424 and PFI-TT 2329884. Part of this study was carried out at the UC Davis Center for Nano and Micro Manufacturing (CNM2).

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