High-speed PiN photodiode design space exploration to break the speed-efficiency trade-off

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ABSTRACT

Ever-evolving imaging and low-to-single photon-count detection applications demand high-speed, efficient, and complementary metal oxide semiconductor (CMOS) compatible photodetectors. Due to the non-overlapping research and development in the CMOS logic and optoelectronic industry, holistic system optimization is lacking. We propose a PiN device design method addressing the speed-efficiency trade-off and enabling an independent optimization of both speed and absorption efficiency. We present a hybrid device structure combining lateral and vertical PiN architectures. We introduce a highly doped buried P^+- region connecting the top P^+- contact doping and separating the N^+-contact doping by a critical width. The top P^+- and N^+- contacts are laterally separated by an i-layer for absorption. The use of a lateral i-layer enables a larger volume for efficient photon absorption, and the presence of a highly doped P^+- region enables an efficient collection of slow-moving holes after the illumination is turned off. The critical i-layer width sandwiched between the buried P^+- region and the N^+- contact doping facilitates an efficient conduction path. We optimize the critical width (optimized width = 200 nm) for device capacitance and the admittance to maximize the response time (rise time, fall time, and full-width half maxima). The optimization is performed using ATLAS Silvaco technology computer-aided design software. The optimized device structure possesses 22 GHz 3 dB bandwidth (BW = 0.35/Fall-time) at 850 nm illumination wavelength as against 0.6-10 GHz 3 dB bandwidth range for conventional PiN devices. We also show that reducing the critical width to zero results in impact ionization drive avalanche phenomenon at ∼6 V applied bias, making these devices suitable for low-power and low-photon count detection. With a large absorber width, an optimized critical conduction path, and a low-bias trigger avalanche process, the proposed photodiodes result in high-speed, high-bandwidth, low-photon count detection, essential for state-of-the-art light detection and ranging systems and the single-photon detectors for quantum communications.

Keywords: Si-PiN, CMOS compatible, high-speed detection, speed-efficiency trade-off

1. INTRODUCTION

Optoelectronic technology has grown rapidly in the past few decades to enable and support numerous applications involving the light-matter interaction. The use of optoelectronic devices such as photodiodes, is widespread. High-speed silicon-compatible photodiodes are in high demand due to their transcendent applications across domains in data communication, photon detection, and advanced imaging. To cater to the need for visible light and near-infrared wavelength applications (e.g., visible light communication,[1] fluorescence lifetime imaging,[2] and light detection and ranging[3]), semiconductors such as silicon,[4–8] GaAs,[9] and InGaAs[10–12] are being explored. In addition to the type of absorber material, various device architectures such as metal-semiconductors-metal detectors, lateral illumination photodiodes,[13] PiN,[7,8] avalanche photodiodes (APD),[14,15] and single-photon detectors are proposed for high-speed communication and imaging applications. Researchers have also demonstrated high absorption efficiency and speed by introducing the photonic crystals into the detectors.[14–18]

Researchers have demonstrated tremendous performance with 3 dB bandwidths as 50+ GHz in an InGaAs-based PiN photodiode,[10,13] 30 GHz in germanium on SOI-based lateral PiN,[19] 20 GHz in silicon detectors by

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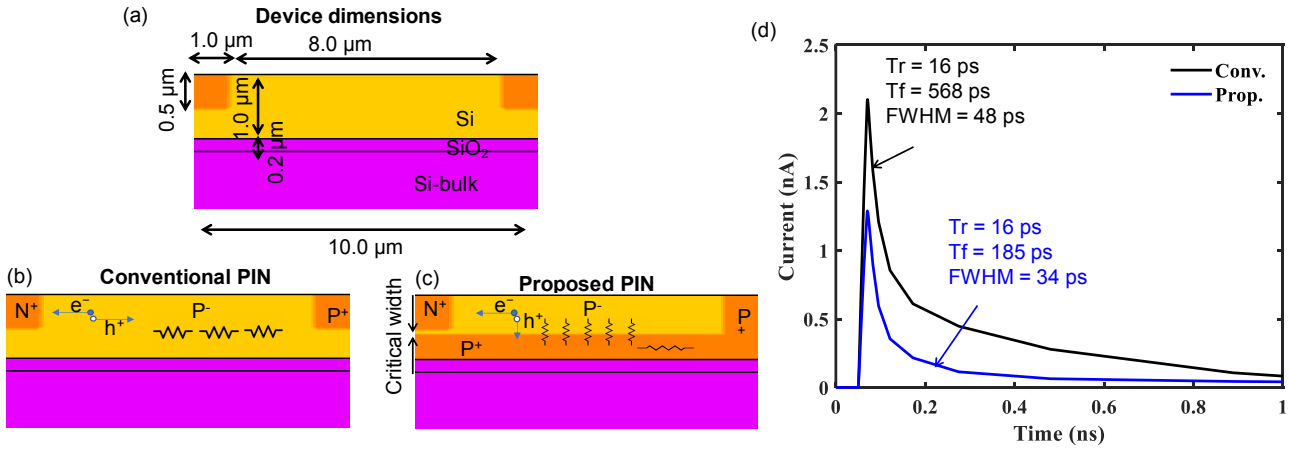

Figure 1. Comparing the proposed device architecture with the traditional lateral PiN device. (a) The conventional PiN marked with the device dimensions simulated in ATLAS Silvaco; (b) The conventional architecture presents greater path resistance for generated e^--h^+ pairs; (c) The proposed design decreases path resistance by incorporating a highly doped P^+-type buried layer; (d) A comparison of transient response time between conventional and proposed PiN devices under the illumination of 850 nm wavelength. The lowered path resistance enhances the effective collection of slow-moving holes at the P^+-contact, leading to improved fall time (T_f) and full-width half maxima (FWHM).

The silicon-based PiN and APDs demonstrate exceptional performance and CMOS integrability. However, the absorption versus speed trade-off results in limited performance optimization. A reduction in the absorber layer thickness is shown to improve the bandwidth[21] at the cost of absorber region volume. To fully optimize the performance of the photodiode, this trade-off needs to be broken.

In this work, we present a hybrid PiN photodiode device architecture by combining a lateral and a vertical PiN photodiode. The proposed PiN is planar, i.e., both the N^+- and the P^+- contacts are present on the same level separated by an absorber layer. Further, a buried P^+- layer has been introduced in contact with the top P^+- contact and separating the N^+- contact by a critical width. This unique combination makes the device planar, a feature essential in CMOS process technology, and using silicon as a base material enables homogeneous integration of the proposed device into the existing CMOS process. The lateral absorber region separating the N^+- and P^+- contact enables efficient absorption and the narrow vertical contact separation facilitates a rapid collection of the generated e^--h^+ pairs. First, we present a thorough critical width optimization using 2D device simulations. Further, using the optimized critical width, we present a 3D device performance evaluation for an accurate performance assessment and show significant performance enhancement in comparison to the conventional PiN devices.

2. PROPOSED DEVICE ARCHITECTURE AND SIMULATION SETUP

We have performed the ATLAS Silvaco simulation to characterize the proposed PiN device architecture and compared the performance with that of the conventional lateral PiN photodiode. Figure 1(a) showcases the dimensions used in the simulation of the proposed photodiode. The photodiode is designed on a silicon-on-insulator substrate with an active layer thickness of 1.0 µm. The separation between the N^+- and P^+-contacts is 8.0 µm, and the N^+- and P^+- contact doping depth is 0.5 µm. The SiO_2 buried oxide thickness is 0.2 µm. The N^+- and P^+-contact layer doping is 2×10^{19} cm^{-3}. To accurately capture the device physics, we have enabled the impact ionization and band-to-band tunneling models in addition to the standard recombination

generation (Shockley Read Hall), drift-diffusion, and high-field mobility models. The simulations are performed at room temperature.

Figures 1(b-c) present a conventional lateral PiN and the proposed hybrid PiN device architecture. The hybrid PiN comprises a lateral and a vertical PiN device. The lateral PiN provides direct exposure to electromagnetic (EM) wavelength to the absorber region. The vertical PiN is enabled by implanting a buried highly doped P^+-doped layer (P^+-layer) facilitating a low resistive hole collection as opposed to a highly resistive path in the conventional lateral PiN as shown in Fig. 1(b-c).

In Fig. 1(d), we show the improvement in the transient response of the proposed device. The transient response is captured at 1 V reverse bias voltage, under the illumination of 850 nm wavelength, and 1 $mW.cm^{-2}$ power. Both the conventional PiN and the proposed PiN devices exhibit equivalent rise time ($T_r = 16$ ps). The fall time (T_f) and the full-width-half-maxima (FWHM), on the other hand, show exceptional reductions of 67% and 29% respectively. The T_r is governed by the fast-moving electrons (e^-) and the T_f and the FWHM are governed by the slow-moving holes (h^+). Introducing the P^+- buried layer facilitates a low-resistive path to the P^+- contact that enables a faster collection of the holes and a rapid turn-off after the illumination is turned off.

The performance limiting parameter in the proposed device is the critical width separating the buried P^+-layer and the N^+ contact. The critical width imposes the limitation on the device capacitance and the admittance, the key device parasitics governing the transient response. In the following section, we optimize the critical width to achieve a high-speed photodiode.

3. DEVICE OPTIMIZATION

We have performed the critical width sweep from 0-400 nm with a step size of 100 nm and captured the device capacitance and the admittance. We have used the small signal AC stimulus of 50 mV amplitude and 10 THz frequency (a high-frequency CV provides an accurate measure of the device's response under high-speed opera of the propc

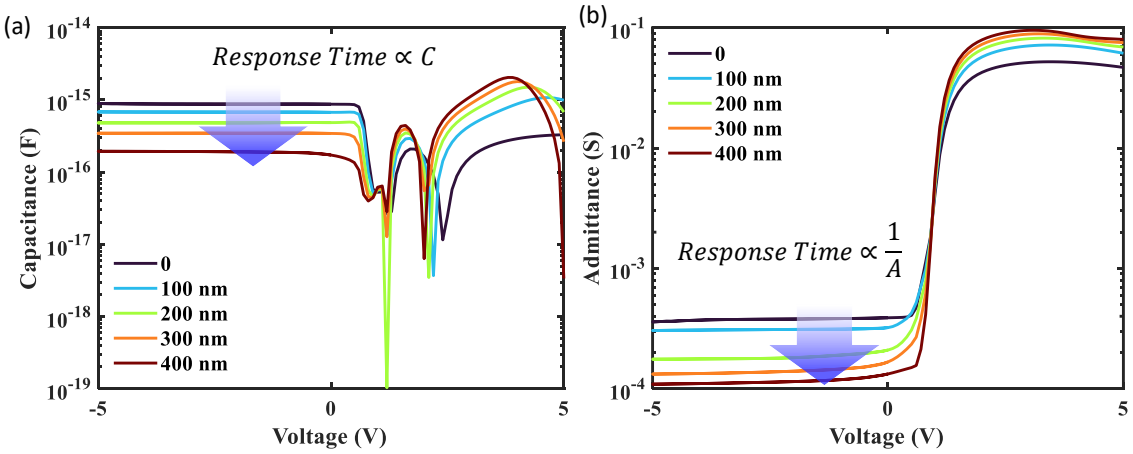

Figure 2. Optimizing device (a) capacitance and (b) admittance through critical width variation. Both capacitance and admittance decrease as the critical width increases. An enlarged critical width leads to a broader depletion width, resulting in reduced capacitance and admittance.

Figures 2(a-b) present the captured capacitance and admittance trends for each critical width ranging from 0 to 400 nm. The increase in the critical width results in a wider depletion region, which in turn reduces the capacitance and the admittance. This reduction is marked in Fig. 2. The response time of the device is proportional to the capacitance and inversely proportional to the admittance. Therefore, to optimize the response time, an intermediate (between 0 to 400 nm) critical width is desired.

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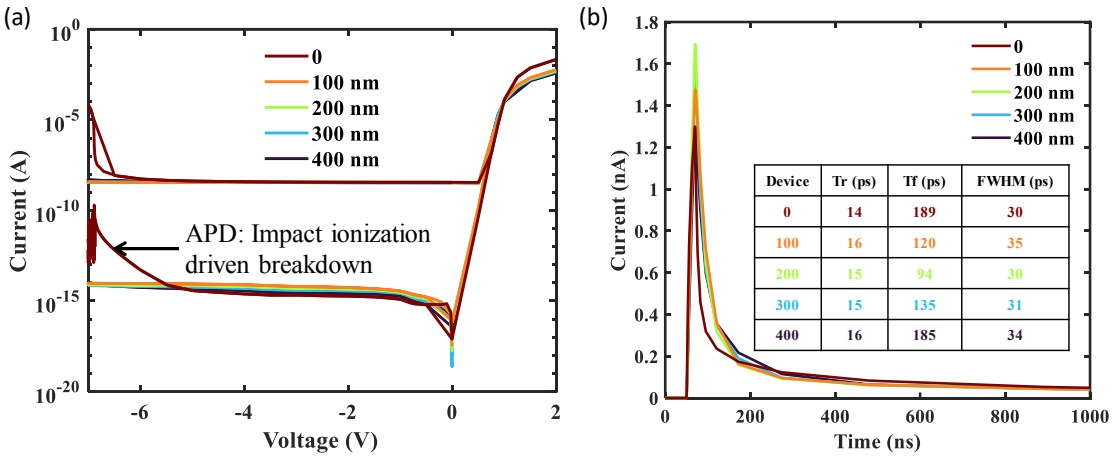

Figure 3. (a) DC IV performance of the proposed devices with varying critical width in the dark and under the illumination of 850 nm wavelength; (b) the transient response capture from the devices and its respective timing responses tabulated. Reduction in the critical width results in an early trigger of the impact ionization and avalanche breakdown. The device with 200 nm critical width exhibits the optimal timing response.

In Fig. 3(a), we present the DC IV performance comparison of the proposed PiN for a range of critical widths in the dark and under the illumination of 850 nm wavelength (power: 1 mW.cm^{-2}). Reduction of the critical width to zero results in a sub-7V trigger of the impact ionization and an early breakdown. The response current does not change significantly with the critical width.

Further, we have simulated the transient response of the proposed PiN for each critical width in Fig. 3(b). We have extracted the T_r, T_f, and FWHM in the table (Inset of Fig. 3(b)). The PiN device with a critical width of 200 nm is shown to have the fastest response as hypothesized earlier.

3.2 3D device simulations

Using the optimized critical width of 200 nm, we designed a 3D PiN photodiode in two different configurations, (1) 1n1p (one N and one P contacts) and (2) 2n3p (two N and three P contacts), as shown in Fig. 4(a-b). In the 2n3p configuration, the interdigitated (ID) contact fingers are separated by 1.0 µm. Figures 4(c-d) present the electric field distribution profiles both in 1n1p and 2n3p configurations. A higher field between the fingers in the 2n3p configuration results in an efficient collection of the generated carriers. Figure 4(e) presents a comparison of DC IV profiles in both configurations. The 2n3p PiN photodiode shows a higher dark current. On the other hand, due to an efficient collection of the generated carriers, the 2n3p PiN exhibits higher external quantum efficiency as shown in Fig 4(f).

Next, we have compared the transient response of both 1n1p and 2n3p PiN photodiodes in Fig. 4(g). Introducing intermediate P^+-regions in the form of ID structures results in faster collection of the carriers and rapid response time as against that in 1n1p PiN photodiode. In Fig. 4(h), we have compared the T_r, T_f, and FWHM of both 1n1p and 2n3p PiN photodiodes and show an exceptional reduction in the response time by adding the ID fingers in 2n3p PiN. With a rapid response time, the 3 dB bandwidth results in 5× increases from 4 GHz to 22 GHz in 2n3p PiN photodiode.

4. DISCUSSION

Bernhard Goll et al., have presented a Spot PiN, with an ultra-low capacitance design,[8] however, they have not utilized the buried P^+ layer for rapid carrier collection. They have demonstrated decent performance with a breakdown voltage of 70 V and a 3 dB bandwidth of 690 MHz. Similarly, W. Gaberl, et al., have also

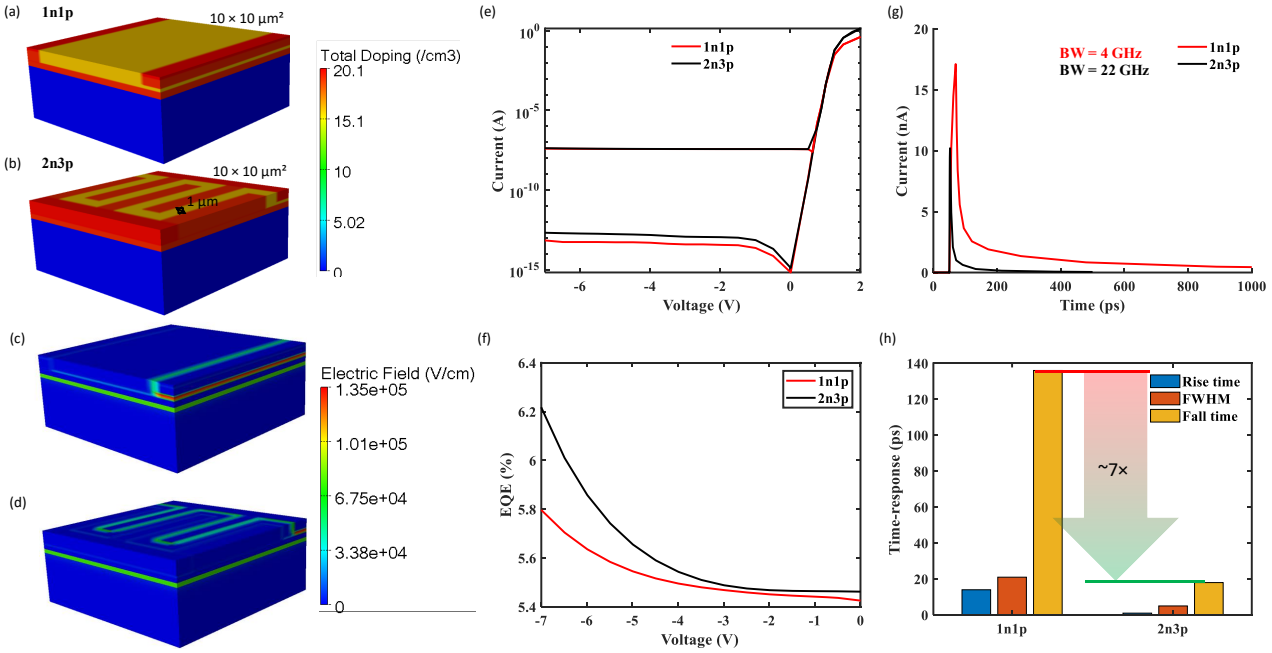

Figure 4. The three-dimensional device simulation: The 3D schematics of the proposed devices with (a) 1n1p (one N and one P contacts) contact arrangement and (b) 2n3p (two N and three P contacts) contact arrangement to show the doping profile. The electric field profile of the (c) 1n1p and (d) 2n3p devices highlights the high-field critical width region. The pixel size of both the devices is 10×10 µm^2. Increasing the contact fingers increases the carrier collection efficiency. (e) A DC IV current characteristics comparison between 1n1p and 2n3p PiN devices. (f) A comparison of the external quantum efficiency at a fixed illumination of 850 nm wavelength. (g) Transient response comparison between 1n1p and 2n3p devices; (h) a bar plot presenting a comparison of rise time, fall time, and FWHM of the two devices. Increasing the contact-fingers facilitates 7× improvement in the fall time and improves the 3 dB bandwidth by 5×.

demonstrated a low capacitance photodiode with integrated silicon fingers[7] and demonstrated a 3 dB bandwidth of 648 MHz. On the contrary, we have optimized the critical width separating the buried P^+- layer from the top N^+- contact and demonstrated an exceptionally high 3 dB bandwidth of 22 GHz. The device performance can be further enhanced by introducing photon trapping features.[14–16]

5. CONCLUSION

We have proposed a hybrid PiN photodiode architecture for CMOS-compatible high-speed applications. We proposed a device design combining the lateral and the vertical PiN by introducing a buried P^+-doped layer for an efficient collection of the generated carriers. We have presented device performance optimization by tuning the critical width separating the buried P^+-doped layer and the N^+ contact layer. We show that a 200 nm thick critical width will result in an optimal transient response of the PiN. By using 3D simulation we demonstrate that using 2n3p interdigitated contact arrangement over 1n1p will result in further enhancement in the response time. We show a 5× increase in the 3 dB bandwidth and 7× reduction in the fall time of the 2n3p PiN in comparison to the 1n1p PiN. These CMOS-compatible, planar PiN devices can be easily incorporated into the existing process line and make sophisticated high-speed detection applications economical and accessible.

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