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Energy Efficient CLB Design Based on Adiabatic Logic for IoT Applications

Wu Yang, Milad Tanavardi Nasab and Himanshu Thapliyal *

VLSI Emerging Design and Nano Things Security Lab (VEDANTS-Lab), Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996, USA; wyang19@vols.utk.edu (W.Y.); mtanavar@vols.utk.edu (M.T.N.)
* Correspondence: hthapliyal@utk.edu

Abstract: Many IoT applications require high computational performance and flexibility, and FPGA is a promising candidate. However, increased computation power results in higher energy dissipation, and energy efficiency is one of the key concerns for IoT applications. In this paper, we explore adiabatic logic for designing an energy efficient configurable logic block (CLB) and compare it to the CMOS counterpart. The simulation results show that the proposed adiabatic-logic-based look-up table (LUT) has significant energy savings for the frequency range of 1 MHz to 40 MHz, and the least energy savings is at 40 MHz, which is 92.94% energy reduction compared to its CMOS counterpart. Further, the three proposed adiabatic-logic-based memory cells are 14T, 16T, and 12T designs with at least 88.2%, 84.2%, and 87.2% energy savings. Also, we evaluated the performance of the proposed CLBs using an adiabatic-logic-based LUT (AL-LUT) interfacing with adiabatic-logic-based memory cells. The proposed design shows significant energy reduction compared to a CMOS LUT interface with SRAM cells for different frequencies; the energy savings are at least 91.6% for AL-LUT 14T, 89.7% for AL-LUT 16T, and 91.3% AL-LUT 12T.

Keywords: configurable logic block; energy efficiency; FPGA; adiabatic-logic-based LUT; adiabatic-logic-based memory cell; IoT

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1. Introduction

The Internet of Things (IoT) is an emerging paradigm in which connected devices exchange data among themselves over networks for complex IoT tasks. It is deeply integrated into our daily activities, from smart home applications employing cameras and lighting systems to sophisticated healthcare solutions leveraging wearables and sensors [1–4]. A wide range of IoT applications raise the need for flexible and high-performance implementation. Field-programmable gate arrays (FPGAs) are a promising solution that provides great computing power and flexibility. An FPGA consists of configurable logic blocks (CLB), routing blocks, and I/O ports, which allows designers to tailor functionality to specific application needs. Furthermore, an FPGA provides numerous I/O ports that meet the communication requirements of different IoT applications. Also, the infinite reconfigurability of FPGAs provides great flexibility and short time-to-market [5–10].

Even with the many benefits of FPGAs, the energy efficiency of FPGA-based IoT applications continues to be one of the major concerns. It is made worse by the limited resources of IoT devices [11,12]. Many existing research studies present micro-architectural approaches to improve the energy efficiency of FPGAs, so it is beneficial to investigate energy efficient techniques at the circuit or system level [13,14]. Adiabatic logic is one such technique for designing energy efficient circuits. Adiabatic-logic-based circuits can effectively reduce the dynamic energy dissipation and recycle the charges from the load capacitance. Many adiabatic logic families, such as efficient charge recovery logic (ECRL) and positive feedback adiabatic logic (PFAL), show significant energy saving at low frequency

ranges [15–18]. The low frequency required for IoT applications makes adiabatic logic a promising candidate for hardware implementation of IoT applications and low-frequency FPGAs [19,20].

Since the main component of an FPGA is the CLB, we investigate the effectiveness and feasibility of applying adiabatic logic to improve the energy efficiency of CLBs. Our proposed designs include an adiabatic-logic-based look-up table (AL-LUT) and adiabatic-logic-based memory cells for constructing the CLB. We present a comprehensive analysis conducted through the Cadence Spectre simulator to evaluate the viability of these designs. Additionally, we demonstrate the feasibility of designing energy efficient CLBs using adiabatic logic. The primary contributions of this study are outlined as follows:

- We propose three adiabatic-logic-based memory cells, which are a 14T design, 16T design, and 12T design.
- We propose an adiabatic-logic-based LUT that can interface different memories such as SRAM cells and adiabatic-logic-based memory cells.
- We present case studies using an adiabatic-logic-based LUT and adiabatic-logic-based memory cells to build a CLB.
- We conduct a comparative analysis of the proposed designs against their CMOS counterpart.
- We also demonstrate that the proposed designs are significantly energy efficient.
- We finally conclude that designing a CLB with adiabatic logic is a viable solution for energy-constrained IoT applications.

This article is organized as follows: Section 2 explains the essential information of FPGA and adiabatic logic. Section 3 describes our proposed adiabatic-logic-based LUT and adiabatic-logic-based memory cells. Section 4 includes the simulation results and discussion, and Section 5 concludes the article.

2. Background

This section provides a brief background of SRAM-based FPGAs and adiabatic logic. Here, we explain the architecture of SRAM-based FPGAs and the structure of a CLB. Further, we present the functionality principles of the LUT and memory cells, which are the building blocks of the CLB. Finally, we discuss the adiabatic logic's energy reduction, charge recycling mechanism, and power clock scheme.

2.1. SRAM-Based Field-Programmable Gate Array (FPGA)

SRAM-based FPGAs have gained much attention in the commercial and academic domains. They stand out due to their flexibility and capability to be dynamically reconfigured, which enable designers to implement custom logic functions and algorithms suited to specific applications, unlike application-specific integrated circuits (ASICs), which have fixed functionality. These features of FPGAs allow designers to develop and test their prototype designs and reduce the time-to-market period [5,21]. Figure 1 presents the structure of an SRAM-based FPGA, where the blue blocks are the CLB, the yellow blocks are the switch block, the green blocks are the I/O port, and the parallel lines are the interconnect [22]. Switch blocks and interconnects are used in an SRAM-based FPGA to pass the signals between different CLBs. The other fundamental building block of the FPGA is the CLB. The CLB mainly consists of three parts: (1) look-up table (LUT), (2) flip flops, and (3) SRAM cells [21,23].

The LUT consists of a tree-like multiplexer and an array of SRAM cells. Figure 2 shows the basic structure of the LUT and SRAM cell in an FPGA [23,24]. When the designer programs the SRAM-based FPGA, SRAM cells store the configuration data of the logic function and routing data of the connections between CLBs. Once inputs are applied to the LUT, the LUT decodes the inputs to select the corresponding SRAM cell. The value in the SRAM cell is amplified as the output of the LUT.

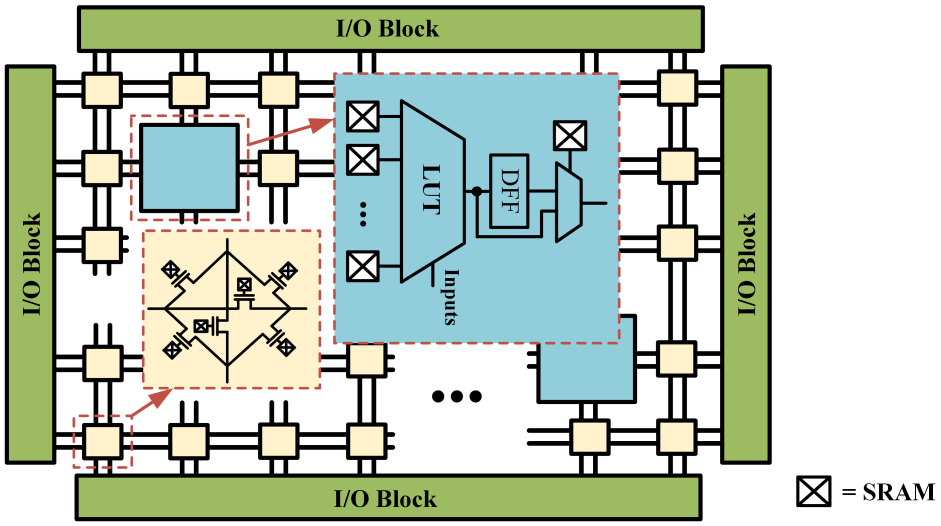

Figure 1. The structure of an SRAM-based FPGA.

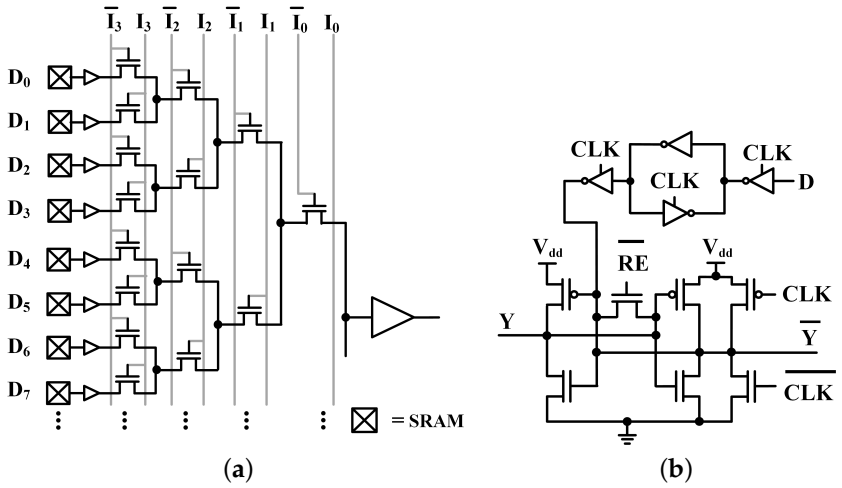

Figure 2. The structure of the circuit: (**a**) CMOS LUT and (**b**) SRAM in FPGA, where I_n is the input and $\overline{I_n}$ is its complement, and D_m is the configuration data (n = 1, 2 . . . 4 and m = 1, 2 . . . 16).

2.2. Adiabatic Logic

Adiabatic logic refers to a specialized technique in digital circuit design that seeks to minimize energy consumption. Adiabatic-logic-based circuits use a slowly rising and falling power clock, which is sinusoidal in this study due to its less complex design and routing. This feature allows the adiabatic-logic-based circuit to minimize the energy loss due to the voltage differences between two nodes and recover the charges from the load capacitors [15]. Figure 3 illustrates the charging and discharging model for the adiabatic-logic-based circuit in each phase. Typically, the adiabatic-logic-based circuit works in two phases: (i) In the evaluation phase, the power clock rises from the ground (GND) to full swing (V_{dd}) and charges up one of the output nodes through the logic tree F or $\overline{F}$; (ii) the power clock falls from V_{dd} to GND in the recovery phase. Due to the voltage difference, the current flows from the output node to the power clock, leading to charge recovery. Those recovered charges are reused in the next evaluation. The energy dissipation is shown as follows:

$$Energy, E = \frac{RC}{T} C V_{dd}^2 \tag{1}$$

where V_{dd} is the full swing of the power clock, C is the load capacitance, R is the transistor's parasitic resistance, and T is the charging/discharging time of the load capacitor. Compared to conventional CMOS, the adiabatic-logic-based circuit consumes less energy when $T >> 2RC$.

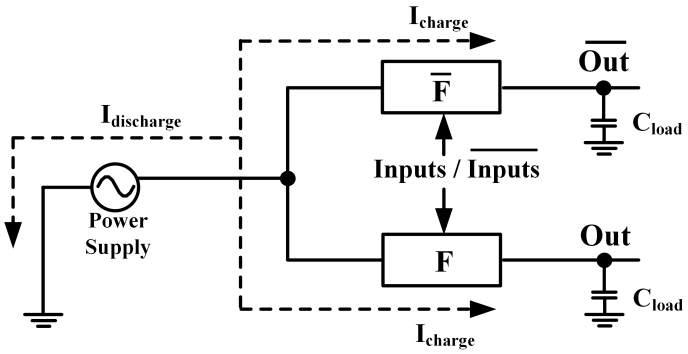

Figure 3. Adiabatic logic charging and discharging model.

3. Proposed Adiabatic-Logic-Based Design

To investigate the benefits of applying adiabatic logic to a CLB, we design an adiabatic-logic-based LUT. Then, we explore the adiabatic-logic-based memory cells for additional energy reduction. We also build a CLB using adiabatic-logic-based LUT with SRAM cells or adiabatic-logic-based memory cells. Finally, two case studies are conducted to evaluate the performance of the proposed designs. All the proposed designs are simulated and compared to their CMOS counterpart.

3.1. Adiabatic-Logic-Based Look-Up-Table (LUT) for Configurable Logic Block (CLB)

Unlike CMOS LUT, an adiabatic-logic-based LUT (AL-LUT) works with a power clock that varies from full swing (V_{dd}) to ground (GND). Once the AL-LUT decodes the input and selects the SRAM cell with a logic value '1' (V_{dd}), it will lead to a short circuit as the power clock is at GND. To avoid a short circuit between the power clock and SRAM cells, we use SRAM cells to drive the NMOS in a tree-like multiplexer. This allows the tree-like multiplexer to function in the proper adiabatic logic manner. Our previous design in [25], which is an adiabatic-logic-based sense amplifier (AL-SA), has been used to properly sense and amplify the value in the SRAM cell. Therefore, the proposed AL-LUT consists of a 5-bit tree-like multiplexer and an AL-SA, as shown in Figure 4. The 5-bit tree-like multiplexer has four select bits (I_0 - I_3 and $\overline{I_0}$ - $\overline{I_3}$), and the fifth bit is the configurable bit from the SRAM cells. The function block F and its complementary $\overline{F}$ have been used on the side of the AL-SA. AL-LUT decodes the inputs, and the power clock charges one of the output nodes of the AL-SA through F or $\overline{F}$. Later, the AL-SA further pulls up the node as the power clock rises to V_{dd}. The waveform of a 16:1 AL-LUT is illustrated in Figure 5, and the detailed evaluation operation is as follows:

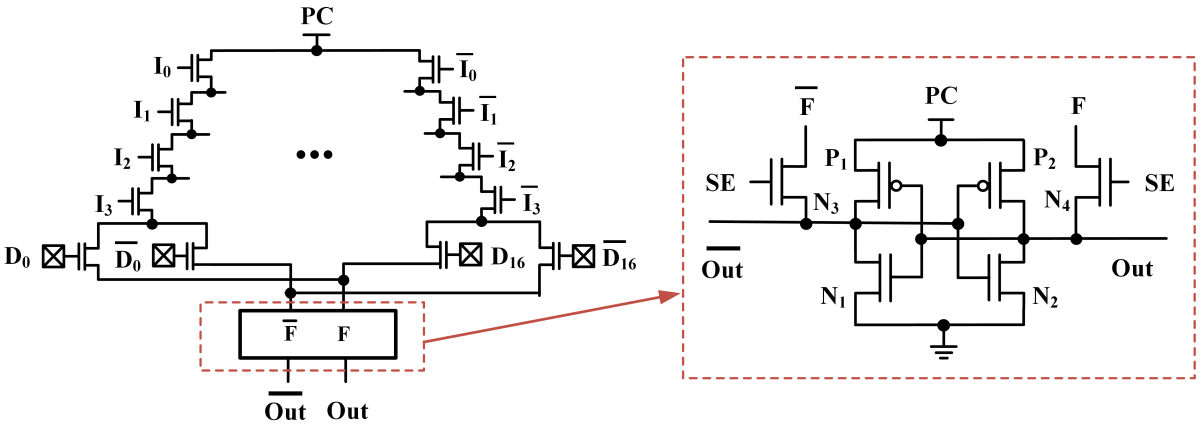

Figure 4. The schematic of the proposed adiabatic-logic-based LUT. The core circuit is shown in the dashed-line box, where I_n is the input and $\overline{I_n}$ is its complement, and D_m are the configuration data and $\overline{D_m}$ are their complements (n = 1, 2 . . . 4 and m = 1, 2 . . . 16).

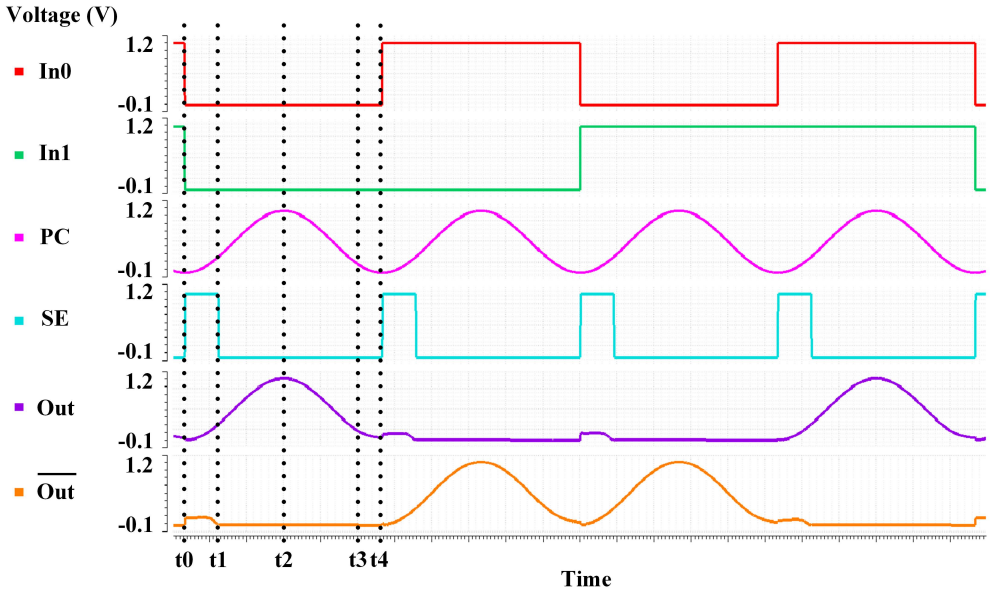

Figure 5. Example of the adiabatic-logic-based LUT's operation (In_2 and In_3 are constant, and PC is the power clock).

- Pre-evaluation: At time = $t0$, a sense enable (SE) signal is applied to the access transistors (N_3 and N_4) of the AL-SA. N_3 and N_4 connect the AL-SA with the logic trees F and $\overline{F}$. Since all inputs are valid, one of the logic trees is ON, which connects one of the output nodes of the AL-SA to the power clock.
- Evaluation: Between time $t0$ and $t1$, the voltage of the power clock (V_{pc}) begins rising, and SE remains at logic value '1' until time = t_1. Assuming the logic tree F is ON, the power clock pulls the Out node up as it rises. The increased voltage of the Out node turns N_1 ON, which results in the $\overline{Out}$ node at the GND. However, V_{pc} is below the threshold voltage of the PMOS (V_{thp}), and P_2 remains inactive.
- Amplifying: At time = $t1$, the SE signal is set to logic value '0'. N_3 and N_4 are OFF, disconnecting the output nodes of the AL-SA from the logic tree F and $\overline{F}$. After time = $t1$, P_2 is ON, which causes AL-SA to pull the Out node up to V_{pc}, while N_1 pulls the $\overline{Out}$ node down to GND.

After the power clock reaches V_{dd}, AL-LUT starts recovering the charges from the load capacitors. The load capacitance charges are recovered through P_2 to the power clock during this phase. The details of the recovery process are as follows:

- Recovering: At time = $t2$, V_{pc} falls from V_{dd}. Hence, V_{pc} is lower than the voltage of the Out node. Due to the potential difference, the current flows from the Out node to the power clock through P_2.
- Idle: At time = $t3$, V_{pc} reaches V_{thp}; this results in turning OFF P_2. Therefore, the discharge process of the adiabatic-logic-based LUT is stopped, and the voltage of the Out node remains at V_{thp}. The AL-LUT ends the charge recovery process after V_{PC} falls below V_{thp}.

3.2. Proposed Adiabatic-Logic-Based Memory Cell

To further reduce energy dissipation, we explored using an adiabatic-logic-based memory cell to replace the SRAM cell in the FPGA. Figure 6 shows the basic block of the proposed adiabatic-logic-based memory cell, which has two operation modes: hold mode and write mode. The circuit mode depends on the inputs of N_3 and N_4. If the inputs of N_3 and N_4 are at logic value '0', the circuit is in hold mode. If the logic values of the inputs of N_3 and N_4 are complementary, the circuit is in write mode. In write mode, based on the values of the inputs of N_3 and N_4, one of these NMOSs is ON and connects its

corresponding output to the power clock (PC), and the data will be latched in the core circuit. After each write or hold operation, the output node with logic value '1' is discharged through the PMOS (P_1 or P_2). However, the PMOS transistors can not discharge to logic value '0' in a full-swing manner since they will be OFF for the gate to source voltages below V_{thp}. Accordingly, there will be some residual charge in one of the output nodes of the core circuit. We assume the Out node has logic value '0' and the $\overline{Out}$ node has logic value '1' in the first clock cycle (from t0 to t1). Therefore, P_2 cannot completely discharge the $\overline{Out}$ node, and some residual charge remains at this node. In the next clock cycle, if the circuit is in hold mode, the power clock starts rising from the GND toward V_{dd}, and P_2 turns ON faster than P_1 due to those residual charges. Accordingly, the core circuit sets the $\overline{Out}$ node as logic value '1' and the Out node as logic value '0'. Figure 7 shows the waveform of the basic block of the proposed adiabatic-logic-based memory cell. In this figure, the logic values of '0' and '1' are written into the memory cell's Out and $\overline{Out}$ nodes, respectively. In the next two clock cycles, no new input is applied to the circuit, and the circuit is in hold mode, which leads to repeated outputs.

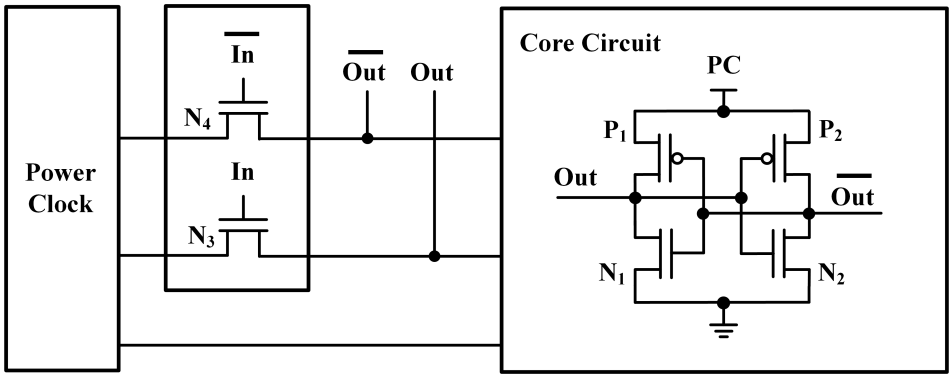

Figure 6. The structure of the basic block of the proposed adiabatic-logic-based memory cell, where PC is the power clock.

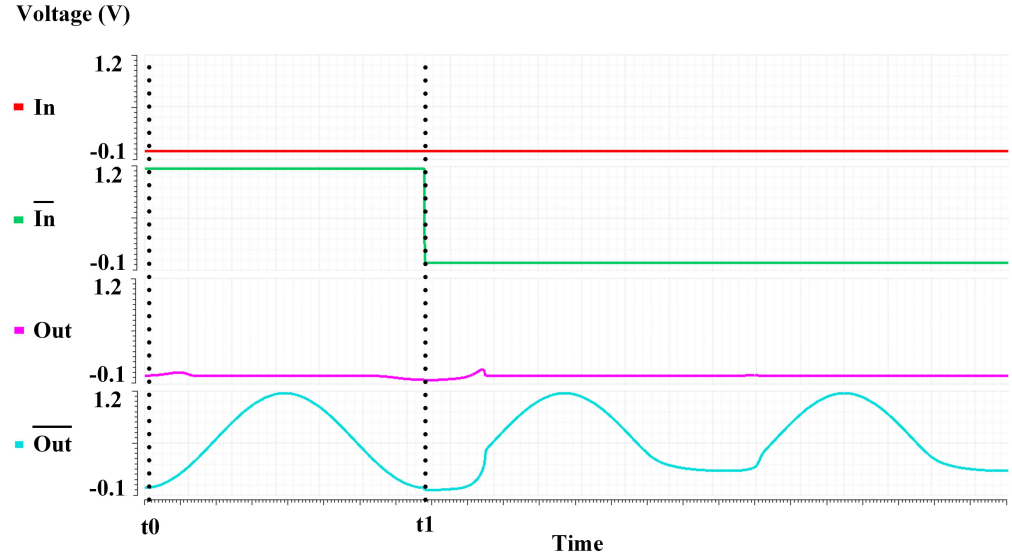

Figure 7. The waveform of the basic block of the proposed adiabatic-logic-based memory cell. When no inputs are applied to the basic block, it generates the repeated output after time = t1.

It is noteworthy that Figure 6 is a basic block, and the actual proposed adiabatic-logic-based memory cell designs will be presented in the following section.

Since adiabatic logic works in a pipeline fashion, we can cascade the adiabatic-logic-based memory cell to build a 16-bit memory cell with a two-phase sinusoidal power

clock scheme. However, cascading the adiabatic-logic-based memory cells will result in a synchronization issue. For the adiabatic-logic-based circuit, the output is only valid during a certain period of the clock cycle: typically when the power clock is at logic value '1' or V_{dd}. Again, the 16-bit memory cell requires two power clocks for proper operation, which leads to invalid output from half of the memory cells. However, AL-LUT requires all valid outputs from the memory cell during the evaluation phase. Therefore, 16:1 AL-LUT cannot generate proper outputs when interfacing with a 16-bit adiabatic-logic-based memory cell. Figure 8a shows a 16:1 AL-LUT interfacing with a 16-bit adiabatic-logic-based memory cell ($PC0$ is power clock 0 and $PC1$ is power clock 1 at a 180-degree phase shift). AL-LUT is connected to $PC0$, and the 16-bit adiabatic-logic-based memory cell is connected to both power clocks ($PC0$ and $PC1$). Here, the odd cells (D_1, D_3, D_5, ..., D_{15}) are connected to $PC0$, and the even cells (D_0, D_2, D_4, ..., D_{14}) are connected to $PC1$. When the AL-LUT performs the evaluation, $PC0$ starts rising from GND, and $PC1$ is at V_{dd}. Therefore, the even cells have valid outputs, and the odd cells do not have valid outputs since the odd cells are in the evaluation phase. These invalid outputs from the odd cells result in false evaluation of the AL-LUT.

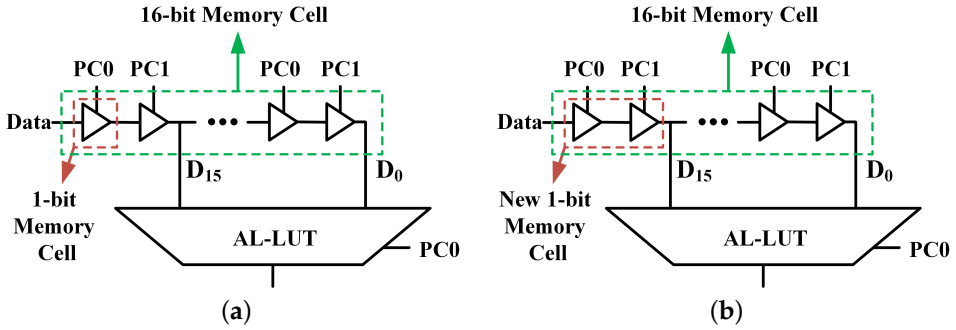

Figure 8. Illustration of the 16:1 AL-LUT interfaced with the 16-bit adiabatic-logic-based memory cell: (**a**) Synchronization issue due to invalid output from the memory cell. (**b**) The proposed solution for solving the synchronization issue.

To resolve this synchronization issue, we need to duplicate the adiabatic-logic-based memory cell to provide valid outputs for the AL-LUT. As shown in Figure 8b, we include another adiabatic-logic-based memory cell to form the new 1-bit memory cell. Hence, the new 1-bit memory cell has two copies of the data (where one copy is stored in the even cell, and the other is stored in the odd cell). Since the AL-LUT is connected to $PC0$ and the odd cell in the new 1-bit memory cell is connected to $PC1$, the odd cell can provide valid output to the AL-LUT. Therefore, we can cascade the new 1-bit memory cell to build the 16-bit adiabatic-logic-based memory cell for the 16:1 AL-LUT.

During the writing process of the 16-bit adiabatic-logic-based memory cell, all data are written to the first memory cell (D_{15}), and it propagates the data through the rest of the memory cells. After the last data are written to D_{15}, the writing process ends, and no inputs will be applied to the 16-bit adiabatic-logic-based memory cell. However, the data in D_{15} will continue propagating through the rest of the memory cells, resulting in all the memory cells having the same data as D_{15}. Hence, we propose three adiabatic-logic-based memory cells to stop the propagating after the last data are written.

3.2.1. Proposed 14T Adiabatic-Logic-Based Memory Cell

The proposed 14T adiabatic-logic-based memory cell is illustrated in Figure 9a. It consists of MC_1 for storing the data and MC_2 [18] for supplying output to the AL-LUT. MC_1 has two pairs of NMOS (N_5, N_7 and N_6, N_8) for controlling the writing process. N_5 and N_6 stop the propagation after the writing process is completed, and N_7 and N_8 are used to prevent the input nodes of N_9 and N_{10} from floating in hold mode.

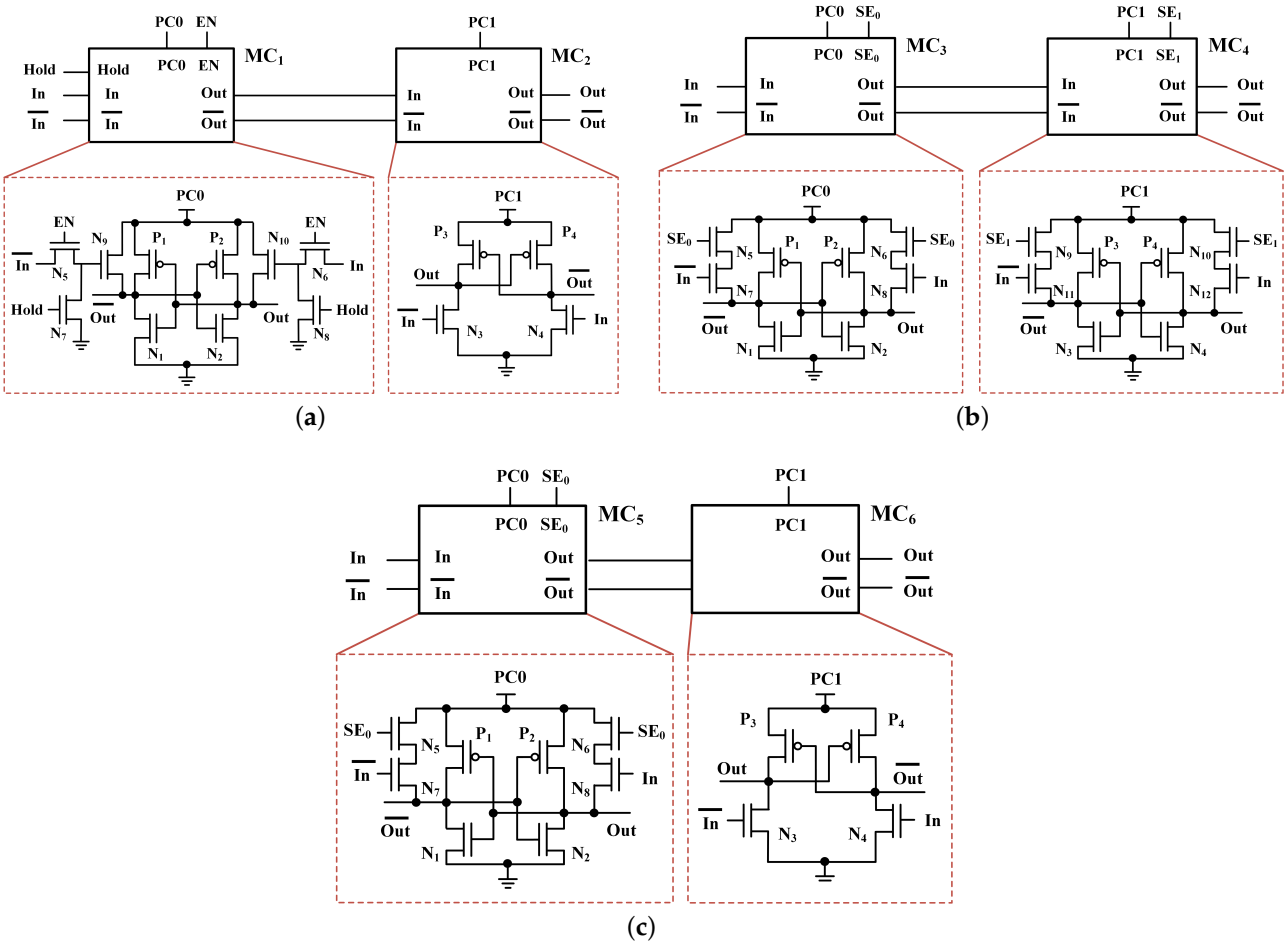

Figure 9. Proposed 1-bit adiabatic-logic-based memory cell: (**a**) 14T adiabatic-logic-based memory cell, (**b**) 16T adiabatic-logic-based memory cell, and (**c**) 12T adiabatic-logic-based memory cell.

The writing process begins when the Enable (EN) signal is applied to the enable transistors (N_5 and N_6) of MC_1 while the Hold signal is at logic value '0'. The enable transistors pass the inputs (In and $\overline{In}$) to the input transistors (N_9 and N_{10}). Assuming In is at logic value '1' and $\overline{In}$ is at logic value '0', these set MC_1's Out node as logic value '1' and $\overline{Out}$ node as logic value '0'. Therefore, MC_1 stores the data, which completes the writing process. Meanwhile, the EN is set to logic value '0' to turn N_5 and N_6 OFF, and Hold is set to logic value '1' to turn ON N_7 and N_8. N_7 and N_8 pull the input nodes of N_9 and N_{10} to GND, ensuring the correct functionality of the 14T memory cell. Further, the outputs from MC_1 lead MC_2 to set its Out node as logic value '1' and $\overline{Out}$ node as logic value '0' when $PC1$ starts rising from GND. MC_2 provides the valid output to AL-LUT when $PC1$ reaches V_{dd}. It is noteworthy that MC_2 also acts as a buffer, and unlike its CMOS counterpart, the proposed 14T memory cell does not need a buffer circuit as an interface with the LUTs.

3.2.2. Proposed 16T Adiabatic-Logic-Based Memory Cell

The 16T adiabatic-logic-based memory cell (Figure 9b) has two AL-SA-based memory cells (MC_3 and MC_4). The AL-SA-based memory cell adopts the AL-LUT design and consists of an AL-SA with an extra pair of NMOSs (N_5 and N_6). The extra pair of NMOSs are the input transistors, and N_7 and N_8 are the access transistors. The writing process of the proposed 16T memory cell is similar to that of the AL-LUT. We assume the inputs In and $\overline{In}$ are at logic values '1' and '0', respectively. SE_0 is set to logic value '1' for a short amount of time and will be applied to MC_3 to enable the writing process. $PC0$ charges up the Out node in MC_3 through N_6 and N_8, storing the data in MC_3. It further amplifies the

data after SE_0 is set to logic value '0'. Similarly, MC_4 evaluates and stores the data when SE_1 is applied. After SE_1 is set to logic value '0', the writing process ends, and MC_4 further amplifies the data. In hold mode, SE_0 and SE_1 remain at logic value '0' to avoid altering the data in MC_3 and MC_4. Therefore, MC_3 and MC_4 generate repeated outputs while the circuit is in hold mode. Also, like the proposed 14T memory cell, the proposed 16T memory cell does not need a buffer as an interface with LUT, and MC_4 acts as a buffer, too.

3.2.3. Proposed 12T Adiabatic-Logic-Based Memory Cell

Adiabatic logic is dual-rail in nature, leading to an increase in the circuit size compared to its CMOS counterpart. Reducing the memory cell size will result in an overall area reduction when designing the CLB. Therefore, we propose a 12T adiabatic-logic-based memory cell by replacing MC_4 in the 16T memory cell with MC_2 from the 14T memory cell. Figure 9c shows the schematic of the 12T memory cell. In the 12T memory cell, MC_5 stores the data, and MC_6 supplies output to the AL-LUT.

During the write operation of the 12T memory cell, SE_0 is set to V_{dd} for a short amount of time and is then applied to MC_5. Based on the inputs, one side of the output nodes of MC_5 will be pulled up by $PC0$. Later, the data are latched into MC_5, and SE_0 is set to logic value '0'. Further, the output will be amplified by MC_5, which completes the writing process. When $PC0$ reaches V_{dd}, the output of MC_5 becomes valid for MC_6. Therefore, MC_6 will generate the proper output for the AL-LUT. After writing the data into the memory cell, SE_0 remains at the logic value '0' to stop propagating the data to the other memory cells. It is noteworthy that, like the other proposed memory cell in this paper, the proposed 12T memory cell does not need buffer circuitry as an interface with LUT.

4. Simulation Results and Discussion

The proposed designs and their counterpart are investigated and compared in this section. The schematic was created with TSMC 65 nm using Cadence Virtuoso and simulated using Cadence Spectre. In order to eliminate the effects of the initial conditions of the circuits, the configurations of the CLBs are written on the proposed memory cells and their CMOS counterpart. It is noteworthy that the results of this process have not been taken into account in the reported results. Further, the energy performance of all the designs is evaluated by energy per cycle for this study.

4.1. Proposed Adiabatic-Logic-Based LUT

The simulation results and comparison of the proposed adiabatic-logic-based LUT and its CMOS counterpart have been investigated. The simulation results are listed in Table 1 for the frequency range from 1 MHz to 40 MHz. The results show that the AL-LUT has significantly less energy dissipation than its CMOS counterpart. The energy consumption of the COMS LUT ranges from 196.9 fJ to 13.18 fJ, and the proposed adiabatic-logic-based LUT ranges from 13.79 fJ to 0.931 fJ. Figure 10 shows the energy saving of the proposed design compared to its CMOS counterpart for different frequencies. The proposed AL-LUT has a minimum savings of 92.94% at 40 MHz and a maximum savings of 93.67% at 12.5 MHz. Further, the energy savings are relatively consistent across the 1 to 40 MHz range.

Table 1. Energy performance (fJ/cycle) comparison for proposed 16:1 adiabatic-logic-based LUT design at different frequencies.

Frequency (Hz)	1 M	2.5 M	5 M	10 M	12.5 M	20 M	40 M
CMOS LUT [23,26]	196.9	84.03	46.44	27.69	23.94	18.25	13.18
Proposed AL-LUT	13.79	5.691	3.032	1.757	1.515	1.173	0.931

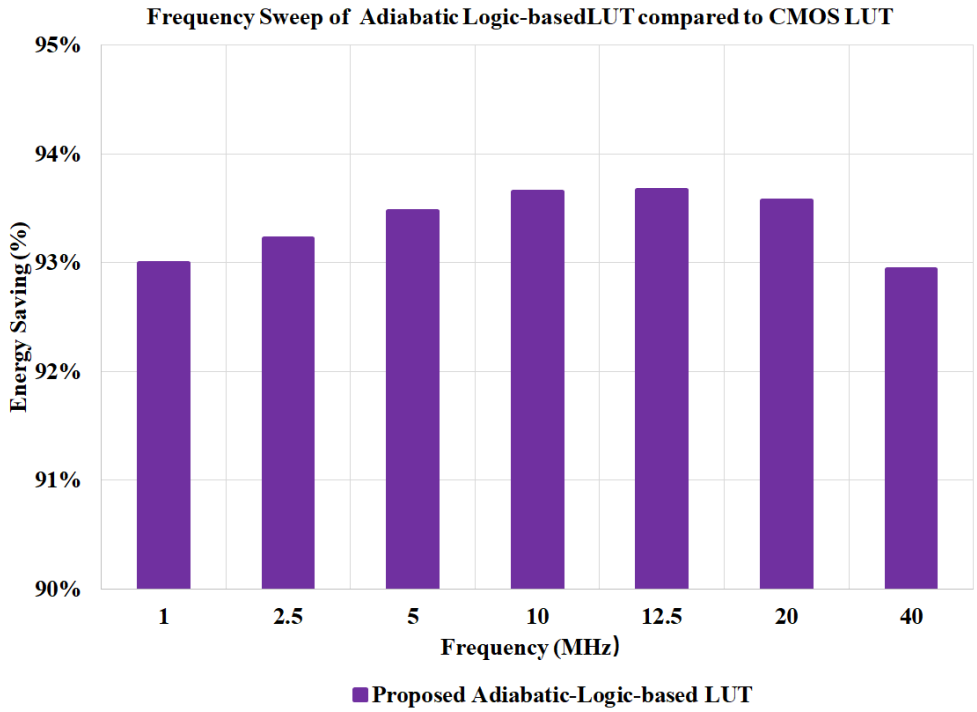

Figure 10. The energy savings of the proposed adiabatic-logic-based memory design compared to the CMOS LUT at different frequencies.

4.2. Proposed Adiabatic-Logic-Based Memory Cells

The energy consumption of the proposed adiabatic-logic-based memory cells for 16-bit memory is presented in Table 2. The results show that all proposed adiabatic-logic-based memory cells consume significantly less energy compared to the SRAM cell. For example, the SRAM cell dissipates 37.25 fJ at 12.5 MHz. The energy consumptions of the proposed designs at this frequency are 3.872 fJ, 4.823 fJ, and 4.041 fJ for the 14T memory cell, the 16T memory cell, and the 12T memory cell, respectively. The proposed 14T memory cell has the lowest energy consumption among the three proposed designs. Figure 11 shows the energy savings of the proposed 16-bit adiabatic-logic-based memory cells. The results show the energy savings for all of the proposed memory cells. In the frequency range of 1 MHz to 40 MHz, the maximum and minimum energy savings of the three proposed designs are 90.2% and 84.2%, respectively. The best energy savings are reached at 1 MHz for all of the proposed designs. At 1 MHz, the energy savings are 90.2% for the 14T memory cell, 88.2% for the 16T memory cell, and 90.0% for the 12T memory cell.

Table 2. Energy performance (fJ/cycle) comparison for proposed 16-bit adiabatic-logic-based memory cell at different frequencies.

Frequency (Hz)	1 M	2.5 M	5 M	10 M	12.5 M	20 M	40 M
SRAM cell [24]	435	175.6	89.13	45.9	37.25	24.28	13.47
Proposed 14T Design	41.9	17.25	8.905	4.715	3.872	2.595	1.587
Proposed 16T Design	51.4	21.01	10.87	5.826	4.823	3.296	2.122
Proposed 12T Design	43.48	17.79	9.193	4.901	4.041	2.741	1.720

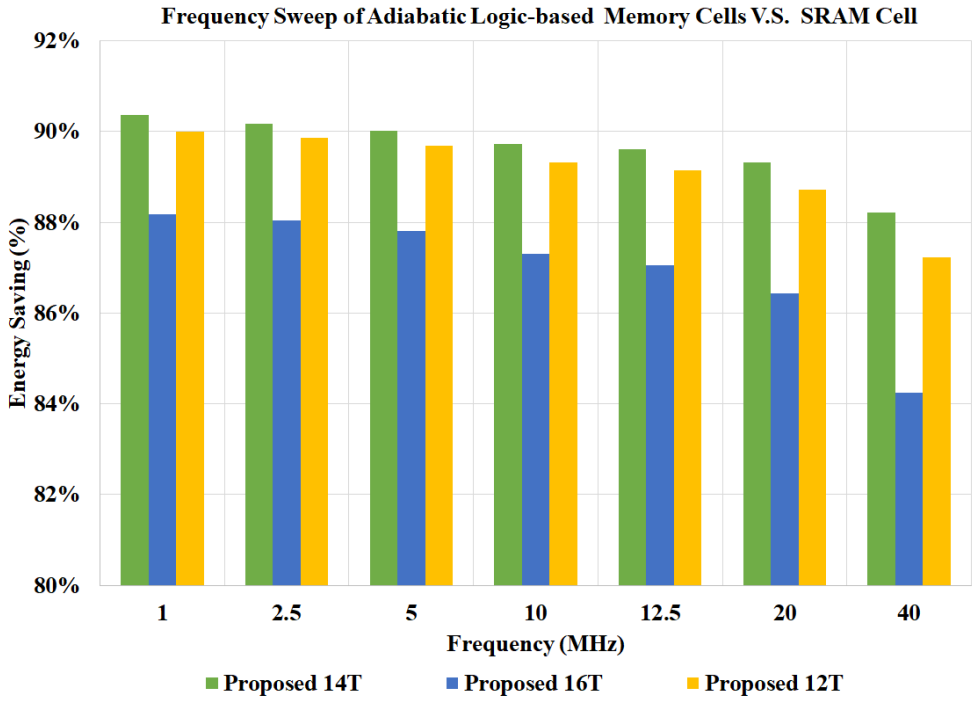

Figure 11. The energy savings of the proposed adiabatic-logic-based memory design compared to the CMOS-based SRAM at different frequencies.

4.3. Case Study: Combining Proposed Adiabatic-Logic-Based LUT with SRAM Cell and Proposed Adiabatic-Logic-Based Memory Cells for Building CLB

To better understand the performance of the proposed designs using adiabatic logic, different CLBs using an SRAM cell and the proposed memory cells combined with AL-LUT and CMOS LUT (C-LUT) are simulated. Different simulated combinations of memory cells and LUTs to build different CLBs are shown in Table 3.

Table 3. Case study: building the CLB with the adiabatic-logic-based LUT and the different memory cells.

CLB Design	Look-Up Table	Memory Cell
C-LUT with SRAM	CMOS LUT [23,26]	SRAM cells [24]
AL-LUT with SRAM	Proposed Adiabatic-Logic-Based LUT	SRAM cells [24]
AL-LUT with 14T	Proposed Adiabatic-Logic-Based LUT	Proposed Adiabatic-Logic-Based 14T Memory Cell
AL-LUT with 16T	Proposed Adiabatic-Logic-Based LUT	Proposed Adiabatic-Logic-Based 16T Memory Cell
AL-LUT with 12T	Proposed Adiabatic-Logic-Based LUT	Proposed Adiabatic-Logic-Based 12T Memory Cell

4.3.1. Proposed Adiabatic-Logic-Based LUT with Different Memory Cells at Different Frequencies

The energy consumption of the different designs is listed in Table 4. Even in the case of only using AL-LUT instead of C-LUT and combining it with SRAM cells (AL-LUT with SRAM), the energy consumption is reduced compared to C-LUT with SRAM. In addition, using the proposed adiabatic memory cells alongside the AL-LUT to implement the CLB reduces energy consumption even further. For example, at 12.5 MHz, the energy consumptions of C-LUT with SRAM and AL-LUT with SRAM are 61.19 fJ and 42.46 fJ, respectively. Also, at 12.5 MHz, the AL-LUT with 14T, AL-LUT with 16T, and AL-LUT with 12T designs use 5.04 fJ, 5.992 fJ, and 5.21 fJ, respectively, which is significantly lower than the energy consumption of AL-LUT with SRAM and C-LUT with SRAM. Also, comparing

the energy consumption of AL-LUT with SRAM and CLBs using AL-LUT and adiabatic-logic-based memory cells shows the crucial role of the adiabatic-logic-based memory cells in maximizing energy savings. It is also noteworthy that this significant reduction in energy consumption is achieved across all frequencies from 1 MHz to 40 MHz.

Table 4. Energy performance (fJ/cycle) comparison for proposed 16:1 adiabatic-logic-based LUT with different memory cells at different frequencies.

Frequency (Hz)	1 M	2.5 M	5 M	10 M	12.5 M	20 M	40 M
C-LUT with SRAM	632	259.6	135.6	73.59	61.19	42.53	26.65
AL-LUT with SRAM	520.1	208.9	105	52.89	42.46	26.81	13.78
AL-LUT with 14T	53.03	21.85	11.34	6.092	5.04	3.451	2.196
AL-LUT with 16T	62.65	25.61	13.31	7.204	5.992	4.153	2.733
AL-LUT with 12T	54.71	22.39	11.63	6.279	5.21	3.597	2.331

Figure 12 shows the energy savings of the proposed designs compared to C-LUT with SRAM. The energy savings of AL-LUT with SRAM varies from 17.71% to 48.29% at the frequency range of 1 MHz to 40 MHz. It achieves more energy savings as the frequency increases. However, it has significantly lower energy savings than the other proposed designs. For example, the CLB designs with AL-LUT and adiabatic-logic-based memories have relatively consistent energy savings of around 91% across the frequencies from 1 MHz to 40 MHz compared to C-LUT with SRAM. Among the proposed designs, AL-LUT with 14T has the best energy saving.

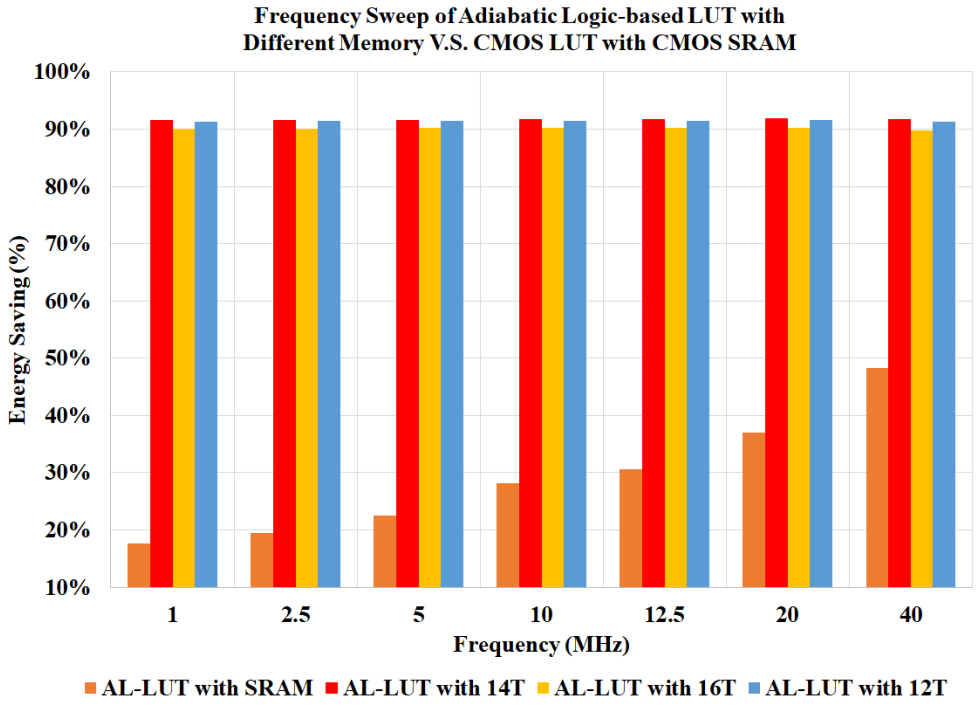

Figure 12. The energy savings of the 16:1 adiabatic-logic-based LUT with different memory designs compared to the CMOS-based LUT with SRAM cells at different frequencies.

4.3.2. Proposed Adiabatic-Logic-Based LUT with Memory Cells with Different Supply Voltage

In order to investigate the effects of different supply voltage values on the proposed designs, the designs in Table 3 are simulated with different power supply voltages. Table 5 presents the energy consumption of the five designs at 12.5 MHz. All proposed designs

consume significantly less energy than their CMOS counterpart in the voltage range of 1.2 V to 0.7 V. As expected, AL-LUT with SRAM has significantly less energy savings compared to the AL-LUT interfacing with the proposed adiabatic-logic-based memory cells.

Table 5. Energy performance (fJ/cycle) comparison for proposed 16:1 adiabatic-logic-based LUT with different memories using different supply voltages.

Voltage (V)	1.2	1.1	1.0	0.9	0.8	0.7
C-LUT with SRAM	61.19	42.36	28.99	38.93	12.89	8.196
AL-LUT with SRAM	42.46	29.58	20.36	27.24	9.176	5.955
AL-LUT with 14T	5.04	3.712	2.702	3.421	1.418	1.018
AL-LUT with 16T	5.992	4.325	3.091	3.711	1.58	1.131
AL-LUT with 12T	5.21	3.761	2.686	3.26	1.369	0.973

Figure 13 shows the energy savings of the proposed designs compared to their CMOS counterpart with supply voltages ranging from 1.2 V to 0.7 V. At 0.7 V, the energy saving of AL-LUT with SRAM is 28.2%, which is significantly lower energy savings compared to the other proposed CLB designs. For example, also at 0.7 V, AL-LUT with 14T is 89.8%, AL-LUT with 16T is 89.4%, and AL-LUT with 12T is 90.7%. Further, the simulation results show that the energy savings of all of the proposed designs slightly decreases as the supply voltage decreases, but the difference is negligible. Hence, it can be concluded that the energy savings across the voltage range from 1.2 V to 0.7 V is almost consistent.

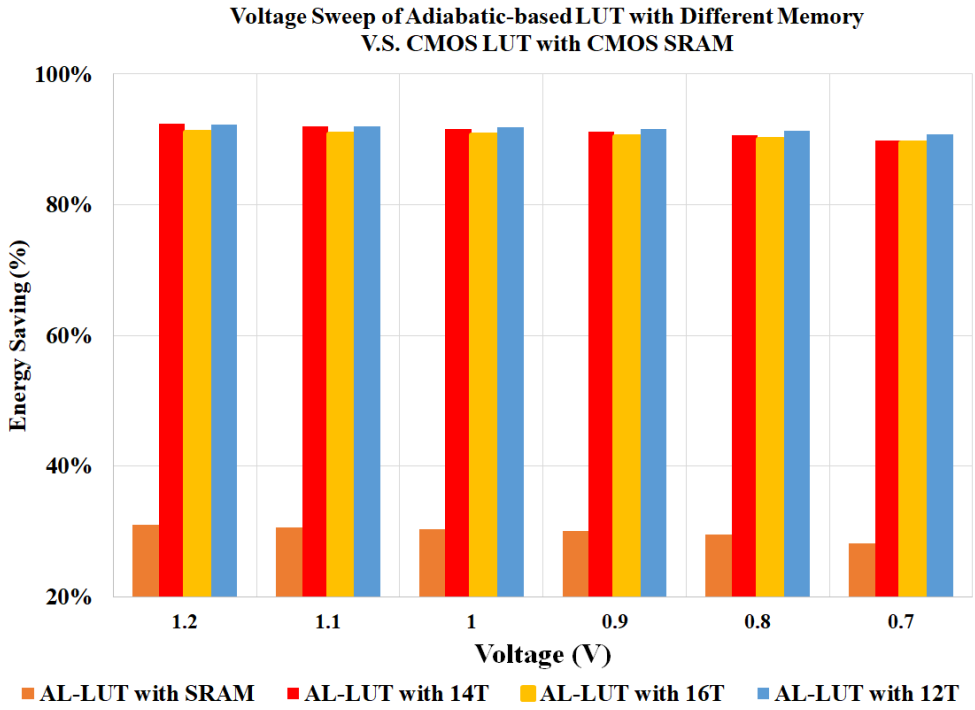

Figure 13. The energy savings of the 16:1 adiabatic-logic-based LUT with different memory designs compared to the CMOS-based LUT with SRAM cells using different supply voltages.

In order to compare the area overhead of the proposed designs and their counterpart, transistor count is used as the metric. Table 6 shows the transistor count of the 16:1 LUT designs. Since adiabatic logic is usually designed in a dual-rail fashion, it has double the transistor count compared to CMOS-based logic, as indicated by the results in Table 6 for LUT designs. On the other hand, the proposed memory cells in this paper have fewer

transistors compared to their counterpart (SRAM cells in FPGAs). Accordingly, the results in Table 6 show that all proposed CLBs in this paper have fewer transistors compared to their CMOS counterpart, and AL-LUT with 16T, 14T, and 12T reduce the transistor count by 19.40%, 21.36%, and 35.32%, respectively.

Table 6. Transistor count of CLB using proposed 16:1 adiabatic-logic-based LUT design with different memories and its CMOS counterpart.

16:1 Look-Up Table					
Design	CMOS LUT [23,26]		Proposed AL-LUT		
Transistor Count	34		68		
16-bit Memory Cell					
Design	SRAM cells in FPGA [24]	16T Memory Cell	14T Memory Cell	12T Memory Cell	
Transistor Count	336	256	224	192	
Configurable Logic Block					
CLB Design	C-LUT with SRAM	AL-LUT with SRAM	AL-LUT with 16T	AL-LUT with 14T	AL-LUT with 12T
Transistor Count	402	468	324	292	260

5. Conclusions

In this article, we utilized adiabatic logic to improve the energy efficiency of a CLB. We proposed a 16:1 adiabatic-logic-based LUT (AL-LUT). The proposed AL-LUT shows significant energy savings compared to its CMOS counterpart. However, the overall energy savings of AL-LUT was significantly reduced when including the energy of the SRAM cell. We explored adiabatic logic and designed a memory cell for further energy savings. Three proposed adiabatic-logic-based memory cells are 14T, 16T, and 12T designs. The proposed memory cells show significant energy savings compared to their CMOS counterparts. Also, the energy savings significantly increase by using the proposed memory cells alongside the AL-LUT compared to the CMOS counterpart and the AL-LUT and SRAM cell. This comparison shows the significant impact of using adiabatic-logic-based memory cells on the energy savings of CLBs. We conducted two case studies with frequency sweep and voltage sweep to investigate the performance of AL-LUT with different memories at different frequencies and supply voltages. Both studies indicate that AL-LUT with the proposed memory cells shows significant energy reduction. Our study concludes that the proposed AL-LUT and memory cell are viable solutions to help FPGAs meet the energy requirements of IoT applications.

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Abbreviations

The following abbreviations are used in this manuscript:

AL-LUT	Adiabatic Logic-based Look-up Table
AL-SA	Adiabatic Logic-based Sense Amplifier
ASICs	Application-Specific Integrated Circuits
CLB	Configurable Logic Block
C-LUT	CMOS LUT
EN	Enable
ECRL	Efficient Charge Recovery Logic
FPGA	Field-Programmable Gate Array
GND	Ground
V_{dd}	Full Voltage Swing
LUT	Look-up Table
IoT	Internet of Things
PC	Power Clock
$PC0$	Power Clock 0
$PC1$	Power Clock 1
PFAL	Positive Feedback Adiabatic Logic
SE	Sense Enable Signal
SE_0	Sense Enable Signal 0
SE_1	Sense Enable Signal 1
SRAM cell	CMOS SRAM in FPGA
V_{pc}	Voltage of the Power Clock
V_{thp}	Threshold Voltage of the PMOS

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