

Elastic integrated electronics based on a stretchable n-type elastomer–semiconductor–elastomer stack

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Elastic integrated electronics are of potential use in a range of emerging applications, particularly those that require devices that can form an interface with soft biological tissue. The development of such devices has typically focused on the creation of stretchy p-type semiconductors, and the lack of suitable stretchy n-type semiconductors limits the potential of stretchable integrated systems. Here we show that a brittle n-type organic semiconductor can be made mechanically stretchable by integrating into a stack with an elastomer–semiconductor–elastomer architecture. The structure suppresses the formation and propagation of microcracks and can be stretched by up to 50% with negligible loss of performance. It also improves the long-term stability of the semiconductor in an ambient environment. We use the n-type elastomer–semiconductor–elastomer stack, together with other stretchy electronic materials, to build elastic transistors, digital logic gates, complementary electronics, p–n photodetectors and an active matrix multiplexed deformable imager.

Fully elastic electronic devices and integrated systems can be used to create human–machine interfaces¹, artificial skins², smart health-care systems³ and implantable biomedical devices⁴. Such technology requires stretchy elastic semiconductors, and the devices typically only use stretchy p-type semiconductors⁵. However, complementary electronics, optoelectronics and p–n junction-based devices (such as diodes, photodetectors and solar cells) also require stretchy n-type semiconductors^{6–9}. The development of stretchy n-type semiconductors is limited by the intrinsic material properties of existing n-type

organic semiconductors, which include poor stability^{10–13} and lower charge transporting efficiency than with their p-type counterparts due to charge trapping by oxygen and moisture^{10,14,15}. Additionally, n-type organic semiconductors are often rigid and there are few strategies for conferring mechanical stretchability to them.

In this Article, we report a stretchable n-type organic semiconductor based on an elastomer–semiconductor–elastomer (ESE) stack structure. Poly[(N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl)-alt-5,5'-(2,2'-bithiophene)]

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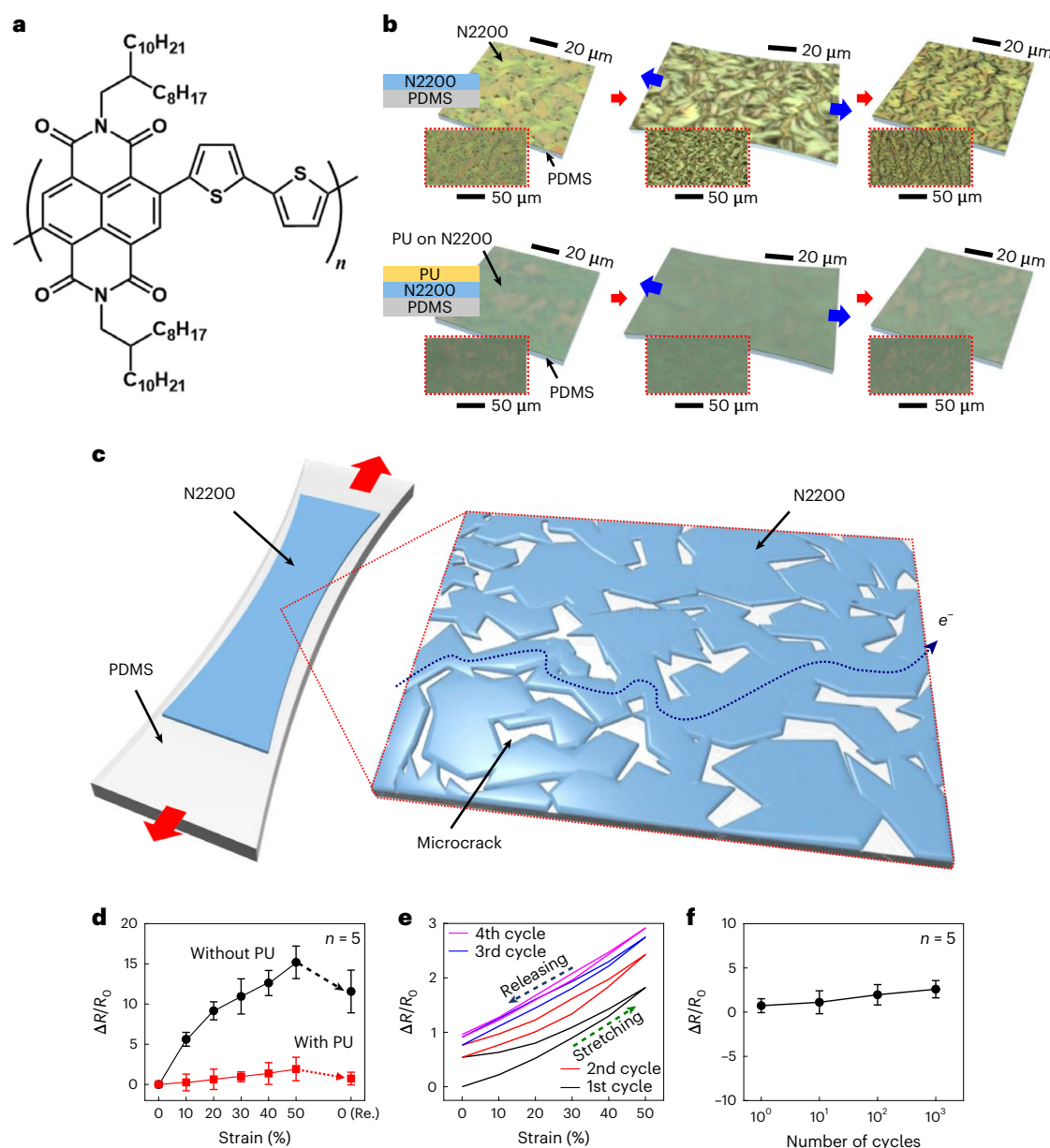


Fig. 1 | Stretchable n-type ESE stack. a, The molecular structure of N2200. **b**, Optical microscope images of N2200 on PDMS (top) and PU-encapsulated N2200 on PDMS (bottom) before and after stretching (tensile strain $\varepsilon = 50\%$) and release ($\varepsilon = 0\%$). **c**, A schematic illustration of microcracked N2200 under mechanical stretching. **d**, The normalized resistance change of N2200 with and

without PU encapsulation depending on the tensile strain. **e**, The normalized resistance change on repetitive stretching and releasing over four cycles. **f**, The normalized resistance change after cyclic stretching at the tensile strain of 50%. Data are presented as mean values ± 1 s.d. on the basis of measurements from five samples.

(P(NDI2OD-T2) or N2200; Fig. 1a) is used as the n-type semiconductor layer, and elastomeric films of polydimethylsiloxane (PDMS) and polyurethane (PU) are used on either side and function as the substrate and gate dielectric, respectively. The stack architecture improves mechanical stretchability and suppresses the formation and propagation of microcracks in the intrinsically brittle N2200 semiconductor, as illustrated through tensile stress tests, charge transport measurements under different strains and in stability tests. We use the n-type semiconductor stack to fabricate stretchy transistors, optoelectronics and integrated electronics, including digital logic gates (NAND and NOR), a pseudocomplementary inverter, a photodetector and an integrated curvature-adjustable imager. The elastic transistors retain high device performance under a tensile strain of 50% along and perpendicular to the channel length direction. The devices also exhibit long-term stable operation for over 100 days in an ambient environment, due

to the elastomer dielectric creating a physical barrier between the semiconductor and the ambient environment.

Stretchable n-type ESE stack

N2200 films on top of PDMS substrates were fabricated by spin coating N2200 solutions in mesitylene (2.5 mg ml^{-1}) at 1,000 r.p.m. for 60 s, followed by baking at 90°C for 1 h in a N_2 environment. Figure 1b (top) shows optical microscope images of PDMS–N2200 films before stretching (that is, 0% strain, left frame), 50% stretching (middle frame) and released to 0% (right frame), demonstrating that the N2200 layer of these films stretched at a strain of 50% exhibits formation of a high number of microcracks; however, the cracked film retains considerable connections as shown schematically in Fig. 1c. This semiconducting network allows charge transport. On coating the PDMS–N2200 film with a thin elastomer PU film, resulting in the ESE semiconductor stack

structure, the number and size of the microcracks in the N2200 central film are significantly reduced (see optical images in Fig. 1b (bottom)). The ESE structure, with the PU encapsulation of the N2200 on a PDMS substrate, results in competing shear stress applied on the N2200 film, that is, on the bottom from the PDMS substrate and the top from the PU encapsulation, which leads to a larger critical crack length of the N2200 film. In addition, the robust adhesive interfaces between the N2200–PDMS and PU–N2200 delocalize any stress concentration, which increases the crack onset strain and prevents crack propagation¹⁶. Thus, the effect of the PU coating, which will function as the gate dielectric for the resulting transistors, greatly improves the elasticity simultaneously.

Additional details of the N2200 film morphologies without and with the PU layer are shown in Supplementary Fig. 1. Moreover, Supplementary Fig. 2 further compares the N2200 films without and with PU after stretching by 50% and releasing to 0%. It is noted that Supplementary Fig. 2b is obtained after removal of PU by immersing the sample in dimethylformamide. The comparison clearly demonstrates that the N2200 layer without PU has a larger density of and larger microcracks compared to that coated with PU. In addition, the electrical property of the PDMS–N2200 and ESE films was investigated. As shown in Fig. 1d, the normalized resistance change ($\Delta R/R_0$) of the N2200 without PU increases substantially by -17 upon stretching to 50% compared with that of the ESE stack (by -3.3). This result further verifies the positive effect of the PU layer on both film elasticity, suppressing crack formation, and charge transport. Figure 1e shows the $\Delta R/R_0$ of the ESE stack under four repeated stretching cycles at a strain up to 50%, demonstrating that after four cycles the resistance does not notably change. There is negligible change in the resistance even after 1,000 cycles (Fig. 1f). These results demonstrate that the ESE structure is a robust elastic n-type semiconductor stack.

Stretchable n-type ESE stack-based transistors

Figure 2a shows a schematic illustration in an exploded view of a stretchable n-type organic transistor consisting of the ESE stack, silver nanowires in PDMS (AgNWs–PDMS) as source–drain contacts and a eutectic liquid metal alloy of gallium–indium (liquid-metal) gate electrode. The transistor fabrication process involves the preparation of AgNW–PDMS-based source and drain electrodes, as described in Methods. Then, the N2200 solution in mesitylene was patterned on the channel region of the AgNW–PDMS electrodes by spin coating with a shadow mask. The PU gate dielectric was also deposited by spin coating on top of the N2200 film, creating the ESE stack structure. Finally, the liquid-metal gate was patterned by doctor blading with a shadow mask. The details of the layer thickness, channel geometry and fabrication process are reported in Methods. Among several parameters affecting the field-effect mobility (μ_{FE}) of these devices, the thickness of the organic semiconductor plays an important role due to several factors, including effective thickness of the channel with charge accumulation, vertical resistance of the channel and charge trapping density in the bulk^{17–19}. In this study, we optimized device performance by investigating different N2200 thicknesses of 7, 30, 60, 130 and 280 nm by spin coating semiconductor solution concentrations of 0.1, 0.5, 1.0, 2.5 and 5.0 mg ml⁻¹, respectively. The optimal thickness, after optimization (Supplementary Fig. 3) is -130 nm.

A stretchable n-type transistor array (5 × 5) (Fig. 2b) was next fabricated using a solution process as described in Methods. Figure 2c shows optical images of the array without and with a tensile strain of 50% along (top) and perpendicular to (bottom) the channel length directions. A 25-transistor array shows reliable transfer characteristics with a yield of 100%. As shown in Fig. 2d,e and Supplementary Fig. 4, the device threshold voltage (V_{TH}) and μ_{FE} are 1.93 ± 0.55 V and 0.24 ± 0.07 cm² V⁻¹ s⁻¹, respectively, with the highest μ_{FE} value 0.44 cm² V⁻¹ s⁻¹. The error is determined on the basis of the s.d. These values are comparable to the μ_{FE} of N2200 transistors based on conventional rigid substrates^{20–22}.

Both μ_{FE} and V_{TH} were obtained from the (drain current (I_{DS}))^{1/2} versus gate voltage (V_{GS}) curve using the specific capacitance of the PU gate dielectric of 13.494 pF mm⁻² at the frequency of 1 kHz (Supplementary Note 1). The representative output and transfer curves are shown in Fig. 2f,g, respectively. In addition, these devices exhibit stable electrical response under operation (drain voltage = $V_{DS} = 30$ V) for 3,000 s, and excellent long-term stability in an ambient condition for 113 days, as shown in Supplementary Figs. 5 and 6, respectively.

The stretchability of the n-type transistors was evaluated by measuring the transistor's electrical performance under different tensile strains. Figure 2h shows the transfer curves of the stretchable transistors under tensile strains of 0%, 10%, 30%, 50% and 0% (released) along the channel length direction, which indicate that the device retains its performance under stretching. The μ_{FE} decreases from 0.22 ± 0.15 cm² V⁻¹ s⁻¹ to 0.12 ± 0.09 cm² V⁻¹ s⁻¹, then recovers to 0.14 ± 0.09 cm² V⁻¹ s⁻¹ on releasing the strain to 0%, as shown in Fig. 2i. It is noted that the calculated μ_{FE} was obtained by accounting for the channel geometry deformation and capacitance changes (Supplementary Fig. 7). In addition, the ON current (I_{ON}) and OFF current (I_{OFF}) changed from $(5.22 \pm 1.49) \times 10^{-7}$ A to $(1.95 \pm 0.76) \times 10^{-7}$ A and from $(2.05 \pm 0.78) \times 10^{-9}$ A to $(1.62 \pm 0.59) \times 10^{-9}$ A, respectively. I_{ON} and I_{OFF} recovered to $(3.22 \pm 1.15) \times 10^{-7}$ A and $(1.86 \pm 0.67) \times 10^{-9}$ A, respectively, on releasing the applied strain. Moreover, V_{TH} and I_{ON}/I_{OFF} also show a negligible decrease (Supplementary Fig. 8). It is noted that I_{ON} and I_{OFF} were obtained at a drain voltage of 30 V while applying a V_{GS} of 30 V and 0 V, respectively. For practical applications, mechanical robustness is critical. Therefore, the fabricated stretchable transistors were electrically characterized for 1,000 cycles of up to 50% strain, exhibiting negligible performance degradation, as shown in Fig. 2j and Supplementary Fig. 9. A similar trend was observed under tensile strain applied perpendicular to the channel length direction (Fig. 2k–m and Supplementary Figs. 10 and 11). These results show that the stretchable ESE stack structure enables n-type transistors with excellent mechanical endurance while the electrical properties are comparable to those of N2200 transistors on conventional rigid substrates.

Stretchable logic gates based on n-type organic transistors

Stretchable logic gates are basic building blocks for stretchy digital integrated electronics and have the potential to perform logical functions through binary inputs and outputs. Based on the stretchable n-type organic transistors, stretchable logic gates, including pseudocomplementary inverter, NAND and NOR gates, are demonstrated. Figure 3a,b shows a schematic illustration and circuit diagram, respectively, of a stretchable pseudocomplementary inverter. The fabricated inverter (Fig. 3c) was reliably stretched as shown in Fig. 3d and Supplementary Fig. 12. The electrical properties were tested by measuring the output voltage (V_{OUT}) while the input voltage (V_{IN}) was swept from 0 to 30 V with a constant source voltage (V_{SS}) and drain voltage (V_{DD}) of 40 V and 30 V, respectively. The voltage transfer curves (VTCs) of the stretchable inverter under tensile strains of 0%, 10%, 30%, 50% and back to 0% (released), both along and perpendicular to the channel length direction, are shown in Fig. 3e,f, and exhibit typical logic operation (Fig. 3g) in the range of input (0 and 1) and output logic state (1 and 0). It is noted that, when the devices are stretched, they show negligible shift of the voltage gain and switching threshold voltage (V_M), as shown in Fig. 3h. This result demonstrates that this device is suitable for logic operations due to a clear distinction of the logic values and can be further optimized.

A stretchable NAND gate was built from six stretchable n-type organic transistors, as shown in Fig. 3i–l and Supplementary Fig. 13. The logic operation was tested by measuring V_{OUT} with a square waveform of 0 V (logic state 0) and 30 V (logic state 1) applied to the input voltages ($V_{IN,A}$ and $V_{IN,B}$). Under tensile strain of 0% (Fig. 3m) and 50% along (Fig. 3n) and perpendicular to (Fig. 3o) the channel

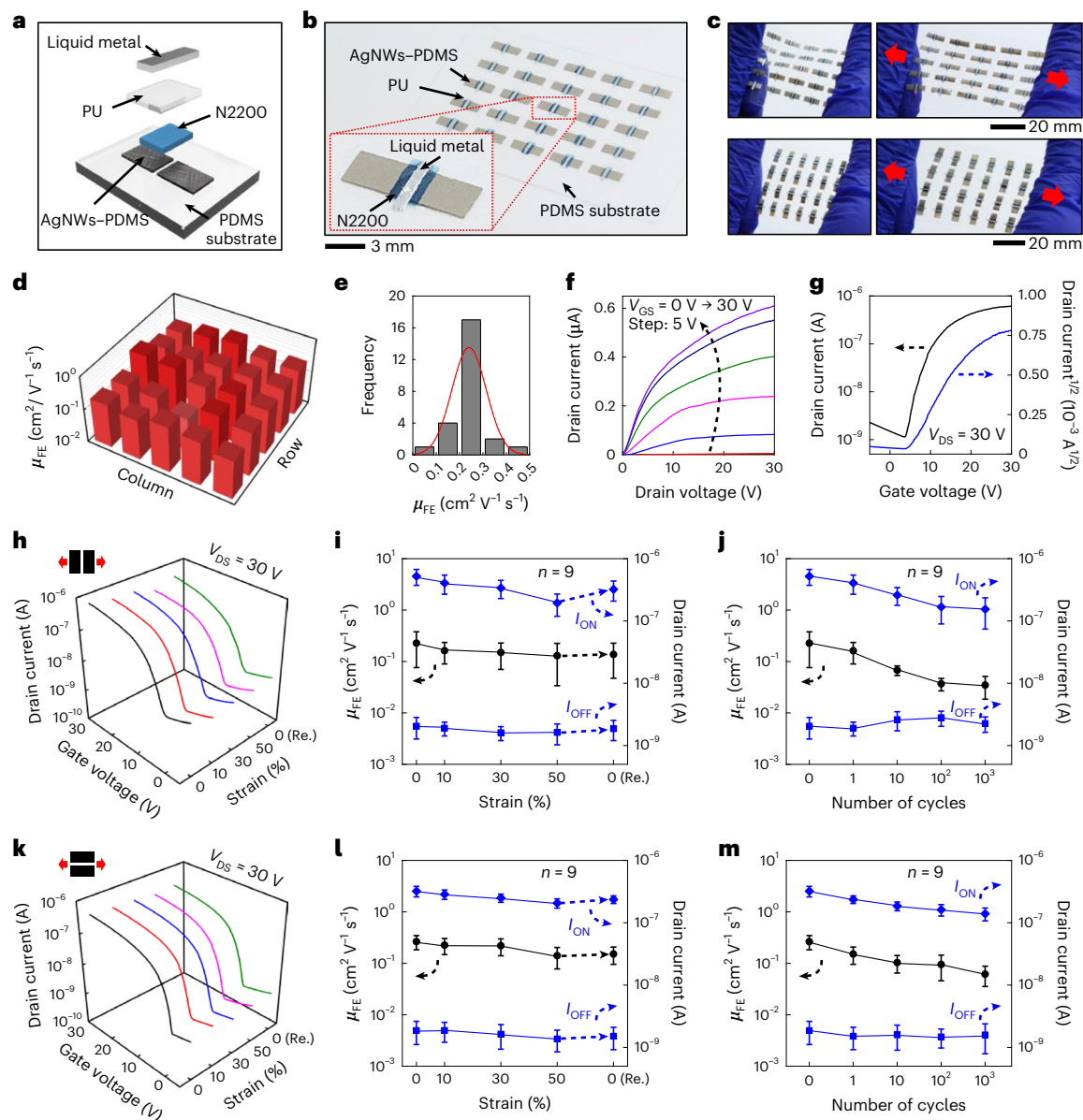


Fig. 2 | Stretchable n-type organic transistor array. **a**, A schematic exploded view of the stretchable n-type ESE based transistor. **b**, An optical microscope image of the stretchable n-type organic transistor array. The inset is a microscopic image of a single transistor from the array. **c**, Optical images of the array under tensile strain both along and perpendicular to the channel length direction. **d**, The calculated μ_{FE} map of the transistor array. **e**, The statistical distribution of the μ_{FE} in the array. **f**, Representative output characteristics of the stretchable n-type organic transistor. **g**, Representative transfer characteristics of the stretchable n-type organic transistor. **h**, Transfer characteristics of the

stretchable n-type organic transistor under tensile strain along the channel length direction. **i, j**, The μ_{FE} and drain current depending on the strain (**i**) and the number of cyclic stretchings at 50% strain (**j**) along the channel length direction. **k**, Transfer characteristics of the stretchable n-type organic transistor under tensile strain perpendicular to the channel length direction. **l, m**, The μ_{FE} and drain current depending on the strain (**l**) and the number of cyclic stretchings at 50% strain (**m**) perpendicular to the channel length direction. Data are presented as mean values ± 1 s.d. on the basis of measurements from nine devices.

length direction, the stretchable NAND showed normal logic operation (Fig. 3p) without notable performance change, which presents logic state 0 only when both inputs are logic state 1.

Figure 3q–s shows a schematic illustration, circuit diagram and optical image of a stretchable NOR gate, which also consists of six n-type transistors. As shown in Fig. 3t and Supplementary Fig. 14, the NOR gate also exhibits excellent stretchability without any substantial performance degradation or any physical damage. In terms of electrical properties of the stretchable NOR gate, normal logic operations were obtained under tensile strains of 0% and 50% both along and perpendicular to the channel length direction (Fig. 3u–w). Figure 3x reports

the summarized truth table of the NOR gate. These results suggest that it is possible to use the stretchable logic gates based on n-type organic transistors in circuits that must be stretched without compromising their logic functions.

Fully stretchable complementary inverters

Complementary inverters using p-type and n-type transistors offer several advantages, such as low power consumption, high gain and dense integration, compared with those based on unipolar transistors^{23–26}. In this study, stretchable complementary inverters were constructed by using the N2200-based ESE stack and semiconducting single-walled

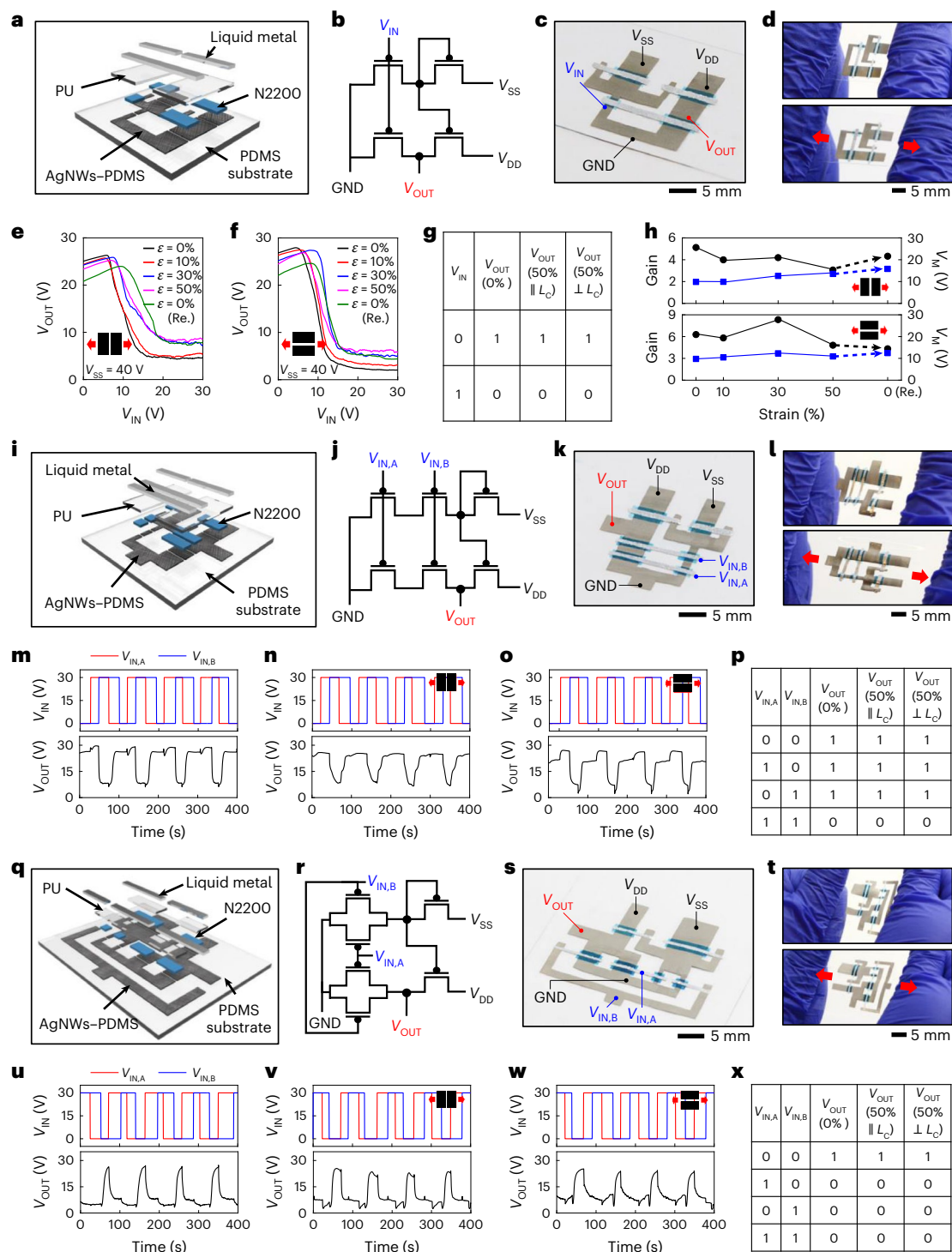


Fig. 3 | Stretchable logic gates based on n-type organic transistor. **a–c**, The schematic exploded view (**a**), circuit diagram (**b**) and optical image (**c**) of the stretchable pseudocomplementary inverter. **d**, Images of the device under tensile strain along the channel length direction. **e, f**, VTC of the stretchable inverter under tensile strains of 0, 10, 30, 50 and 0% (released) along (**e**) and perpendicular to (**f**) the channel length direction. **g**, Truth tables for the stretchable inverter. **h**, Voltage gain and V_M of the stretchable inverter under tensile strains of 0, 10, 30, 50 and 0% (released) along and perpendicular to the channel length direction. **i–k**, Schematic exploded view (**i**), circuit diagram (**j**) and optical image (**k**) of the stretchable NAND gate. **l**, Optical images of the

device under the tensile strain along the channel length directions. **m–o**, The output characteristic of the stretchable NAND gate without tensile strain (**m**) and under tensile strain of 50% along (**n**) and perpendicular to (**o**) the channel length direction. **p**, Truth tables for the stretchable NAND gate. **q–s**, Schematic exploded view (**q**), circuit diagram (**r**) and optical image (**s**) of the stretchable NOR gate. **t**, Images of the device under tensile strain along the channel length direction. **u–w**, The output characteristic of the stretchable NOR gate without tensile strain (**u**) and under tensile strain of 50% along (**v**) and perpendicular to (**w**) the channel length direction. **x**, Truth tables for the stretchable NOR gate.

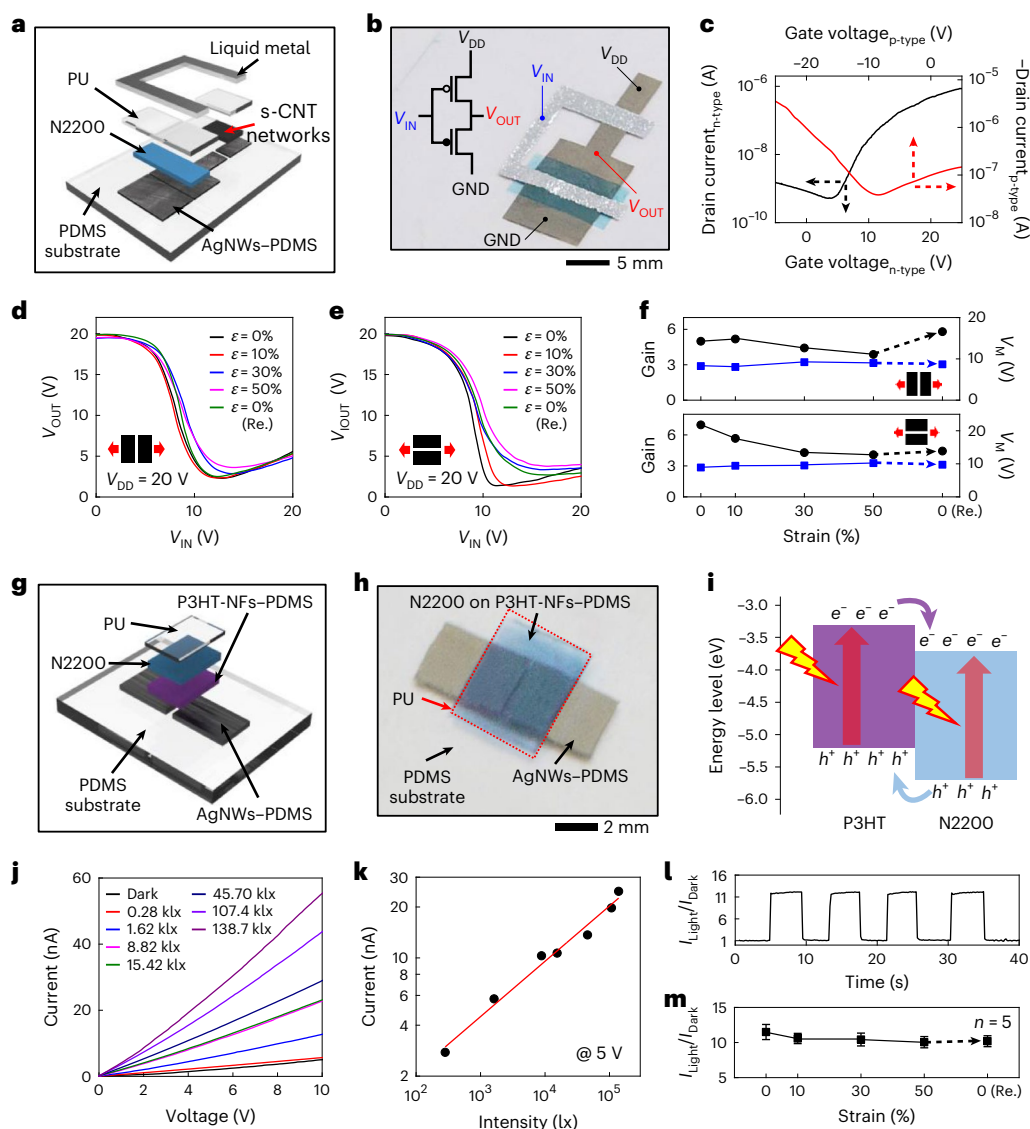


Fig. 4 | Stretchable complementary inverter and bilayer photodetector.

a,b, A schematic exploded view (**a**) and optical image (**b**) of the stretchable complementary inverter. Inset of **b**: circuit diagram of the complementary inverter. **c**, Transfer characteristics of both n-type and p-type transistors in the complementary inverter. **d,e**, VTCs of the stretchable complementary inverter under the tensile strains of 0, 10, 30, 50 and 0% (released) along (**d**) and perpendicular to (**e**) the channel length direction. **f**, Voltage gain and V_M of the stretchable complementary inverter under the tensile strains of 0, 10, 30, 50 and 0% (released) along and perpendicular to the channel length direction.

g,h, A schematic exploded view (**g**) and optical image (**h**) of the stretchable bilayer photodetector. **i**, The energy band diagram of the photodetector. **j**, The obtained current of the photodetector under different light intensities. **k**, The calibration curve of the stretchable photodetector. **l**, The dynamic photoresponse characteristic at 5 V under cycles turning ON and OFF light with an intensity of 138.7 klx. **m**, The calculated ratio of photocurrent and dark current depending on the tensile strain. Data are presented as mean values ± 1 s.d. based on measurements from five devices.

carbon nanotube (s-CNT) networks for n-type and p-type transistor operation, respectively. In particular, the electrical characteristics of the transistor based on s-CNT networks (that is, the p-type transistor) were investigated, as shown in Supplementary Fig. 15. The p-type transistor retains substantial electrical performance ($V_{TH} = -8.9$ to -7.245 V, $\mu_{FE} = 4.7$ – 2.99 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$) under tensile strains of 0%, 10%, 30%, 50% and back to 0% (released), both along and perpendicular to the channel length direction (Supplementary Fig. 16). On the basis of the performance of these transistors, for complementary device fabrication their channel widths/lengths were determined to be 6,000/100 μm (n-type transistor) and 2,000/300 μm (p-type transistor). Figure 4a,b shows a schematic illustration and optical image of the stretchable complementary inverter. The detailed fabrication processes are described in Methods. As shown in Fig. 4b, the gate electrodes of both type of transistor are connected with a liquid metal electrode to form the input

node. The connected area between the source of the p-type transistor and the drain of the n-type transistor serves as the output node. The transfer characteristics of the individual transistor in the complementary inverter are shown in Fig. 4c. To investigate the electrical properties of the stretchable complementary inverter, the V_{IN} was swept from 0 to 20 V with a constant V_{DD} of 20 V. No damage under mechanical deformations (Supplementary Fig. 17) was observed. The VTCs of the stretchable complementary inverter under tensile strains of 0%, 10%, 30%, 50% and back to 0% (released) both along and perpendicular to the channel length direction are shown in Fig. 4d,e, which shows stable logic operation. It is noted that the complementary inverter shows better performance compared with a traditional zero- V_{GS} inverter constructed with only the n-type of transistor, as shown in Supplementary Fig. 18. Figure 4f shows the moderate change of the gain and V_M of the complementary inverter during a stretching and releasing cycle.

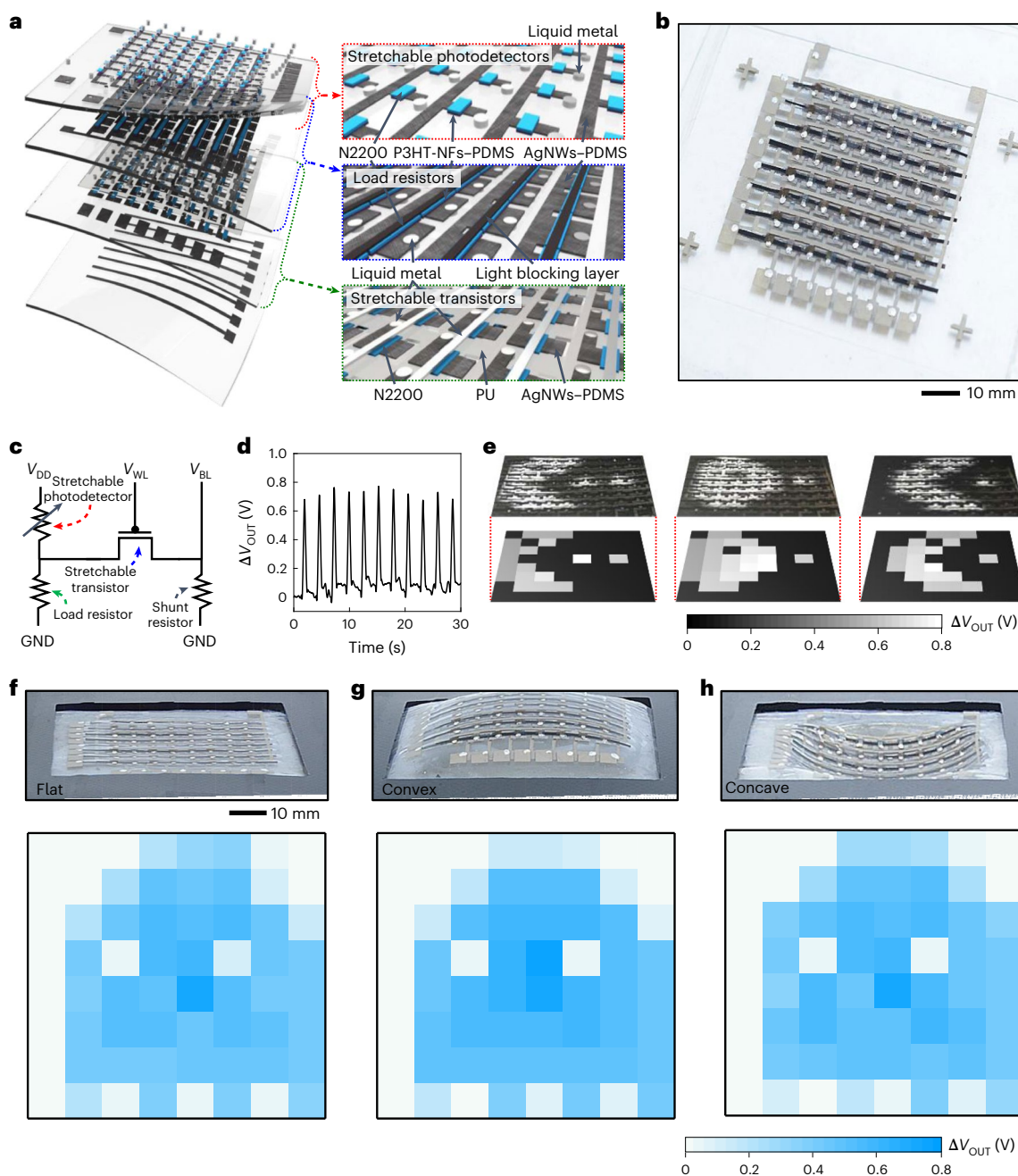


Fig. 5 | Curvature-adjustable imager. **a, b**, A schematic exploded view (**a**) and optical image (**b**) of the curvature-adjustable imager. **c**, The circuit diagram of a single sensing pixel. **d**, Dynamic photoresponse of the single sensing pixel. **e**, The obtained voltage mapping results (lower row) on the basis of light

projection to the imager (upper row) through different photomasks. **f–h**, Optical images (upper row) and maps (lower row) of the ΔV_{OUT} of the imager under different mechanical deformation conditions: flat (**f**), convex (**g**) and concave (**h**).

Stretchable photodetectors

A photodetector is an essential and basic optoelectronic device²⁷, with the planar architecture having attracted attention due to easy fabrication and facile integration of the detector with the circuit^{28–30}. Although inorganic materials (such as one- or two-dimensional materials or perovskites) are commonly used in this type of photodetector as the light-sensing layer³¹, organic semiconducting materials have several advantages, including easy manufacturing process, facile modulation of light absorption properties, light weight and low cost³². However, the strong binding energy of photogenerated excitons in organic semiconductors hinders exciton separation to free carriers, thus both p-type (donor) and n-type (acceptor) materials are required to

ensure enough potential bias for charge dissociation^{30,32–34}. Therefore, in this work fully stretchable bilayer photodetectors were designed and constructed using the n-type ESE stack and poly(3-hexylthiophene) (P3HT) nanofibrils in PDMS (P3HT-NFs-PDMS) as n-type and p-type semiconductors, respectively. It is noted that the P3HT-NFs-PDMS has rubber-like mechanical properties, as reported previously^{35–37}. Figure 4g,h shows a schematic illustration and optical image, respectively, of the fully stretchable photodetector. The detailed fabrication process is described in Methods. Figure 4i reports the energy band diagram of P3HT and N2200 in the photodetector. Upon illumination of the semiconductor layer, electrons in both P3HT and N2200 are excited from the highest occupied molecular orbitals to the lowest unoccupied

molecular orbitals if the photon energy is higher than their band gaps, which generates excitons. The excitons at the interface between P3HT and N2200 are readily dissociated due to the internal potential created by the different band energies of the p-type and n-type semiconductors, thus the photocurrent can be enhanced when compared with devices with only a single type of semiconductor as the active layer^{32,38}. Supplementary Fig. 19 shows the dynamic photoresponse of these devices depending on concentration of P3HT (0, 0.5, 1.0, 1.5 and 2.5 mg ml⁻¹) and constant concentration of N2200 (2.5 mg ml⁻¹) to optimize the device performance. The results suggest that the optimized concentration of P3HT is 1.0 mg ml⁻¹. The optimal thicknesses of P3HT and N2200 are ~120 and 130 nm, respectively. As expected, the p–n junction enhances the photoresponse property when compared with the performance of the devices based on only P3HT-NFs or only N2200. Figure 4j shows the photocurrent at different applied voltages under light intensities varying from 0 to 138.7 klx. The photo-to-dark-current ratio under a light intensity of 138.7 klx and a voltage of 5 V is 12.56, with photo- and dark currents of 2.475×10^{-8} A and 1.970×10^{-9} A, respectively. The calibration curve for this device is shown in Fig. 4k, which shows a typical linear response of photocurrent with light intensity. The dynamic photocurrent response under ON and OFF cycling of light with an intensity of 138.7 klx and voltage of 5 V is shown in Fig. 4l. Supplementary Fig. 20 shows the optical images of the photodetector without and with a mechanical deformation. When the device was stretched at strains of 0%, 10%, 30%, 50% and back to 0% (released), the photo-to-dark-current ratio showed no substantial change, as illustrated in Fig. 4m and Supplementary Fig. 21. These results indicate that the stretchable photodetector holds potential for various optoelectronic devices, such as a deformable imager described in the following section.

Curvature-adjustable imager devices

A focal plane array imager with a curved geometry is crucial to alleviate image distortion induced by, for example, the Petzval surface and enhanced wide-angle field of view^{39–42}. In addition, it is highly desirable to have imagers with tunable curvatures to match with adjustable lenses and/or optics with different Petzval surfaces or fields of view in many applications. We further demonstrated a curvature-adjustable imager in a multiplexed array, all based on stretchable electronics and optoelectronic devices, including the transistor, resistor and photodetector as switching element, load and light sensor. Figure 5a schematically illustrates the exploded view of the curvature-adjustable imager. Specifically, the imager consists of four different layers, including a sensor array, load resistor array, switching transistor array and electrode array, which are connected vertically through via holes using a liquid metal. These devices were fabricated following the same procedures as reported in the previous sections. The load resistor is prepared by using the same materials and structure as used in the photodetector but with different dimensions and an additional light-blocking layer for efficient voltage dividing depending on the incident light. The detailed fabrication processes are schematically illustrated in Supplementary Figs. 22–25 and described in Methods. The fabricated curvature-adjustable imager is shown in Fig. 5b. The gate electrodes of each row were connected to a word line (V_{WL}), and the source electrodes of each column were connected to a bit line (V_{BL}). The drain electrodes of each transistor were supplied with the voltage obtained from the voltage divider circuit, which was composed of a stretchable photodetector and a load resistor. Figure 5c and Supplementary Fig. 26 show the circuit diagram of an individual sensing pixel and the 8×8 array, respectively. Figure 5d shows the output voltage change (ΔV_{OUT}) under a cyclic pulse with a duration of 500 ms and a period of ~3 s at V_{DD} and V_{WL} of 10 V. The absolute voltage output results of the single sensing pixel of the imager corresponding to light projection are shown in Supplementary Fig. 27. These data demonstrate the respectable light-sensing properties of this circuit. The voltage mapping results (lower row) on the basis of light projection to the imager (upper row)

through three different shaped photomasks (left, middle and right) are shown in Fig. 5e. It is noted that the ΔV_{OUT} mapping to display light sensing was obtained with a data acquisition system (National Instruments) and the detailed interfaces with the data acquisition system are described in Supplementary Note 2. The curvature-adjustable imager could be deformed by using a custom-made pneumatic chamber, as shown in Supplementary Fig. 28. Figure 5f–h shows the resulting voltage map of ΔV_{OUT} under different mechanical deformation conditions: flat, convex and concave. The upper images in each subfigure are optical images of the imager, and the lower images show the corresponding map of ΔV_{OUT} . The agreement of the imaging results under different deformation conditions demonstrates the potential of this device for various imaging technologies.

Conclusions

We have reported a stretchable ESE stack structure that is composed of PDMS, an n-type organic semiconductor N2200 and PU. The structure reduces the formation and propagation of cracks within the brittle N2200 film under mechanical deformations and enhances its long-term stability in ambient environments. This strategy could also be applied to other classes of brittle materials including non-organics. The n-type stack is used to create stretchable transistors, optoelectronics and logic gates, which exhibit robust operation up to 50% strain. We also demonstrated multicomponent integration of our ESE stack and other stretchy components by creating a deformable active multiplexed arrayed imager based on all-stretchable materials. In contrast to their rigid counterparts, the stretchable n-type ESE stack could potentially be used to make integrated electronics in a fully stretchable format and without using dedicated architectures to enable structural stretchability^{43–46}. Stretchy n-type semiconductors created with our ESE stack method could be of use in the development of bioelectronics, wearables, soft robotics and large-scale integrated circuits.

Methods

Materials

N2200 (weight-averaged molecular mass $M_w = 79$ kDa, polydispersity index PDI = 2.6) was obtained from Flexterra and used without any further purification. P3HT (regioregular, $M_w = 50,000$ – $100,000$), PU (Selectophore grade), liquid metal (gallium–indium eutectic, $\geq 99.99\%$), mesitylene (98%), tetrahydrofuran (anhydrous, $\geq 99.99\%$), 1,2-dichloromethane (anhydrous, $\geq 99.8\%$), gold (III) chloride trihydrate ($\text{HAuCl}_4 \cdot 3\text{H}_2\text{O}$, $\geq 99.9\%$, trace metals basis) and ammonia (NH_4OH , anhydrous, 28%) were purchased from Sigma-Aldrich and used as received. PDMS (Sylgard 184 silicone elastomer kit) and AgNW solution (AWO90, diameter range 75–105 nm, length range 15–45 μm , purity 99.96%, 10 mg ml⁻¹) were from Dow Corning and Zhejiang Kechuang Advanced Materials, respectively. s-CNT solution (IsoNanotubes-S, single walled, mean diameter 1.4 nm, mean length ~0.5 μm , purity 98%) was from NanoIntegris Technologies and used without any further purification or dilution.

Preparation of stretchable AgNW–PDMS electrodes

The AgNW–PDMS composite electrodes were prepared starting with patterning AgNWs on a clean glass substrate through drop casting of the solution with a Kapton film-based shadow mask that was prepared by a programmable cutting machine (Silhouette Cameo), followed by baking at 60 °C for 10 min, then 200 °C for 30 min for thermal welding between the wires for enhanced electrical conductivity. The patterned AgNWs were coated with PDMS solution (10:1 weight ratio of base and curing agent) by spin casting at 300 r.p.m. for 60 s, then cured at 60 °C for 4 h to fully solidify the PDMS. The partially embedded AgNWs in the PDMS were obtained due to the porous structured AgNW network through permeation of solution state PDMS into the network. Finally, the AgNW–PDMS composite electrode was completed by peeling the solidified PDMS off the glass substrate.

Fabrication of stretchable n-type transistors, pseudocomplementary inverter and NAND and NOR gates

The fabrication of the stretchable n-type transistor based on the N2200 semiconductor started with the preparation of the N2200 solution in mesitylene. The solution was spin coated at 1,000 r.p.m. for 60 s on the AgNW–PDMS composite-based stretchable electrodes with a Kapton film-based shadow mask to form the patterned channel, followed by annealing at 150 °C for 1 h under N₂ atmosphere. To form the encapsulation top gate dielectric, PU solution (75 mg ml⁻¹) in tetrahydrofuran (prepared by dissolving at 80 °C for 2 h) was spin coated on top of the channel at 1,000 r.p.m. for 60 s, then the sample was annealed at 100 °C for 1 h. Afterwards, a piece of Kapton film as the mask was placed on the PU, followed by removing exposed PU using tetrahydrofuran. Thereafter, the liquid metal gate electrode was formed on top using the doctor-blading process.

Fabrication of stretchable complementary inverters

The complementary inverter was constructed with N2200 and s-CNT networks as n-type and p-type semiconductors, respectively. First, stretchable electrodes based on the AgNW–PDMS composite conductor were prepared using the previously described process. To minimize the energy barrier between s-CNT networks and the AgNW–PDMS electrode, an AuNP coating on the exposed AgNWs was formed using a galvanic exchange process with HAuCl₄·3H₂O. The HAuCl₄·3H₂O solution (0.5 mM) was dropped onto the p-channel region of the AgNWs–PDMS, followed by rinsing using deionized water after 2 min, which allows Ag–Au galvanic replacement. Thereafter, the byproduct of AgCl was removed using NH₄OH solution (28%), then the sample was dried on a hotplate at 90 °C for 1 h. To form a p-channel, the s-CNT solution (10 µl) was dropped on the channel region through a Kapton film-based shadow mask, then baked at 90 °C for 30 min. The formed s-CNT networks were rinsed with deionized water to remove surfactant and fully dehydrated in a vacuum oven at 90 °C for 1 h. Afterwards, the patterned n-channel was formed out of N2200 with a shadow mask, then PU gate dielectrics and gate electrode were formed successively through the abovementioned procedure to complete the device fabrication.

Fabrication of stretchable photodetectors

The fabrication of the stretchable photodetector involved the preparation of AgNW–PDMS composite-based stretchable electrodes as the first step. To prepare stretchable p-type semiconductor, 2 mg ml⁻¹ P3HT solution was prepared by dissolving P3HT in dichloromethane, followed by sequentially heating at 60 °C to form a homogeneous solution, and then cooling the solution to form P3HT-NF, and finally mixing with PDMS solution in dichloromethane (10:1 weight ratio of base and curing agent) to form P3HT-NF–PDMS at the weight ratio of 2:8 (ref. 47). The prepared P3HT-NF–PDMS solution is spin coated on the AgNW–PDMS electrode through a Kapton film-based shadow mask at 2,000 r.p.m. for 60 s, then baked at 100 °C for 1 h. Thereafter, N2200 was coated on top of P3HT-NFs–PDMS through the abovementioned process in a N₂ environment. To form an ESE structure, PU solution was coated on top of N2200 by spin coating at 3,000 r.p.m. for 60 s, then the derived stretchable photodetector was annealed at 100 °C for 1 h.

Fabrication of curvature-adjustable imagers

The fabrication of the curvature-adjustable imager enabled by fully stretchable materials and devices began with the preparation of a stretchable electrode array based on AgNW–PDMS composite, as shown in Supplementary Fig. 22. To prepare a layer with a stretchable transistor array, N2200 was patterned on another AgNW–PDMS array as described above, followed by forming punched via holes for interconnection between layers. The layer with the transistor array was assembled with the prepared electrode array by heating at 90 °C for 1 h after UV–O₃ treatment, which allows strong covalent bonding between PDMS layers. Thereafter, the liquid metal was injected into

the via holes to form the interconnection between two layers. PU for the gate dielectric was patterned using a shadow mask, then liquid metal was patterned using the doctor-blading process. The detailed process is schematically shown in Supplementary Fig. 23. The layer with the stretchable load resistor array is followed by the photodetector fabrication procedure, as described above and Supplementary Fig. 24. The via holes were formed again for vertical interconnects. A rubbery light-blocking layer was formed based on a mixture of PDMS precursor (10:1 weight ratio of base and curing agent) with black powder (thermochromic black dye, LCR Hallcrest) at the ratio of 2:1, followed by spin coating on a glass substrate at 1,000 r.p.m. for 40 s, then fully solidified at 95 °C for 1 h. The solidified, rubbery light-blocking layer was cut into shape and laminated on top of the photodetector to fully cover the channel region to prevent light illumination, which allows the device to become a load resistor. The prepared stretchable load resistor array was carefully aligned, stacked on the prepared transistor array and assembled using the abovementioned process. The last layer was prepared by fabricating a stretchable photodetector array using N2200 and P3HT-NF/PDMS through a Kapton film-based shadow mask as described previously. It is noted that the channel dimensions (width/length) of the photodetector and load resistor are 1,000 µm/120 µm and 4,000 µm/50 µm, respectively. Finally, the imager was assembled with the load resistor and transistor array layer, followed by injection of liquid metal into the via holes to complete the device construction (Supplementary Fig. 25).

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

K.S. and C.Y. conceived and designed the experiment. K.S., H.S., Y.Z., S.P. and S.J. performed the experiments. K.S., H.S. and Y.Z. characterized device performance. K.S., H.S. and Y.Z. analysed the experimental data. B.W., T.J.M. and A.F. provided materials and advised on the experiment. H.S., K.S. and C.Y. wrote the paper.

Competing interests

The authors declare no competing interests.

Additional information

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