A Multi-Branch Receiver With Modulated Mixer Clocks for Concurrent Dual-Carrier Reception and Rapid Compressive-Sampling Spectrum Scanning

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***Abstract*— A multi-branch receiver is introduced that uses mixer-clock modulation to unify the functions of single-carrier and concurrent dual-carrier reception, as well as compressive-sampling spectrum scanning into a single architecture. With CW-modulated mixer clocks, the receiver achieves concurrent reception from two distinct bands and realizes tuned impedance matching that greatly improves its out-of-band (OB) linearity. With pseudo-noise (PN)-modulated mixer clocks, the receiver supports rapid spectrum scanning. Disabling modulation reverts the receiver to a single-carrier receiver with good OB linearity. A 65-nm CMOS prototype is presented that offers 2.7-dB minimum NF, −1.3-dBm B1dB, and +8-dBm IIP3 for high-sensitivity single-carrier reception. Concurrent dual-carrier reception at 500 and 900 MHz is demonstrated that offers −8.4-dBm B1dB and sub-6-dB NF. In the CS spectrum scanning mode, the receiver achieves a 66-dB dynamic range with −75-dBm sensitivity over a 630-MHz RF span and consumes 18.7 nJ per detected signal.**

***Index Terms*— Carrier aggregation, clock modulation, compressive sampling, concurrent tuned matching, multi-branch, noise cancelling, spectrum scanning, wireless scanning, wireless sensing.**

I. Introduction

MIXERS are deployed in receivers for shifting signals from one frequency range to another, known as heterodyning, for further signal processing. Different mixer topologies typically rely on either non-linear or time-varying characteristics [1]. Most of the state-of-the-art (SoA) software-defined radio (SDR) receivers are realized with LNTAs and passive current-mode mixers to avoid voltage gain in the front end for better linearity [2]–[5]. The mixers inside these receivers are driven by clock waveforms derived from a single continuous-wave (CW) source. In compressive-sampling (CS) receivers for spectrum scanning [6], [7], the concept of clock modulation has been introduced [8], where pseudo-random bit sequences (PRBSs) are used to modulate the single-frequency clocks.

In this article, we explore several unique functions that can be achieved when the clocks of a mixer-first receiver are modulated [9], including concurrent tuned matching at two different bands and concurrent reception from two distinct RF carriers, while doing noise cancellation across these two carriers. These features can possibly help to address some of the challenges posed by carrier-aggregation (CA) technology, which requires concurrent reception from multiple RF carriers from either the same band (intra-band) or different bands (inter-band) across the spectrum [10]. Intra-band CA occurs within tens of MHz in a single band and has been demonstrated with two-step down-conversion [11], complex signal processing [12], and digitally assisted down-conversion [13] architectures. It does not require substantial changes in the receiver RF front-end architectures nor their front-end module (FEM) design. Inter-band CA occurs across hundreds of MHz in different bands and poses significant challenges to both the receiver RF front-end architectures and their FEM design in terms of RF filtering and interface [10], [14]–[16].

Traditional frequency-translational noise-canceling (FTNC) receivers [2], [3] receive the I/Q components from one carrier at a time. They present the matched impedance at the signal band of interest and a low impedance out-of-band (OB). While this is beneficial to obtain good OB linearity, it is impractical to connect multiple FTNC receivers in parallel for concurrent reception. Conventional inter-band CA solutions split the RF carriers from different bands into independent signal branches with diplexers, antenna switches, and dedicated filter banks [16]. However, this approach does not scale well as the number of aggregation band combinations increases. Another approach is to convert the RF signals from voltage to current and then split the current into separate signal branches [12]. By using multiple frequency-translation feedback loops, the receiver is impedance matched to the antenna at multiple frequencies. The complex signal processing limits its concurrent reception capabilities within tens of MHz (i.e., intra-band CA). A frequency-translational quadrature-hybrid (FTQH) receiver [17] aggregates two or more inter-band RF

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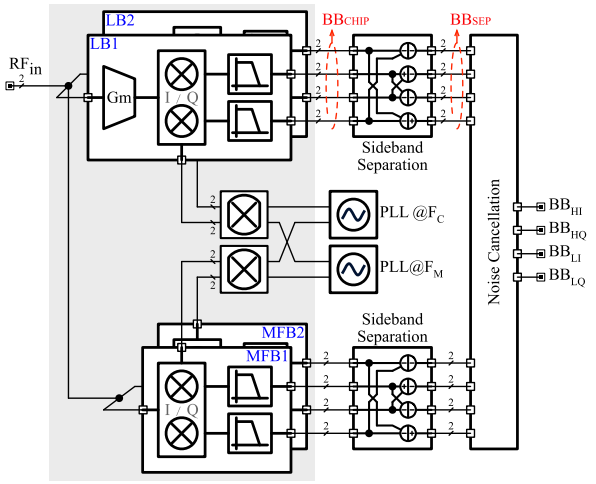


Fig. 1. Simplified block diagram of the proposed multi-branch MMC receiver.

carriers without translational loops and realizes broadband matching with an off-chip hybrid coupler. The broadband interface offers no selectivity at RF and, thus, limits the OB linearity. The gain-boosted N-path-filter [18] receiver can also aggregate two inter-band RF carriers and offers a tuned antenna interface at two distinct frequencies by placing N-path band-stop filters in a feedback loop. However, its active realization limits both the in-band and the OB linearity. Recently, an FTNC receiver [19] has been proposed utilizing 32-phase non-overlapping clocks. By summing the down-converted signals with the appropriate weights, up to three RF carriers can be received concurrently. It offers a tuned RF interface at the desired frequencies but is also matched at all other harmonic frequencies. A key limitation is that the RF carriers have to be harmonically related and cannot be arbitrarily allocated.

To receive carriers at F_{RF1} and F_{RF2} with mixer clock modulation, a modulation clock at $F_M = |F_{\mathrm{RF1}} - F_{\mathrm{RF2}}|/2$ is used to modulate an RF clock at $F_C = (F_{\mathrm{RF1}} + F_{\mathrm{RF2}})/2$ in Fig. 1. Applying the resulting clocks to mixer-first branches (MFBs) translates the low-pass baseband impedance to two narrow-band bandpass responses at F_{RF1} and F_{RF2}. It offers up-front RF filtering and tuned matching around these frequencies, thus achieving better OB linearity. By adding two LNTA branches (LBs), noise cancellation across both carriers can be performed, and the receiver's noise performance is improved. If PRBS sequences are used for clock modulation, the MFBs can also be used for rapid CS spectrum scanning [8]. With no clock modulation, the receiver works as a standard FTNC receiver with excellent OB linearity for single-carrier reception.

This article is organized as follows. Section II develops the proposed multi-branch modulated-mixer-clock (MMC) receiver architecture. Section III describes configurability and analytical analyses, including RF interface and OB linearity, conversion gain, noise analysis, sideband rejection, and spurious responses. Sections IV and V present the circuit implementation and experimental results. Section VI compares this work with the prior art in concurrent receivers and CS spectrum scanners. Section VII gives conclusions.

II. Multi-Branch Modulated-Mixer-Clock Receiver Architecture Development

We now develop the proposed multi-branch MMC receiver architecture step by step. With the aid of periodic S-parameters and periodic AC analyses, we quantify the behaviors of the proposed circuits.

A. Single I/Q Mixer-First Receiver

Consider a single I/Q mixer-first receiver shown in Fig. 2(a). The mixers are implemented as NMOS switches and are driven by four-phase 25%-duty-cycle, non-overlapping clocks

$$\xi_i(t) = \sum_{k=-\infty}^{+\infty} \alpha_k \cdot e^{-j\frac{k\pi}{2}\cdot i} \cdot e^{jk2\pi F_C t} \tag{1}$$

where $F_C = 1/T_C$, $\alpha_k = (1/4)\cdot\exp(\text{-}jk\pi/4)\cdot\mathrm{sinc}(k\pi/4)$, and $i = \{0, 1, 2, 3\}$. These clocks have strong frequency components at their fundamental and harmonic frequencies. The RF input impedance [20], [21] becomes the mixer switch resistance R_{SW} in series with the frequency-translated baseband impedance Z_{BB} that loads the mixer. Fig. 2(b) shows the simulated input matching and RF filtering profiles using $F_C = 800$ MHz. The input impedance is 50 Ω within the signal band of interest but low outside, thus attenuating OB blocking signals and preventing them from developing large voltage swings at the receiver's input. However, this feature of tuned matching makes it impractical to connect multiple mixer-first receivers in parallel for concurrent matching.

B. Single I/Q Mixer-First Receiver With Modulated Clocks

Let us now consider an I/Q mixer-first receiver [see Fig. 3(a)] with the mixer switches clocked by four modulated clocks that are generated by mixing four-phase 25%-duty-cycle, non-overlapping clocks at F_C and two-phase 50%-duty-cycle, non-overlapping clocks at F_M. These 50%-duty-cycle clocks are

$$\rho_i(t) = \sum_{n=-\infty}^{+\infty} \beta_n \cdot e^{-jn\pi\cdot i} \cdot e^{jn2\pi F_M t} \tag{2}$$

where $F_M = 1/T_M$, $\beta_n = (1/2)\cdot\exp(\text{-}jn\pi/2)\cdot\mathrm{sinc}(n\pi/2)$, and $i = \{0, 1\}$. Using the equations in Fig. 3(b), the modulated clocks can be derived

$$\begin{aligned}
\phi_0(t) &= \sum_{p,q} \alpha_p\beta_q \cdot [1 + (-1)^{p+q}] \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_1(t) &= \sum_{p,q} \alpha_p\beta_q \cdot e^{-jp\frac{\pi}{2}} \cdot [1 + (-1)^{p+q}] \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_2(t) &= \sum_{p,q} \alpha_p\beta_q \cdot e^{+jq\pi} \cdot [1 + (-1)^{p+q}] \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_3(t) &= \sum_{p,q} \alpha_p\beta_q \cdot e^{+jp\frac{\pi}{2}} \cdot [1 + (-1)^{p+q}] \cdot e^{j2\pi(pF_C + qF_M)t}
\end{aligned} \tag{3}$$

where p and q are any integers. The differential, modulated mixer clocks are then

$$\begin{aligned}
\phi_0(t) - \phi_2(t) &= 4 \cdot \sum_{p,q} \alpha_p\beta_q \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_1(t) - \phi_3(t) &= 4 \cdot \sum_{p,q} \alpha_p\beta_q \cdot e^{-jp\frac{\pi}{2}} \cdot e^{j2\pi(pF_C + qF_M)t}
\end{aligned} \tag{4}$$

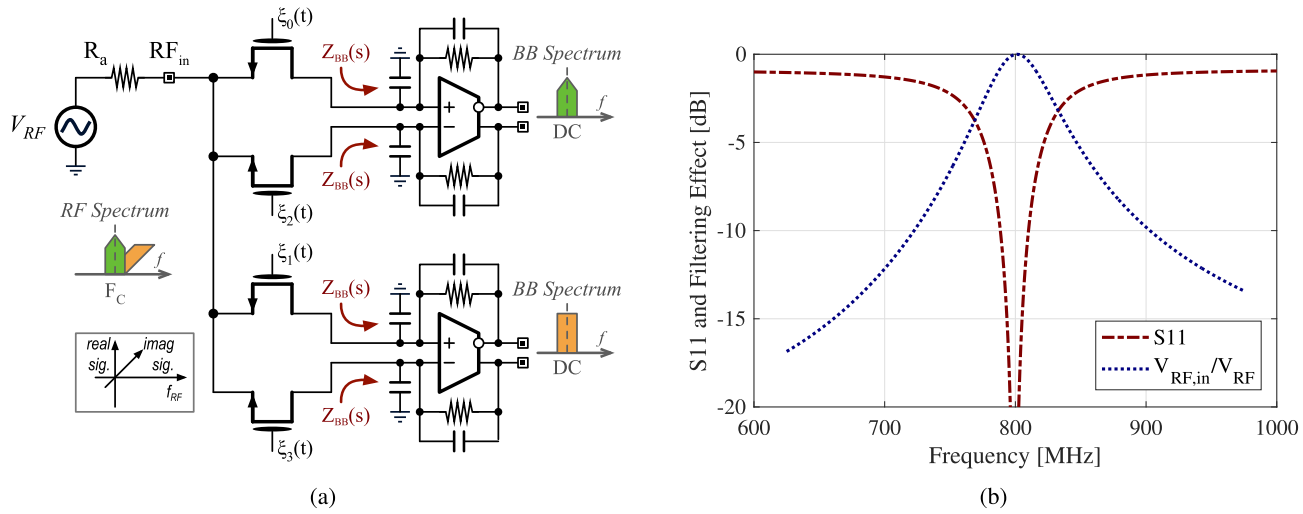


Fig. 2. Single I/Q mixer-first receiver driven by four-phase 25%-duty-cycle, non-overlapping clocks. (a) Simplified schematic whose mixer switches are loaded by the baseband impedance $Z_{BB}(s)$. (b) Simulated input matching S_{11} and up-front RF filtering ($V_{RF,in}/V_{RF}$) for an 800-MHz clock, a 2.5-Ω switch resistance, and $Z_{BB}(s)$ is the parallel combination of a 300-Ω resistor and 45-pF capacitor.

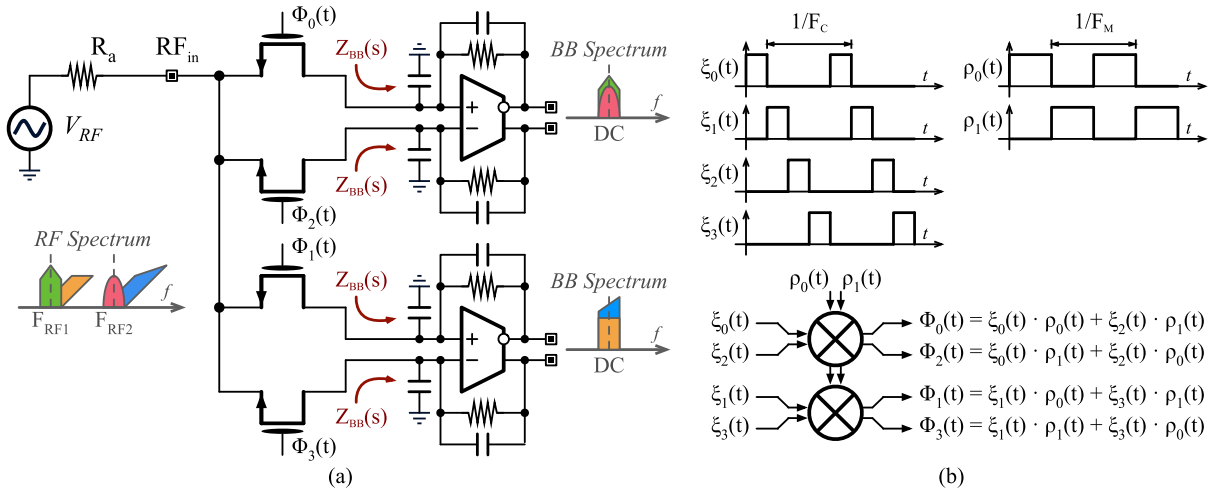


Fig. 3. Single I/Q mixer-first receiver driven by modulated mixer clocks. (a) Simplified schematic. (b) Digital modulator input clock waveforms and the expressions for the output modulated clock signals.

where p and q are odd integers. These waveforms contain strong components at $(F_C \pm F_M)$. Passive mixer switches, driven by these modulated clocks, translate the baseband impedance to $(F_C \pm F_M)$ and down-convert the signals around $(F_C \pm F_M)$ to baseband. However, the I/Q components of both signals are overlapping at baseband. To distinguish the I/Q components from both signals, more down-conversion branches are needed.

C. Dual I/Q Mixer-First Receiver With Modulated Clocks

Two I/Q mixer-first receivers are now placed in parallel [see Fig. 4(a)] and are driven by eight modulated clocks that need to be non-overlapping to achieve tuned impedance matching. These modulated clocks are generated by mixing four-phase 25%-duty-cycle, non-overlapping clocks at F_C, $\xi_0(t)$ to $\xi_3(t)$, and four-phase 25%-duty-cycle, non-overlapping clocks at F_M, $\rho_0(t)$ to $\rho_3(t)$. Based on the equations in Fig. 4(b), the expressions of these four pairs of differential, modulated clocks are

$$\begin{aligned}
\phi_0(t) - \phi_4(t) &= 4 \cdot \sum_{p,q} \alpha_p \alpha_q \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_1(t) - \phi_5(t) &= 4 \cdot \sum_{p,q} \alpha_p \alpha_q \cdot e^{-jp\frac{\pi}{2}} \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_2(t) - \phi_6(t) &= 4 \cdot \sum_{p,q} \alpha_p \alpha_q \cdot e^{-jq\frac{\pi}{2}} \cdot e^{j2\pi(pF_C + qF_M)t} \\
\phi_3(t) - \phi_7(t) &= 4 \cdot \sum_{p,q} \alpha_p \alpha_q \cdot e^{-j(p+q)\frac{\pi}{2}} \cdot e^{j2\pi(pF_C + qF_M)t} \quad (5)
\end{aligned}$$

where p and q are odd integers. These modulated clocks contain strong frequency components at $(F_C \pm F_M)$. Thus, the tuned input interface and the RF filtering effect are achieved. Fig. 5 shows the simulated input matching profiles using different F_M frequencies with a fixed F_C at 800 MHz. The return loss is low around $(F_C - F_M)$ and $(F_C + F_M)$, but

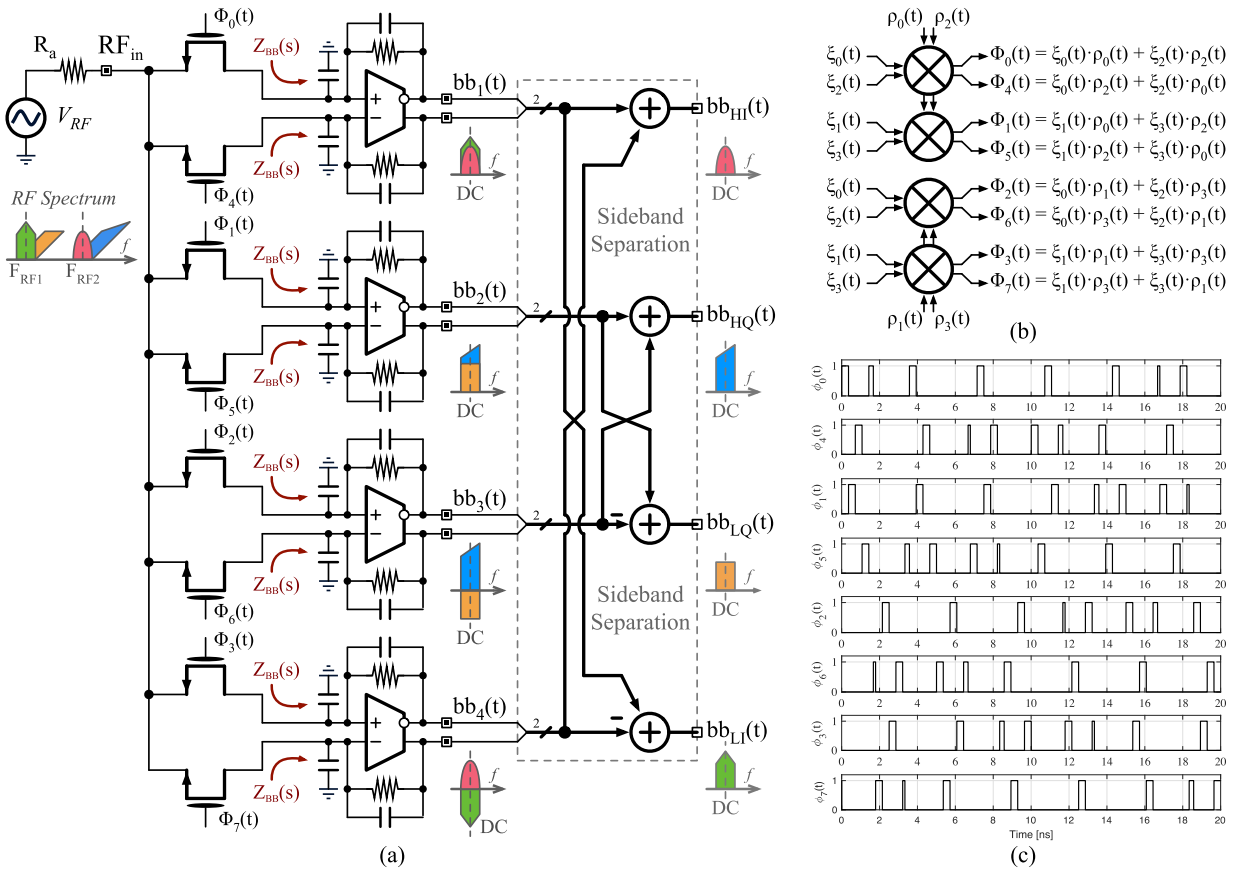


Fig. 4. Two I/Q mixer-first receivers placed in parallel and driven by modulated mixer clocks. (a) Simplified schematic. (b) Expressions for modulated clocks. (c) Time-domain waveforms of modulated clocks using $F_C = 700$ MHz and $F_M = 150$ MHz.

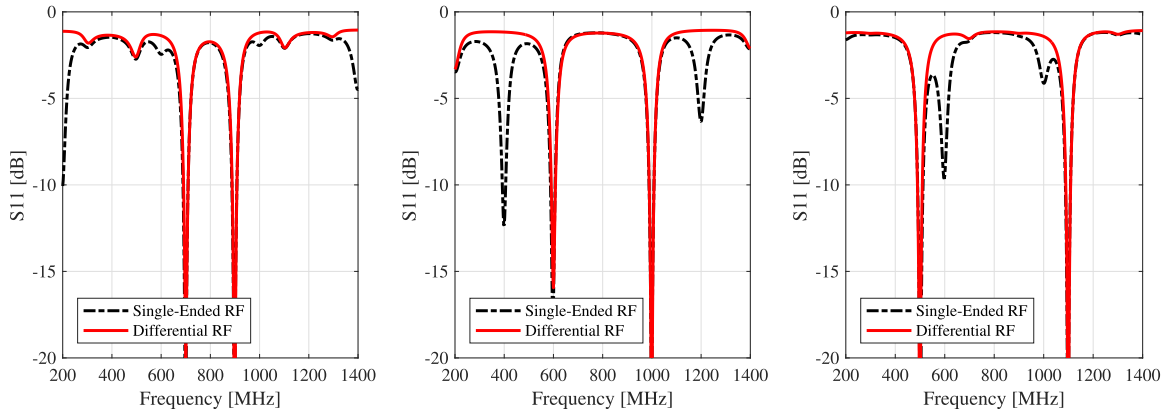


Fig. 5. Simulated input matching profiles of the dual mixer-first receiver structure for single-ended and differential RF inputs with a 2.5-Ω switch resistance and 1.05-kΩ in parallel with 20-pF as $Z_{\mathrm{BB}}(s)$, and using $F_C = 800$ MHz and different F_M rates: (left) 100 MHz, (middle) 200 MHz, and (right) 300 MHz.

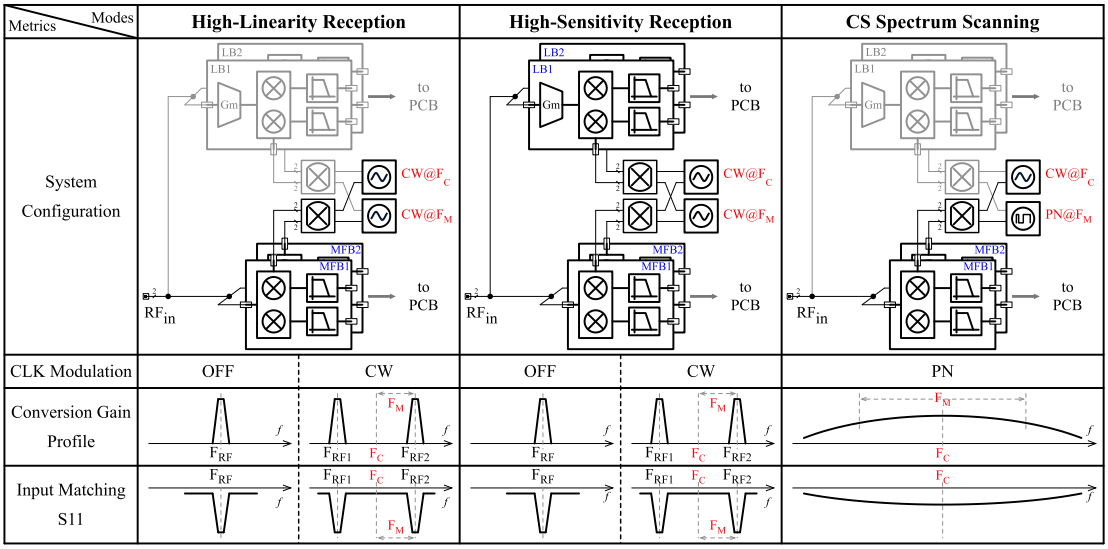
OB signals are attenuated right at the RF interface for a good OB linearity.

In addition, the modulated clocks have different phase shifts at $(F_C \pm F_M)$ [see (5)], resulting in linearly independent down-converted signals and allowing the simple extraction of the I/Q components from both carriers (see Fig. 4). For example, the baseband outputs $bb_1(t)$ and $bb_4(t)$ contain the in-phase components from both carriers but with a different polarity; subtracting $bb_1(t)$ and $bb_4(t)$, the in-phase component from the lower carrier is extracted since the in-phase component from the carrier at $(F_C - F_M)$ adds up, whereas the component from the carrier at $(F_C + F_M)$ cancels. Similarly, the in-phase component from the higher carrier is obtained by summing $bb_1(t)$ and $bb_4(t)$.

D. Multi-Branch Modulated-Mixer-Clock Receiver

Next, two LBs (LB1 and LB2) are added to obtain the multi-branch MMC receiver (see Fig. 1) with improved sensitivity. Since the LNTAs have high input impedance, the tuned

TABLE I
CONFIGURATIONS OF THE MULTI-BRANCH MMC RECEIVER



interface and RF filtering effect are preserved. A single LNTA can be used if its subsequent mixers are driven by modulated mixer clocks that are generated by four-phase 25%-duty-cycle, non-overlapping clocks at F_C and F_M. We opted to use two LNTAs, one for each branch, followed by mixers driven by modulated mixer clocks that are generated from four-phase 25%-duty-cycle, non-overlapping clocks at F_C and quadrature, two-phase 50%-duty-cycle, non-overlapping clocks at F_M since that achieves higher current conversion gain in the mixers.[1] The differential clocks for LB1 and LB2 are in quadrature. The I/Q components of the two bands can be obtained with simple addition and subtraction, similar to the dual MFBs.

III. MULTI-BRANCH MODULATED-MIXER-CLOCK RECEIVER ANALYSIS

We now introduce the different configurations supported by the proposed receiver (see Table I). We then analyze the concurrent dual-carrier reception operation; the single-carrier reception and CS spectrum scanning have been studied in [22] and [23].

A. Receiver Configurations

The operation of the receiver is changed by changing the clock modulation type. A CW clock modulation results in concurrent, dual-carrier reception. This configuration has two sub-modes. For high-linearity, only the two MFBs are used. Due to the large baseband capacitance at baseband TIA's inputs, the OB blocking signals are strongly attenuated, thus offering excellent OB linearity. For high-sensitivity, both MFBs and both LBs are activated. The outputs from these branches are combined with proper coefficients to perform noise cancellation for better sensitivity.

With pseudo-noise (PN) clock modulation, the receiver does CS spectrum scanning. Both LNTA branches are powered down, while both MFBs are active. The PN sequences are used to modulate the RF clocks, resulting in a wideband conversion gain that allows rapid spectrum scanning with CS DSP.

With no clock modulation, the receiver performs single-carrier reception. This configuration also supports high-linearity and high-sensitivity sub-modes. However, in this case, only one LB and one MFB are used.

B. Tuned RF Interface and OB Linearity Improvement

The mixer-first tuned RF interface provides input impedance matching at $(F_C \pm F_M)$ while reflecting OB blocking signals, thus enhancing OB linearity (see Fig. 5). When using a single-ended RF interface, there is also matching at $(p \cdot F_C + q \cdot F_M)$, with p and q as any integers. In this work, we use a differential RF interface, so matching only occurs when p and q are odd.

For OB frequencies, the switch resistance R_{SW} dominates the RF input impedance [24], and the OB attenuation is then

$$\mathrm{ATTN_{OB}} = -20 \cdot \log_{10}\left(2 \cdot \frac{2R_{SW}}{2R_{SW} + R_S}\right) \tag{6}$$

where $R_S = 100\ \Omega$ is the antenna source resistance. Fig. 6 shows the simulated input reflections and RF filtering profiles for different R_{SW} values. When $R_{SW} = 3\Omega$, OB S_{11} is -1 dB, and the OB attenuation is 19 dB, i.e., the OB signals are reflected, and the voltage swing they create at the RF input is almost nine times smaller compared with a broadband match. For example, if a broadband-terminated receiver has a -15-dBm B1dB, then the tuned RF interface is expected to improve B1dB with 19 dB to $+4$ dBm. When $R_{SW} = 15\Omega$,

[1]Note that architecture with a single, double-sized LNTA and 25%-duty-cycle-modulated I/Q mixers will have a 3 dB higher conversion gain compared with architecture with two LNTAs and 50%-duty-cycle-modulated I/Q mixers; as a result, the first architecture will have a 0.3 dB better noise figure but also a worse large-signal in-band linearity, such as P1dB, due to the increased gain.

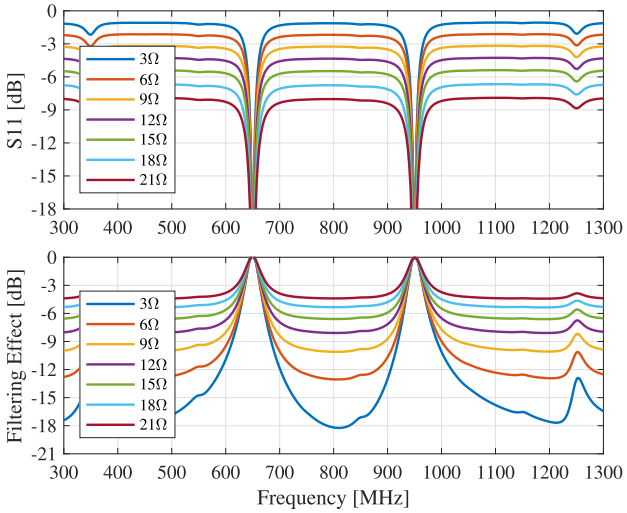


Fig. 6. Simulated input matching S_{11} and up-front RF filtering ($V_{\mathrm{RF,in}}/V_{\mathrm{RF}}$) with different R_{SW} values using $F_C = 800$ MHz and $F_M = 150$ MHz.

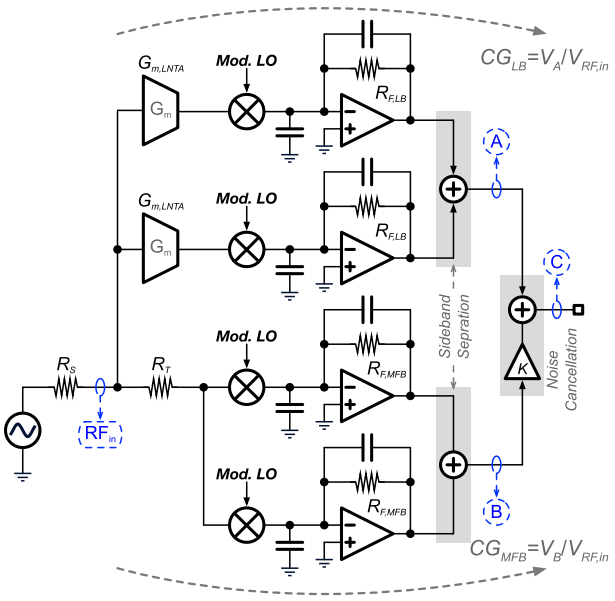


Fig. 7. Simplified block diagram of the system for noise analysis in the dual-carrier reception mode.

OB S_{11} is -5.4 dB, offering 7 dB of OB attenuation and B1dB improvement.

C. Conversion Gain Analysis and In-Band Linearity

In single-carrier reception, the conversion gain of the LNTA branch (see Fig. 1) is

$$\left(\frac{V_{\mathrm{BB,CHIP}}}{V_{\mathrm{RF,in}}}\right) = G_{m,\mathrm{LNTA}} \cdot G_{\mathrm{MXR}} \cdot R_{F,\mathrm{LB}} \tag{7}$$

where $G_{m,\mathrm{LNTA}}$ is the LNTA transconductance, $G_{\mathrm{MXR}} = \sqrt{2}/\pi$ is the current-conversion gain of the mixers [25], and $R_{F,\mathrm{LB}}$ is the TIA feedback resistance for the LBs. For concurrent, dual-carrier reception using F_M modulated mixer clocks, the mixer conversion gain reduces by a factor of $(2/\pi)$ or 3.9 dB and becomes $(2\sqrt{2})/\pi^2$. After sideband separation, the baseband signals double, and the conversion gain of the LBs becomes

$$CG_{\mathrm{LB}} \equiv \frac{V_{\mathrm{BB,SEP}}}{V_{\mathrm{RF,in}}} = 2 \cdot G_{m,\mathrm{LNTA}} \cdot G_{\mathrm{MXR}} \cdot \frac{2}{\pi} \cdot R_{F,\mathrm{LB}}. \tag{8}$$

This gain is 2.1 dB higher than the conversion gain in the single-carrier reception mode.

A similar analysis can be done for the MFBs except that the mixer current-conversion gain now degrades by a factor of $(\sqrt{2}/\pi)$ or 6.9 dB. After sideband separation, the baseband signals again double, and the conversion gain to the separated output is only 0.9 dB lower than the conversion gain for single-carrier reception

$$CG_{\mathrm{MFB}} = -2 \cdot \frac{1}{R_S} \cdot G_{\mathrm{MXR}} \cdot \frac{\sqrt{2}}{\pi} \cdot R_{F,\mathrm{MFB}} \tag{9}$$

where $R_{F,\mathrm{MFB}}$ is the TIA feedback resistance for the MFBs.

The receiver's large-signal in-band linearity, such as P1dB, is mostly limited by the output swing of the baseband circuits and, thus, the supply voltage due to the need for sufficient amplification. With mixer clock modulation and sideband separation, the LB has a higher conversion gain, as given in (8), compared with the conversion gain for single-carrier reception. Thus, its in-band linearity will be worse than that for the single-carrier reception by 2.1 dB. However, the MFB has a 0.9 dB lower conversion gain, as given in (9), meaning that it can tolerate in-band signals with slightly higher power levels. The mixer switches should not be the bottleneck for the in-band linearity since they are still used as current-driven passive switches.

D. Noise Analysis

For single-carrier reception, the receiver operates as an FTNC architecture, and the noise of the impedance matching can be canceled by properly setting the relative gain of the two branches [22]. To the first order, the LNTA transconductor is the only significant noise contributor, and the receiver's noise factor becomes

$$F = \left(1 + \frac{\gamma}{G_{m,\mathrm{LNTA}} R_S}\right) \cdot \frac{\pi^2}{8} \tag{10}$$

where R_S is the antenna source resistance. The multiplication factor in (10) is the noise folding factor [26] for the F_C clock harmonics.

For dual-carrier reception, the simplified receiver model in Fig. 7 is used. It is based on the model in [2], but, now, we are studying the noise behavior for dual-carrier reception. In our receiver, there is no explicit resistor R_T. However, R_T models the noise contribution from the up-converted equivalent baseband resistance at the TIA input. As earlier, we further assume that the LNTA transconductors are the dominant noise contributors, but the analysis can be easily extended to include contributions from other noise sources. First, we will analyze the LBs with their RF clock being modulated by the modulation clock at F_M. Next, the cancellation of the noise of the matching resistor R_T will be discussed, together with the noise cancellation condition. The expression

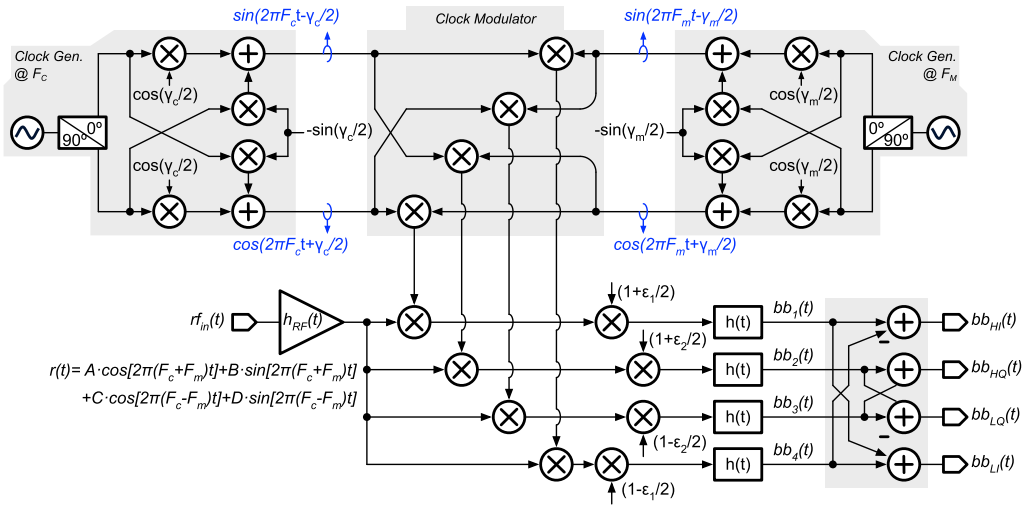


Fig. 8. System-level model for investigating the impact of phase and gain mismatches on the sideband rejection.

of the receiver's noise factor and conversion gain is derived at the end.

1) Noise Behavior of the LNTA Branches: The output noise of the LBs after sideband separation, i.e., at node A in Fig. 7, is due to the noise from the source resistor R_S, the matching resistor R_T, and the LNTA transconductors. Assuming the impedance matching condition, the noise contribution due to the two resistors is the same and can be derived as

$$\frac{v_{nA,R_S}^2}{\Delta f} = \frac{v_{nA,R_T}^2}{\Delta f} = 4kTR_S \cdot \left(\frac{1}{2}CG_{\mathrm{LB}}\right)^2 \cdot \left(\frac{\pi^2}{8}\right)^2 \quad (11)$$

where the two multiplication factors of $(\pi^2/8)$ stem from the noise folding from both the F_C and F_M harmonics. The noise contribution from the LNTA transconductor is

$$\frac{v_{nA,G_m}^2}{\Delta f} = \frac{4kT\gamma}{G_{m,\mathrm{LNTA}}} \cdot CG_{\mathrm{LB}}^2 \cdot \left(\frac{\pi^2}{8}\right)^2. \quad (12)$$

The noise factor at node A is derived by comparing the total output noise to the output noise due to the source resistor R_S

$$F_A = \left(2 + \frac{4\gamma}{G_{m,\mathrm{LNTA}}R_S}\right) \cdot \left(\frac{\pi^2}{8}\right)^2. \quad (13)$$

2) Noise Cancellation and Cancellation Condition: The noise contributions from R_T at the outputs of the LBs (node A) and MFBs (node B) after sideband separation are anti-correlated. By summing these two outputs at node C with proper weighting, the noise from R_T can be canceled, while the desired signals add. At C, the noise contribution due to the LNTA transconductors stays the same, while the noise contributions due to the source resistor R_S and the matching resistor R_T change. The contribution to the output noise at node C from to the matching resistor R_T is

$$\frac{v_{nC,R_T}^2}{\Delta f} = 4kTR_T \cdot \left(\frac{1}{2} \cdot CG_{\mathrm{LB}} - \frac{K}{2} \cdot CG_{\mathrm{MFB}}\right)^2 \cdot \left(\frac{\pi^2}{8}\right)^2 \quad (14)$$

where K is the gain coefficient to adjust the relative gain of the two signal branches. This noise can be canceled by setting K to K_{NC}

$$K_{\mathrm{NC}} = \frac{CG_{\mathrm{LB}}}{CG_{\mathrm{MFB}}} = -\sqrt{2} \cdot G_{m,\mathrm{LNTA}}R_S \cdot \frac{R_{F,\mathrm{LB}}}{R_{F,\mathrm{MFB}}}. \quad (15)$$

Now, the noise from the source resistor R_S is

$$\frac{v_{nC,R_S}^2}{\Delta f} = 4kTR_S \cdot \left(\frac{1}{2}CG_{\mathrm{LB}} + \frac{K_{\mathrm{NC}}}{2}CG_{\mathrm{MFB}}\right)^2 \cdot \left(\frac{\pi^2}{8}\right)^2 = 4kTR_S \cdot CG_{\mathrm{LB}}^2 \cdot \left(\frac{\pi^2}{8}\right)^2. \quad (16)$$

3) Noise Performance After Cancellation: Under the cancellation condition, the conversion gain becomes twice the conversion gain of the LB given in (8). The noise factor of the dual-carrier receiver can now be derived by comparing the total noise at C to the noise at C due to the noise from the source resistor R_S

$$F_{\mathrm{RX}} = \left(1 + \frac{\gamma}{G_{m,\mathrm{LNTA}}R_S}\right) \cdot \left(\frac{\pi^2}{8}\right)^2. \quad (17)$$

This equation has a similar form as that derived in [22]. The only difference is the extra folding factor of $(\pi^2/8)$ due to the noise folding from the F_M clock harmonics. Assuming $\gamma = 2/3$, $R_S = 50\ \Omega$, and $G_{m,\mathrm{LNTA}} = 80$ mS, the calculated NF for single-carrier reception is 1.6 dB and degrades to 2.5 dB for concurrent, dual-carrier reception. These estimates match within 0.1 dB with the simulated noise figure using schematic-level behavioral models and periodic steady-state and periodic noise analyses with shooting engine.

E. Low- to High-Band Isolation

If the mixer driving clocks are ideal with no phase imbalances and the analog baseband circuits are perfectly phase and gain matched, the low-band outputs contain only signals down-converted from the lower RF carrier at $(F_C - F_M)$ and similarly for the high-band outputs at $(F_C + F_M)$ [see Fig. 4(a)]. In practice, due to non-idealities, the low-band outputs will contain signal components down-converted from the high band and vice versa. The model shown in Fig. 8 is

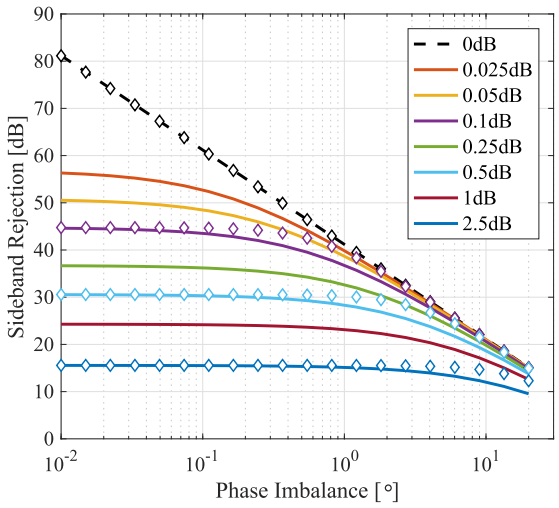


Fig. 9. Studies of phase and gain imbalances on the sideband rejection: comparison of analytical (⋄) and simulation results (–).

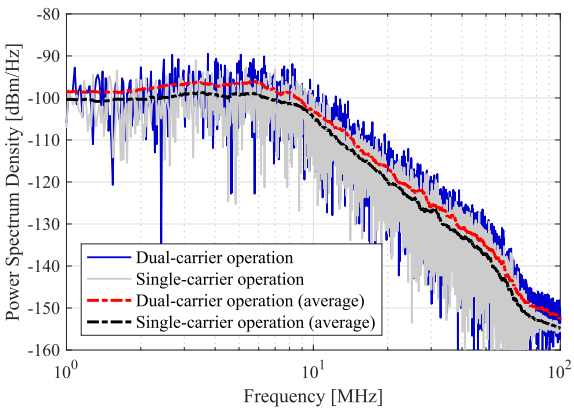


Fig. 10. Simulated baseband PSDs for single-carrier and dual-carrier reception.

used to study the effects of phase and gain imbalances on the band-to-band isolation [27], where γ_c and γ_m are the phase imbalances of the LO clocks running at F_C and F_M, respectively, and ϵ_1 and ϵ_2 are the amplitude imbalances due to gain mismatches in the analog baseband circuitry. Typically, the F_M clocks are running at a significantly lower rate compared with the F_C clocks, and the phase imbalance of the F_M clocks can be neglected by assuming it is zero. The sideband rejection is the ratio of the down-converted signal power from the desired carrier and that of the down-converted signal from the undesired carrier

$$\text{SBR} = \frac{1+\cos[\gamma_c + 2\cdot\text{atan}(\epsilon_1/2)]}{1-\cos[\gamma_c - 2\cdot\text{atan}(\epsilon_1/2)]}. \tag{18}$$

Fig. 9 shows the sideband rejection as a function of phase mismatches for varying gain mismatch. The analytical results agree well with the simulation results. To demodulate an uncoded QAM-256 modulated signal[2] with a bit error ratio of 10^{-6}, a minimum signal-to-noise-and-distortion ratio (SNDR) of 34 dB is needed [29], meaning that the phase imbalances need to be smaller than 2°, while the gain imbalances should stay below 0.3 dB.

F. Non-Idealities of Clock Generation Circuitry

The clock generation circuitry produces modulated mixer clocks using the waveforms running at F_C and F_M and distributes the modulated clocks to the LNTA and the MFBs. Non-idealities can happen from the clock sources and during generation and distribution, including the clock phase noise, the clock I/Q phase mismatches (already studied in Section III-E), and the missing of very narrow pulses.

[2]Both carriers contain useful information modulated onto them. To extract the information, they need to be separated and demodulated independently. We assume that the received power levels of the signals from both carriers are the same. Communication standards [28] often require the received power levels from different carriers to stay within a small range (e.g., ±3 dB) to guarantee roughly the same signal-to-noise ratio (SNR) for each carrier. It enables the same signal modulation scheme to offer more wireless throughput.

1) Effects of Phase Noise: The clock generation circuitry contains two clock inputs at F_C and F_M, with F_C in the GHz range, and F_M in the range of a few hundred MHz. Since the F_M clock source can be easily integrated with very low phase noise, we mainly focus on the impact of the phase noise from the F_C clock source. The model shown in Fig. 8 can also be used for the phase noise study except that the phase and gain mismatches are disabled and the phase noise of the RF clock at F_C is included.

An in-band phase noise profile with a close-in noise floor of −120 dBc/Hz and bandwidth of 80 MHz is created by adding bandpass-filtered noise to the F_C clock source. Transient simulations are performed using $F_C = 700$ MHz for single-carrier reception and $F_C = 700$ MHz and $F_M = 150$ MHz for dual-carrier reception. The desired RF signal is located 1.6 MHz away from the associated LO frequency with a power level of −60 dBm. An in-band blocking signal is placed at 20 MHz away, i.e., within the adjacent channels, with a power level of −20 dBm, which is around 40 dB higher than the desired RF signal [30]. The model assumes a 40-dB conversion gain for single-carrier reception, which corresponds to a 42.1-dB conversion gain for dual-carrier reception. The 2.1-dB gain increment stems from clock modulation and sideband separation (see Section III-C). The baseband filters with impulse response $h(t)$ are second-order low-pass Butterworth filters with 10-MHz bandwidth.

Fig. 10 shows the plots of the simulated baseband power spectral densities (PSDs) for both single- and dual-carrier receptions. The PSD for dual-carrier reception is about 2 dB higher than that for single-carrier reception. Qualitatively, the conversion gain for dual-carrier reception is slightly higher than that for single-carrier reception, thus leading to a slightly higher PSD floor. Quantitatively, the blocking signal shares the same transfer function as the desired signal, and it now converts the phase noise profile down to baseband, resulting in an elevated in-band PSD floor that is 2.1 dB higher compared with that for the single-carrier reception case. However, the signal power also increases by the same 2.1 dB, and the SNR is the same for both cases. The proposed technique does not impose extra requirements for the phase-noise performance of the F_C clock.

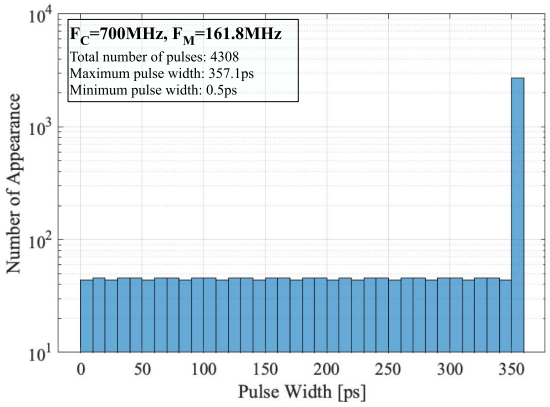


Fig. 11. Histogram of the simulated distribution of the pulse widths for one of the differential, modulated mixer clocks using $F_C = 700$ MHz and $F_M = 161.8$ MHz.

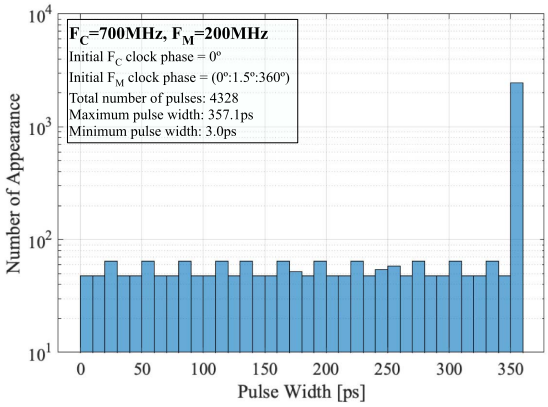


Fig. 12. Histogram of the simulated distribution of the pulse widths for one of the differential, modulated mixer clocks using $F_C = 700$ MHz and $F_M = 200$ MHz and with the initial F_M clock phase varying from 0° to 360° uniformly with 1.5° steps.

2) Effects of Missing Narrow Pulses: During mixer clock modulation, extremely narrow pulses can be produced by two mechanisms. For a given F_C and F_M, the shortest pulsewidth is related to the inverse of their least common multiple (LCM) and the duty cycles of the waveforms that are used for clock modulation. For example, for an $F_C = 700$ MHz and $F_M = 161.8$ MHz, the inverse of their LCM is 1.77 ps, and the shortest pulsewidth will be in the pico-second range. Fig. 11 shows the histogram of the simulated distribution of the pulse widths using the frequency combination mentioned earlier on one differential, modulated mixer clock for the MFBs. The simulation uses schematic-level behavioral models for digital modulators. In this scenario, the greatest common divisor (GCD) of the two clock rates is 0.2 MHz, and the modulated mixer clocks repeat themselves every 5 μs. The simulated, smallest pulsewidth is 0.5 ps and is as expected within the pico-second range; 63.2% of the pulses have a pulsewidth from 350 to 360 ps and 99.0% of the pulses have a width >10 ps.[3]

The second mechanism stems from the relative position of the transition edges of the F_C and F_M clocks. If the transition edges coincide or are spaced very closely in time, extremely narrow pulses can also occur in theory. Fig. 12 shows the histogram of the simulated distribution of the pulse widths on one differential, modulated mixer clock for the MFBs, where the initial F_C clock phase is fixed at 0°, and the initial F_M clock phase varies from 0 to 360° uniformly with 1.5° steps. The simulation uses $F_C = 700$ MHz and $F_M = 200$ MHz and schematic-level behavioral models. In this scenario, the GCD of the clock rates is 100 MHz, and the modulated mixer clocks repeat themselves every 10 ns; 56.7% of the pulses have a pulsewidth from 350 to 360 ps and 98.9% of the pulses have >10-ps widths.

In practice, due to the non-zero response time of the digital gates during clock modulation and distribution, some of these narrow pulses will be missed, which results in magnitude and phase mismatches. However, these narrow pulses contain very little energy in the frequency components that we care about the most, i.e., at $(F_C \pm F_M)$. The operation at these two frequencies is not affected significantly. To demonstrate the effects of the missing pulses, behavioral-model simulations are performed on one differential, modulated mixer clock in the MFBs using $F_C = 700$ MHz and $F_M = 200$ MHz. The initial F_M clock phase is set intentionally to create narrow pulses with around 4-ps widths. Fig. 13 shows the simulated magnitude and phase responses with and without the narrow pulses. For the lower RF carrier frequency at 500 MHz, the simulated magnitude and phase mismatches are 1.2 mdB and 0.22°, respectively. For the higher RF carrier frequency at 900 MHz, the simulated magnitude and phase mismatches are 34.5 mdB and 0.01°, respectively.

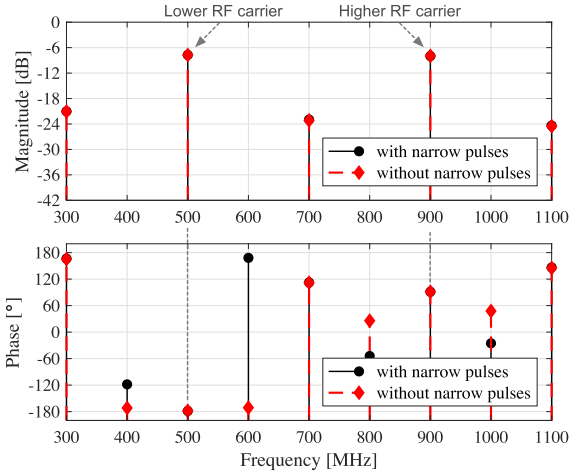


Fig. 13. Simulated magnitude (top) and phase (bottom) responses for one of the differential, modulated mixer clocks with and without narrow pulses using $F_C = 700$ MHz and $F_M = 200$ MHz.

G. Analysis of Spurious Responses

Mixer-clock modulation uniquely offers the possibility to concurrently receive signals from $(F_C - F_M)$ and $(F_C + F_M)$ with different phase shifts, making the baseband outputs easily linearly separable. Due to the rail-to-rail operation of

[3]For the 65-nm technology used in this research, digital gates have a fan-out-of-four (FO4) delay of around 10 ps. With more scaled and faster technologies, this number can be reduced.

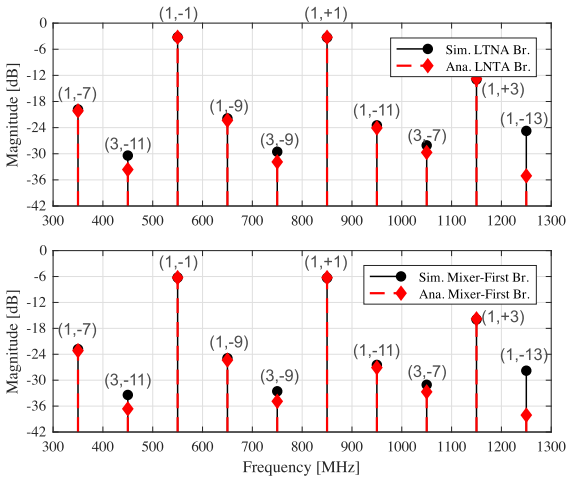


Fig. 14. Simulated and analytical differential LO spectra for LBs (top) and MFBs (bottom) for $F_C = 700$ MHz and $F_M = 150$ MHz.

digital logic gates and the hard switching operation of the mixers, the mixer clock modulation is realized with square waveforms. As a result, not only the fundamental tones of the F_C and F_M clocks are mixed together but the higher-order clock harmonics are also mixed, resulting in spurious receiver responses and meaning that the undesired signals from these inter-mixing tones will also get down-converted to baseband. For the MFBs, the location and its relative power levels of the spurious responses can be estimated with (5). For the LBs, (5) can also be used, but the Fourier coefficients need to be replaced by the term $\alpha_p \beta_q$ since the F_M clocks have a 50%-duty cycle. The analytical and simulated, differential modulated mixer clock spectra agree well (see Fig. 14).

The spurious rejection ratio (SRR) is the ratio of the conversion gain to the separated baseband outputs for the low or high band to the conversion gain from the spurious response at $(p \cdot F_C \pm q \cdot F_M)$, where p and q are both odd integers. To the first order, it is

$$\mathrm{SRR}_{p,q} = \frac{|\alpha_1 \cdot \alpha_1|}{|\alpha_p \cdot \alpha_q|} = \frac{\mathrm{sinc}^2(\pi/4)}{|\mathrm{sinc}(p\pi/4)| \cdot |\mathrm{sinc}(q\pi/4)|} \quad (19)$$

for the MFBs. For the LBs, the Fourier coefficients need to be replaced with $\alpha_1 \cdot \beta_1$ in the numerator and $\alpha_p \cdot \beta_q$ in the denominator.

Broadband receivers generally exhibit spurious responses [31]. For example, conventional single-carrier receivers employing four-phase 25%-duty-cycle, non-overlapping clocks at F_C have spurious responses at $p \cdot F_C$, where p is an odd integer. The impact of spurious responses largely depends on the desired input bandwidth for the receiver system and the extent of front-end RF filtering available, and the system frequency planning is often used to mitigate spurious responses. When using mixer-clock modulation, there are also spurious responses at the intermodulation products of higher order F_C and F_M harmonics that can fall into the receiver's RF frequency range and possibly degrade its linearity and noise performance. Higher-order clock modulation can be used to suppress and eliminate some of the spurious responses (e.g., [3] and [19]) and reduce the noise folding from the intermodulation products (see Section VI-C). However, this requires a more scaled, faster CMOS technology than the 65-nm technology used in this research.

IV. Circuit Implementation

The fully differential multi-branch MMC receiver prototype shown in Fig. 15(a) was implemented in 65-nm GP CMOS with an active area of 1.8 mm^2 [see Fig. 15(b) for the annotated die micrograph]. Operating from a 1.2-V power supply, the prototype consists of two LBs, two MFBs, and the clock path circuitry. For maximum testing flexibility, the baseband circuits for sideband separation and noise cancellation are implemented off-chip.

A. LNTA Branch

Each LB contains a cascoded common-source amplifier as its LNTA, current-mode passive mixers, and two baseband TIAs. The LNTA with common-mode feedback and bias circuitry [see Fig. 16(a)] delivers 88 mS of transconductance and consumes 13 mA. The common-source devices are biased at a (g_m/I_D) of 10 for good linearity, and the cascoded devices are biased at a (g_m/I_D) of 15 for good noise performance [32]. A replica biasing circuit is used to keep performance variations across process, voltage, and temperature (PVT) variations small. The passive mixers use transmission gates with a post-layout resistance R_{SW} of 7.5 Ω. The baseband TIAs use two-stage Miller-compensated OTAs with 4-bit feedback resistors and 5-bit feedback capacitors for baseband gain and bandwidth control, respectively.

B. Mixer-First Branch

The RF switches in the MFBs limit three key receiver performance metrics: the maximum operating frequency, the RF input matching profile, and the OB linearity. The parasitic drain/source-substrate junction capacitors limit the maximum operating frequency since, at high frequencies, the signal is lost to the grounded substrate. By floating the bodies of the bulk NMOS switches through a resistor within a deep N-well [33], these capacitive losses can be reduced. Processes with the high-resistivity substrate (e.g., SOI) can be employed to further significantly reduce these RF signal losses [34]. The RF input matching profile and the OB linearity are mainly limited by R_{SW} and the trace routing resistances. Processes with additional ultra-thick-metal (UTM) layers can help to significantly reduce the routing resistance.

The baseband TIAs use single-stage folded-cascode OTAs with 4-bit feedback resistors and 5-bit feedback capacitors for gain and bandwidth control. The Cherry–Hooper voltage buffers [see Fig. 16(b)] have 6-bit degeneration resistors and 2-bit feedback resistors for linearity and gain control. Due to their source resistive degeneration, they can handle signals up to 0 dBm at their input, deliver a simulated IIP3 of +20.3 dBm, and achieve a simulated voltage gain of 12.6 dB over a wide bandwidth with no additional filtering effects. The baseband TIAs and the voltage buffers together consume 4.92 mA per branch.

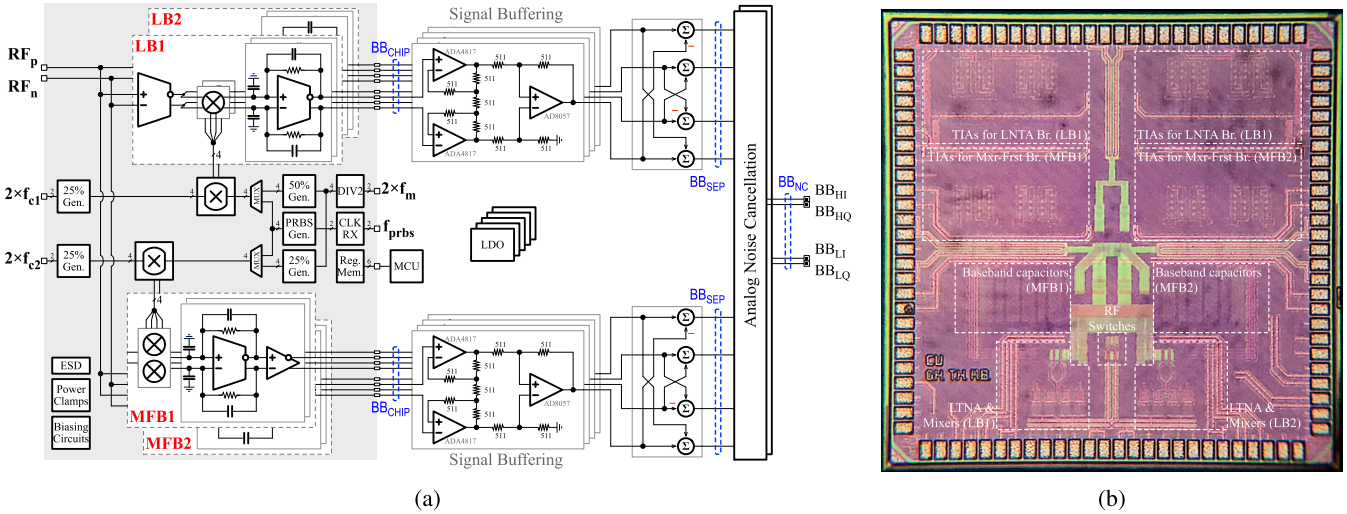


Fig. 15. Multi-branch modulated-mixer clock receiver prototype. (a) Block diagram. (b) Annotated die micrograph.

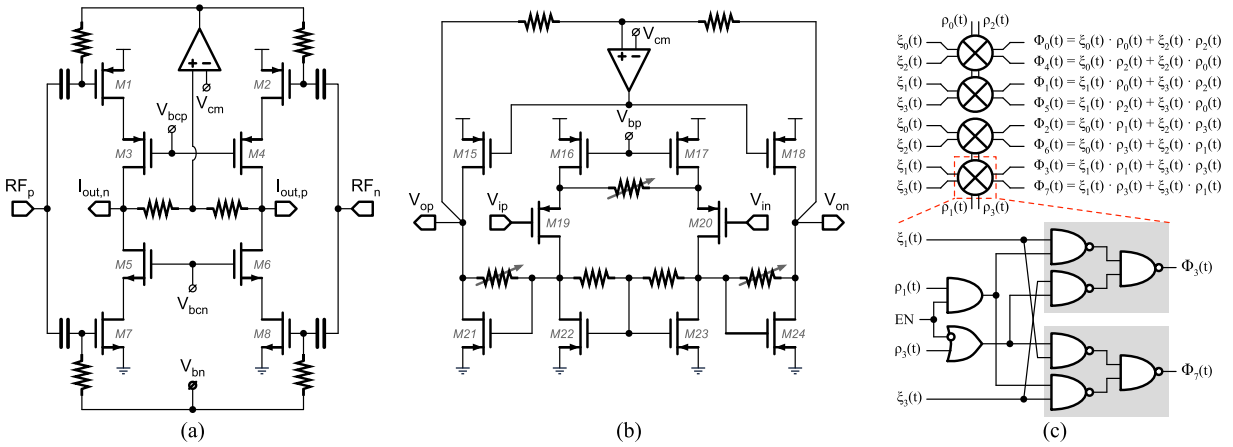


Fig. 16. Transistor-level implementation of some key blocks. (a) LNTA core. (b) Cherry–Hooper voltage buffer for the mixer-first path. (c) Core circuits of the clock modulator.

C. Clock Path

The clock generation path consists of clock receivers, dividers, non-overlapping waveform generators, clock buffers, and two clock modulators (each modulator in Fig. 16(c) containing four modulator cores). Matched, symmetrical layouts are used for the clock paths to all outputs to ensure that the duty cycle and the delay are the same, and careful verifications have been performed across all PVT variations.

When EN is low, the modulator cores directly pass the input RF clocks at F_C to their outputs. When EN is high, the modulator cores mix the RF clocks at F_C and the modulation clocks at F_M. They either flip the polarity the RF clock inputs or not or hold both output signals low. When one clock modulator core is switching, the outputs of the other three cores stop switching. Thus, all eight clock outputs are guaranteed to be non-overlapping by digital logic. The PRBS synthesizer can produce either shift-registered-based or LFSR-based sequences of various lengths.

For high-sensitivity, dual-carrier reception mode, the clock generation circuit consumes a simulated current of 16.68 mA using $F_C = 700$ MHz and $F_M = 200$ MHz. The current consumption of the clock generation circuit varies from 15.96 to 17.59 mA when F_C is fixed at 700 MHz and F_M varies from 100 to 300 MHz. If F_M is fixed at 200 MHz, the current consumption varies from 14.09 to 20.14 mA when the F_C clock rate changes from 500 to 1000 MHz. Note that the current consumption of the clock generation circuit will reduce to about half in the high-linearity sub-mode since the clock generation circuit now only provides clocks to the MFBs.

V. Experimental Results

The receiver prototype was bonded in an open-cavity 72-pin 10 mm × 10 mm QFN package and has been mounted on an FR-4 printed circuit board. Two symmetric 50-Ω transmission lines are used for differential RF inputs. A wideband balun converts the RF input signal from single-ended to differential.

A. Measurements for Single-Carrier Reception

We first open the RF switches in the MFBs and put a broadband resistive termination on the RF input. The swept-B1dB profile is measured by sweeping a tone from 350 to 1050 MHz,

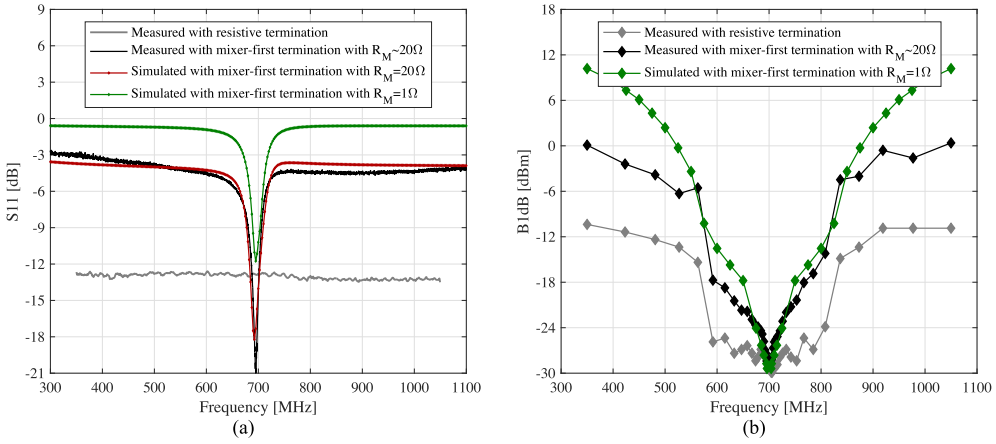


Fig. 17. Return loss and OB linearity for single-carrier reception with tuned mixer-first termination using $F_C = 700$ MHz compared with broadband resistive termination. (a) Measured and simulated return-loss profiles. (b) Measured and simulated swept-B1dB profiles.

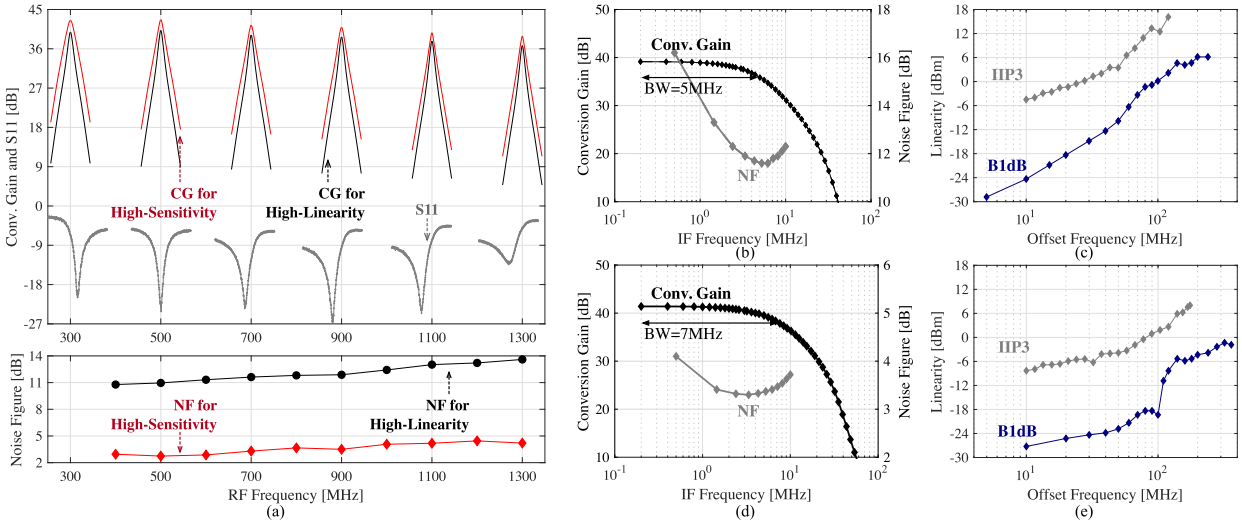


Fig. 18. Measurement results for single-carrier reception. (a) Conversion gain, return loss, and NF profiles for high-linearity and high-sensitivity sub-modes. (b) and (c) Conversion gain and NF versus IF frequency and IIP3 and B1dB versus offset frequency for high-linearity sub-mode, respectively. (d) and (e) Conversion gain and NF versus IF frequency and IIP3 and B1dB versus offset frequency for high-sensitivity sub-mode, respectively.

where a standard B1dB measurement at the LNTA branch outputs is performed at each tone frequency and is shown in Fig. 17, along with S_{11}. Then, we measure the performance of our prototype with the tuned RF-input interface using the mixer-first termination. Both MFBs are activated, forming two four-path filters in parallel. Due to the tuned RF interface, a 10-dB improvement in B1dB is measured. The 4-dB return loss floor in Fig. 17(a) stems from the RF switch resistance R_{SW} and the trace routing resistance R_M estimated from extractions to be 3 and 20 Ω, respectively, resulting in a total equivalent resistance of 23 Ω per branch, or about 12 Ω for both branches in parallel. The measured −4-dB OB S_{11} matches well with simulations and calculations. R_M can be significantly reduced to probably below 1 Ω in future designs by improving layout routing and using additional UTM layers. This will result in a significantly better OB S_{11} [see Fig. 17(a)] and up to an additional 10-dB B1dB improvement [see Fig. 17(b)].

Fig. 18 shows the measured performance[4] for single-carrier reception at various F_C. In high-linearity sub-mode at $F_C = 700$ MHz [see Fig. 18(b) and (c)], the B1dB is +6.2-dBm and IIP3 is +16.1 dBm, while the measured NF varies from 10.8 to 13.6 dB from 0.3 to 1.3 GHz. In high-sensitivity sub-mode at $F_C = 700$ MHz [see Fig. 18(d) and (e)], the B1dB is −1.3 dBm, and the IIP3 is +8.0 dBm; the measured NF after cancellation varies from 2.7 to 4.4 dB from 0.3 to 1.3 GHz, including 3 dB at 500 MHz and 4.1 dB at 900 MHz.

The measured clock power varies from 6.4 to 16.8 mW in the high-sensitivity sub-mode when the F_C clock rate varies from 300 to 1300 MHz. In the high-linearity reception sub-mode, this power reduces by half since the clock generation circuit only provides clocks to the MFB.

[4]The slight frequency offset between the minima in S_{11} and the maxima in the gain stems from the parasitics at the RF input (see [35]).

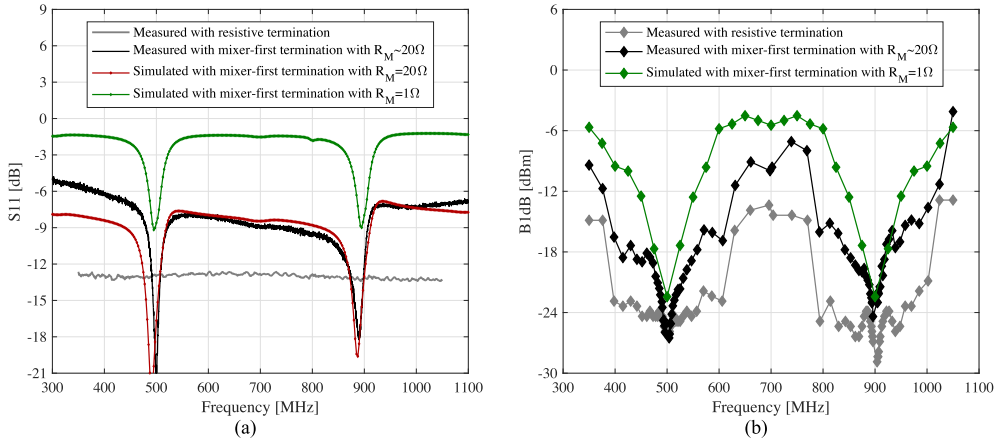


Fig. 19. Return loss and OB linearity improvement for concurrent dual-carrier reception by tuned mixer-first terminations using $F_C = 700$ MHz and $F_M = 200$ MHz. (a) Measured and simulated return loss profiles. (b) Measured and simulated B1dB.

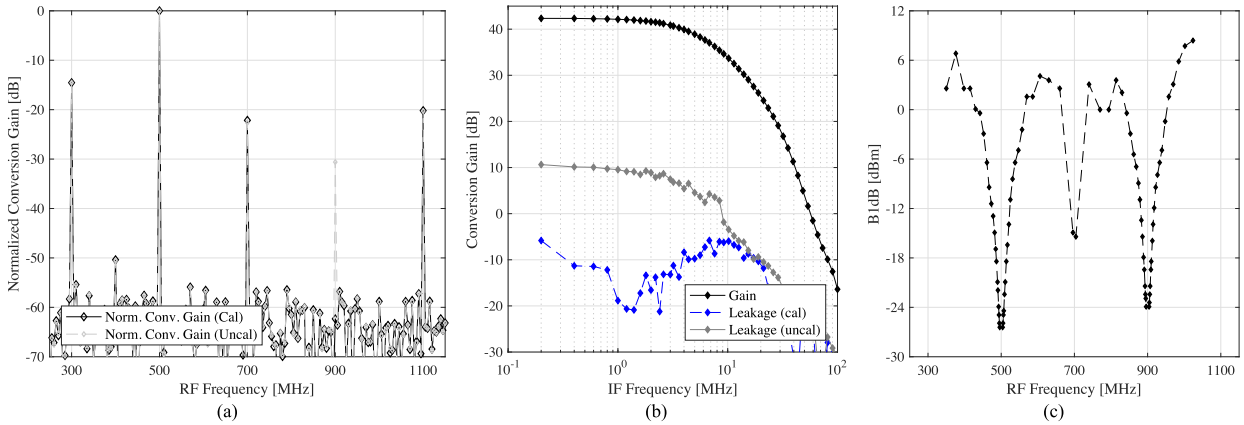


Fig. 20. Measurement results at low-bands output for concurrent high-linearity dual-carrier reception using $F_C = 700$ MHz and $F_M = 200$ MHz. (a) Spurious response profile. (b) Conversion gain and leakage from the higher RF carrier. (c) Swept-B1dB profile.

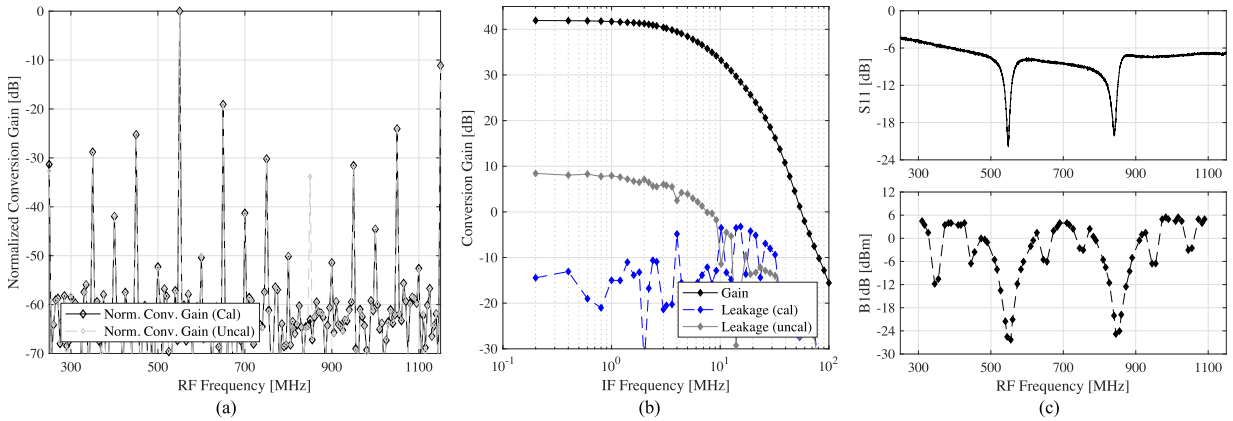


Fig. 21. Additional measurement results at low-band outputs for concurrent high-linearity dual-carrier reception using $F_C = 700$ MHz and $F_M = 150$ MHz. (a) Spurious response profile. (b) Conversion gain and leakage from the higher RF carrier. (c) S_{11} and swept-B1dB profiles.

B. Measurements for Concurrent Dual-Carrier Reception

For concurrent, dual-carrier reception, the modulated clock F_M can be swept from 100 to 300 MHz,[5] thus supporting reception with a carrier separations from 200 to 600 MHz. The measured clock power varies from 20.3 to 22.7 mW in the high-sensitivity reception sub-mode when F_C is fixed at 700 MHz and F_M varies from 100 MHz to 300 MHz. The power varies from 17.7 to 26.1 mW when F_M is fixed at 200 MHz and F_C varies from 500 to 1000 MHz. For high-linearity reception, the power reduces to about half since the clock generation circuit provides clocks only to the MFBs.

Similarly, as for the single-carrier reception, we measured the swept-B1dB profiles for $F_C = 700$ MHz and

[5]For concurrent dual-carrier measurements, the signal generators for the F_C and F_M clocks share a standard 10-MHz reference clock for the same time base. We did not knowingly set phase constraints on these two clocks but left the initial phase for these clocks as random by default.

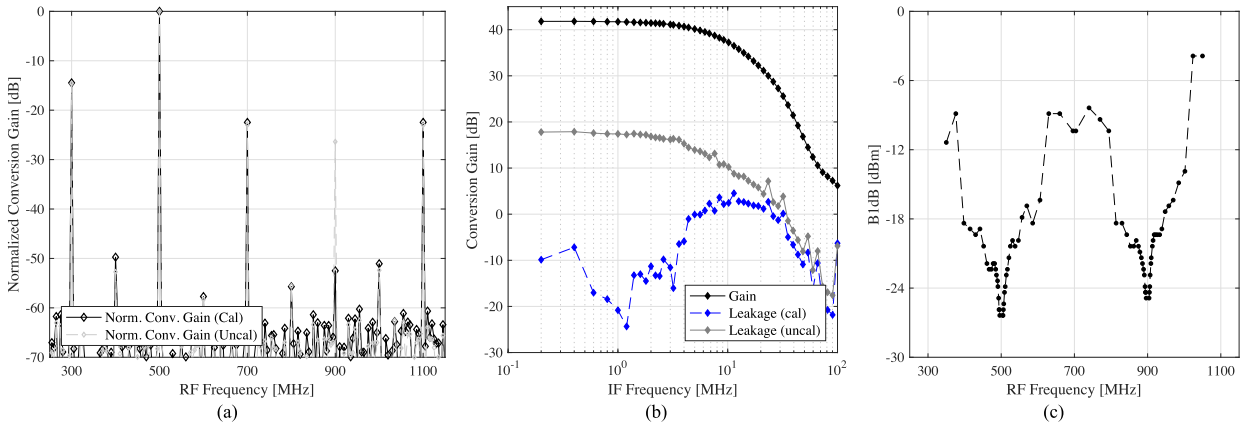


Fig. 22. Measurement results at low-band outputs for concurrent high-sensitivity dual-carrier reception using $F_C = 700$ MHz and $F_M = 200$ MHz. (a) Spurious response profile. (b) Conversion gain and leakage from the higher RF carrier. (c) Swept-B1dB profile.

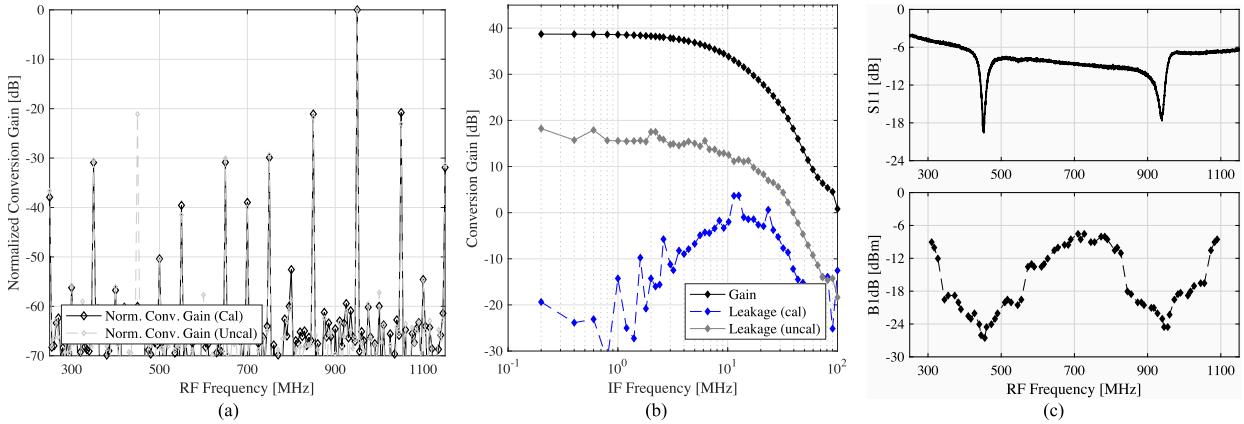


Fig. 23. Additional measurement results at high-band outputs for concurrent high-sensitivity dual-carrier reception using $F_C = 700$ MHz and $F_M = 250$ MHz. (a) Spurious response profile. (b) Conversion gain and leakage from the lower RF carrier. (c) S_{11} and swept-B1dB profiles.

$F_M = 200$ MHz with the dual-frequency tuned matching at $(F_C \pm F_M)$ from the mixer-first path, as well as with a broadband resistive match (see Fig. 19). About 6-dB B1dB improvement is measured due to the tuned mixer-first termination in Fig. 19(b). The two MFBs are driven by different clocks, and each presents a $(R_{SW} + R_M)$ of 23 Ω resulting in an OB S_{11} of -8.6 dB. With improved routing layout, R_M can be reduced below 1 Ω resulting in a better S_{11} profile [see Fig. 19(a)] and an additional 5-dB B1dB improvement [see Fig. 19(b)].

Fig. 20(a) shows the measured normalized conversion gain and swept-B1dB profiles for **high-linearity dual-carrier reception** (i.e., using only the MFBs) with $F_C = 700$ MHz and $F_M = 200$ MHz. The broadband conversion gain is then measured by sweeping a test tone from 250 to 1150 MHz with 5-MHz steps and 1-MHz offset and measuring the response at the low-band outputs. The swept-B1dB profile is measured by sweeping a test tone from 350 to 1050 MHz, and a standard B1dB measurement is performed at the low-band output for each frequency point. Equation (18) can be used to estimate the spurious response. For the spurious responses at $(F_C - 5F_M) = 300$ MHz, $(F_C - 9F_M) = 1100$ MHz, and $(F_C + 3F_M) = 1300$ MHz, rejection is estimated to be 14, 19, and 10 dB, respectively, which agrees well with the measurement. However, for the spurious responses at $(F_C - 3F_M) = 100$ MHz and $(F_C - 7F_M) = 700$ MHz, the measured rejections are 30 and 23 dB, which are better than the calculated results due to higher-order effects.

Fig. 20(b) shows the measured conversion gain versus IF frequency and the channel leakage from the high-band carrier. The channel leakage is measured by sweeping a test tone around the high-band carrier and measuring its contribution to the low-band output. The receiver achieves a 31.7-dB sideband rejection without calibration, which stems from the receiver's I/Q phase and gain mismatches, 1% board component mismatches, and trace length mismatches. With a standard calibration [23], [27] at 1 MHz, the receiver achieves a 48.2-dB sideband rejection across the whole channel. The calibration is done by first injecting a calibration tone at 1-MHz IF frequency around the high-band carrier and acquiring the calibration coefficients for gain and phase mismatches to cancel this tone at the low-band output. These coefficients are then used for the channel leakage measurement. The measured mid-band B1dB is +4.1 dBm. The measured NFs are 12.8 dB for the lower carrier and 12.9 dB for the higher carrier.

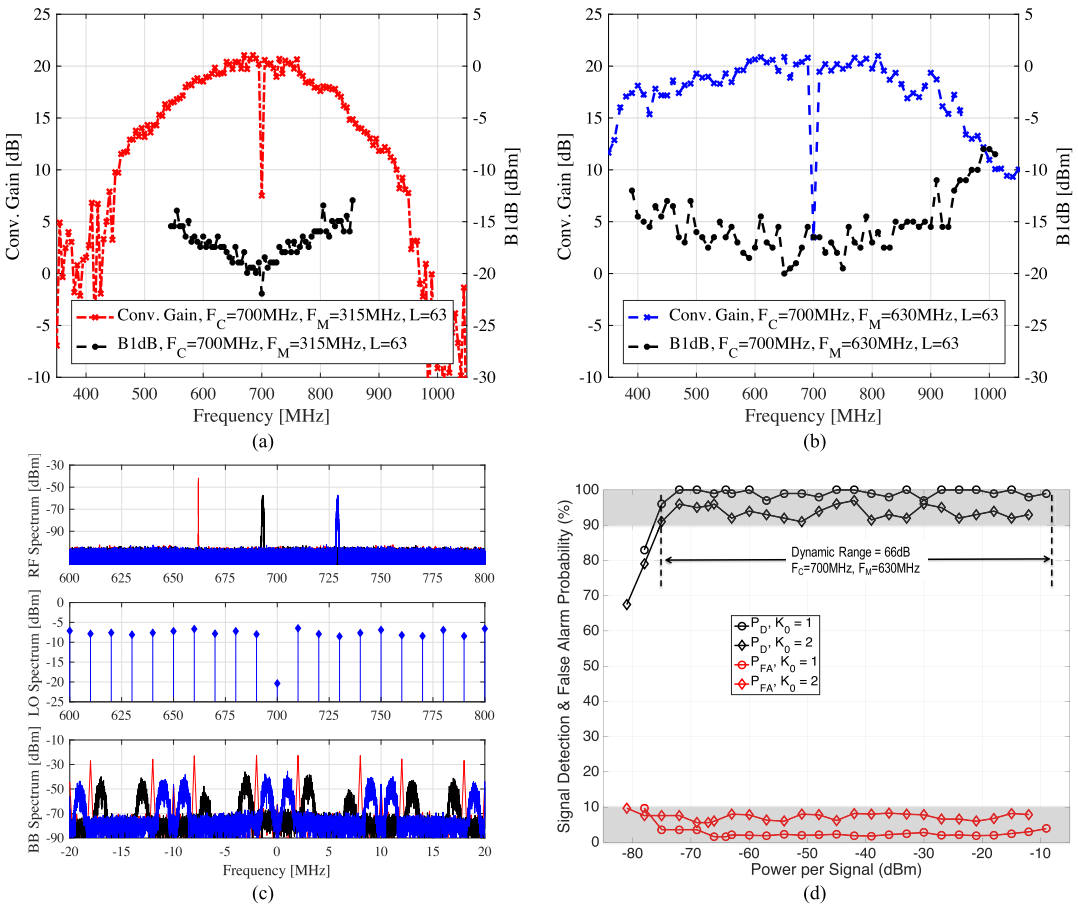


Fig. 24. Measurements for rapid CS spectrum scanning: conversion gain and swept-B1dB profiles using (a) $F_C = 700$ MHz, $F_M = 315$ MHz, and $L = 63$ and (b) $F_C = 700$ MHz, $F_M = 630$ MHz, and $L = 63$. (c) RF input, LO, and baseband output spectra when three signals are simultaneously converted with PN-modulated mixer clocks. (d) Detection probability P_D and probability of false alarm P_{FA} characteristics for one ($K_0 = 1$) and two ($K_0 = 2$) signals.

Fig. 21 shows the measurement results for the same high-linearity reception sub-mode but for a different F_M clock rate of 150 MHz. Fig. 21(a) shows the measured spurious responses, and (18) can be employed to estimate the spurious responses. For the responses at $(F_C - 9F_M)$ or 650 MHz, $(3F_C - 9F_M)$ or 750 MHz, and $(3F_C - 7F_M)$ or 1050 MHz, the spurious rejection is estimated to be 19, 29, and 26 dB, respectively, which agrees fairly well with the measured results. The receiver delivers a sideband rejection of 33.5 dB without calibration and 52.8 dB with calibration. Concurrently tuned input matching is measured at 550 and 850 MHz. The measured mid-band B1dB is +4.0 dBm.

Fig. 22(a) shows the measured normalized conversion gain and swept-B1dB profiles for **high-sensitivity dual-carrier reception** using $F_C = 700$ MHz and $F_M = 200$ MHz and combining the outputs from the LBs and the MFBs for noise cancellation. The canceled NFs are 4.6 dB for the lower carrier and 5.9 dB for the higher carrier. It degrades by 1.5 dB compared with the measured NFs for the single-carrier reception. This degradation is 0.5 dB worse than the expected 1-dB value (see Section III-D) probably due to the mismatches at the RF input. The measured mid-band B1dB is −8.4 dBm. The measured sideband rejection shown in Fig. 22(b) is 24 dB without calibration and improves to 51.7 dB with calibration.

Fig. 23 shows the plots of the measurements for the same high-sensitivity reception sub-mode but, now, for an F_M clock rate of 250 MHz with the responses measured at the high-band baseband outputs. Fig. 23(a) shows the measured spurious response. For the responses at $(3F_C - 5F_M)$ or 850 MHz and $(F_C - 7F_M)$ or 1050 MHz, the rejection can be estimated using (18) to be 23.5 and 16.9 dB, respectively. These numbers match fairly well with the measured results. Fig. 23(b) shows the measured conversion gain and channel leakage from the lower carrier. The receiver, in this case, has a sideband rejection of 20.8 dB without calibration and 53.0 dB with calibration. Fig. 23(c) shows the simultaneous tuned input impedance matching measured at 450 and 950 MHz. The measured mid-band B1dB is −7.6 dBm.

C. Rapid Compressive-Sampling Spectrum Scanning

For rapid CS spectrum scanning, only the MFBs are active, and the PRBS waveform synthesizer generates a PN sequence of length $L = 63$ running at F_M that modulates the RF clock at F_C. Depending on F_M, the conversion gain profile has different frequency spans, as shown in Fig. 24(a) and (b). Also shown are the swept-B1dB responses. In the measurement in Fig. 24(c), three signals are simultaneously down-converted to baseband. With CS DSP, the spectral locations of the

TABLE II
COMPARISON WITH SOA CONCURRENT RECEIVERS

	This Work		Agrawal	Zhu	Wu	Chen	Hwu	Soundstorm
	High-Linearity	High-Sensitivity	JSSC'18	JSSC'16	JSSC'19	JSSC'15	JSSC'15	ISSCC'13
Receiver Architecture	Multi-Branch Modulated-Mixer-Clock		Gain-Boosted N-Path Filter	Freq.-Translational Quadrature Hybrid	Harmonic-Selective FTNC	Current-Domain Signal Processing	Digital-Assisted Two-Step Conv.	Dual-Conv. w/ IF Filtering
RF Input	Differential		Differential	Single-Ended	Single-Ended	Differential	Single-Ended	Differential
RF Frequency (MHz)	300 ~ 1300		300 ~ 1400	600 ~ 2200	500 ~ 3000	500 ~ 3000	2000	700 ~ 2700
Max. Gain (dB)	53.2	46.7	38.5	48.0	42.0	50.0	37.0	45.0
Baseband BW (MHz)	5 ~ 33	7 ~ 33	1	6 ~ 35	10	1 ~ 30	35	2.5 ~ 10
No. of Clock Phases	4/4		4	8	32	4	4	4/8
CMOS Process	65nm GP		65nm	65nm GP	28nm	65nm GP	45nm	65nm
Supply Voltage	1.2V		N/R	1.1	N/R	1.2/2.5	1.0	1.45/1.8
Active Area (mm2)	1.8		0.31	1.1	1.2	7.8[2]	0.16	7.91[2]
	Single-Carrier Reception				**Single-Carrier Reception**			
NF DSB (dB)	10.8 ~ 13.6	2.7 ~ 4.4	3.4 ~ 4.9	0.9 ~ 1.8	2.4 ~ 5.0	3.8 ~ 4.7	3.6 ~ 3.8	4.5
IB IIP3 (dBm)	-6.9	-12.1	-26.0	-12.5	N/R	-28.0	-13.7	-15.5
OB IIP3 (dBm)	+16.1	+8.0	+10.0	+8.0	+4.0	+10.0	+2.8	+2.4
Offset /Baseband BW (MHz)	120/5	175/7	150/1[1]	80/10	50/10	200/10[1]	N/R	100/2.5[1]
B1dB (dBm)	+6.2	-1.3	-11.8	-10.0	-10.0	-1.0	N/R	-15.5
Offset /Baseband BW (MHz)	200/5	320/7	N.R.	200/10	70/10	N/R		100/2.5[1]
Analog Power (mW)	12.4	39.4	25.5	95.0	21.0	96.0	12.0	155.0
Clock Power (mW/GHz)	5.2	10.4	N/R	10.5	N/R	56.0	N/R	N/R
	Inter-Band CA				**Harmonic-Based CA**	**Intra-Band CA**		
# of Carriers	2		2	2	3	3	2	2
Carrier Separation (MHz)	200 ~ 600		< 700	< 1500	N/A	< 100	< 70	< 70
NF DSB (dB)	12.8 ~ 12.9	4.6 ~ 5.9	3.4 ~ 4.9	1.3 ~ 3.2	2.4 ~ 5.0	4.8	3.6 ~ 3.8	4.5
Mid-Band B1dB (dBm)	+4.0	-8.4	-11.8	-10.0	-10.0	-9.0	N/R	-15.5
Sideband Rejection (dB)	31.7 (uncal)	24.0 (uncal)	35	N/A	45 (uncal)	N/R	30 (uncal)	35 (uncal)
	48.2 (cal)	51.7dB (cal)			80 (cal)		70 (cal)	60 (cal)
Analog Power (mW)	24.8	78.8	25.5	96.0	21.0	168.0	12.0	290.0
Clock Power (mW/GHz) F_C Clock	8.4	16.8	N/R	10.5	N/R	56.0	N/R	N/R
Clock Power (mW/GHz) F_M Clock	6.0	12.0						

N/R = Not Reported. N/A = Not Applicable. 1. Estimated from the reported measurement data. 2. Area including frequency synthesizers.

signals at the input are rapidly found. Fig. 24(d) shows the measured signal-detection probability P_D and false-alarm probability P_{FA}; the sensitivity for $P_D > 90\%$ and $P_{FA} < 10\%$ is -75 dBm, and the dynamic range is 66 dB over a 630-MHz bandwidth with 75 samples per measurements. The receiver can detect up to two signals within 0.71 μs and consumes 18.5 nJ per detected signal.

VI. DISCUSSION

The multi-branch MMC architecture is unique in that a single device can perform single-carrier reception, dual-carrier reception, as well as rapid CS spectrum scanning. The receiver performance is summarized in Tables II and III.

A. Comparison With Concurrent Receivers

Table II compares the MMC receiver in single- and dual-carrier reception modes with other SoA concurrent inter-band receivers. We also included some SoA concurrent intra-band receivers even though their design challenges are quite different. For single-carrier reception, the receiver in the high-linearity reception mode delivers excellent in-band and OB IIP3, as well as outstanding B1dB, with low power consumption for the offered baseband bandwidth. In the high-sensitivity mode, it achieves a minimum of 2.7 dB NF while still delivering good IIP3 and excellent B1dB.

For concurrent, dual-carrier reception, the MMC receiver offers narrow-band impedance matching at the two desired frequencies only, and reflects OB signals, resulting in improved B1dB operation compared with other architectures. With a single-point calibration, the receiver achieves around 50-dB sideband rejection, which can be greatly improved using more complicated techniques.

TABLE III
COMPARISON WITH SOA CS SPECTRUM SCANNERS

	This Work	Yazicigil JSSC'15	Adam JSSC'17	Haque JSSC'18
Design Type	Multi-Branch MMC	QAIC	MWC	DRF2IC
Number of Detected Signals	2	3	4	6
Number of Branches	4	16	5	4
Scanning Frequency (MHz)	385 ~ 1015	2700 ~ 3700	0 ~ 900	635 ~ 2840
RFFE Chip Power (mW)	24.8	80	704	58.5
PRBS Length	63	127	740	127
PRBS Clock Frequency (MHz)	630	1270	7400	1270
Scan Time (us)	0.71	4.4	1.2	1.2
Energy per Scan (nJ)	36.9	528	1076	132
Energy per Detected Signal (nJ)	18.5	176	269	22
Sensitivity (dBm)	-75	N/R	N/R	-71
Dynamic Range (dB)	66	30	61	66

B. Comparison With SoA CS Spectrum Scanners

Compared with other SoA CS scanners in Table III [8], [36], [37], the presented work delivers the best-reported detection sensitivity, scan time, and energy consumption. Though this work can only detect two signals, more signals can be detected with more PN sequences [8] or time-segmented techniques [38].

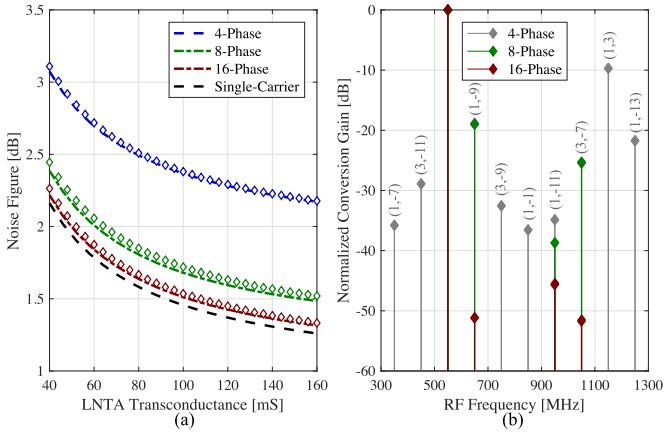


Fig. 25. Studies for higher-order clock modulation using schematic-level behavioral models with different numbers of F_M clock phases assuming $F_C = 700$ MHz and $F_M = 150$ MHz. (a) Simulated ($\diamond$) and analytical (–) NFs versus LNTA transconductance. (b) Simulated spurious response at the low-band output.

C. Future Improvements

To improve the receiver's spurious responses, higher-order mixer-clock modulation can be used in a future design, where the digital mixing of the F_C and F_M clocks can still be used with harmonic-rejection baseband circuits. For example, eight-phase F_M clock modulation can help to suppress higher-order harmonics, specifically the third and fifth F_M harmonics. As shown in Fig. 25(b), the receiver's spurious responses improve significantly by using eight-phase clock modulation. The responses at 650 and 1050 MHz stem from the $(F_C - 9F_M)$ and $(3F_C - 9F_M)$ responses and cannot be suppressed with an eight-phase clock. With 16-phase F_M clock modulation, these responses can be suppressed.

More clock phases do not only reduce spurious responses but also improve the receiver's noise performance since the noise now is being folded back from fewer intermodulation products of the higher-order F_C and F_M harmonics. Following the same analysis methodology as in Section III-D, the receiver's noise factor can be derived as:

$$F_{\mathrm{RX}} = \left(1 + \frac{\gamma}{G_{m,\mathrm{LNTA}} R_S}\right) \cdot \frac{1}{\mathrm{sinc}^2(\pi/N)} \cdot \frac{1}{\mathrm{sinc}^2(\pi/4)} \quad (20)$$

where N is the number of F_M clock phases; the multiplication factor of $\mathrm{sinc}^{-2}(\pi/N)$ is the noise folding factor [2]. Assuming the same numbers listed in Section III-D, the NFs employing eight-phase and 16-phase F_M clock phases can be calculated as 1.81 and 1.64 dB, respectively. The NF for single-carrier reception is 1.58 dB. Note that as the number of clock phases increases, more baseband TIAs are needed. For example, for four-phase F_C clocks and four-phase F_M clocks, $(4/2) \times (4/2) = 4$ TIAs are needed. If the number of F_M clock phases increases from 4 to 16 by a factor of four, then $(4/2) \times (16/2) = 16$ TIAs are needed. For current-mode front-end circuits with op-amp-based TIAs, to maintain the same noise performance, the op-amps can be scaled down by a factor of four, and the feedback resistance can be scaled up by the same amount [19], [39]. Therefore, an increased number of clock phases do not increase the baseband power consumption or its silicon area to the first order. However, clock generation and distribution gets more complicated, which might result in increased LO power consumption and silicon area.

From another perspective, to achieve the same noise performance as single-carrier reception, the needed LNTA transconductance can be reduced due to higher-order clock modulation. For example, to achieve a 2-dB NF, the LNTA transconductance needs to be 47 mS for single-carrier reception. To achieve the same 2-dB NF, it is impractical to use four-phase clock modulation since it will result in a very large transconductance. With higher-order clock modulation, the needed LNTA transconductances only need to be 60 and 50 mS for eight- and 16-phase modulations, respectively.

VII. Conclusion

This article proposed a receiver architecture that explores mixer clock modulation in its LNTA and mixer-first branches to unify three different operations in a single device. Concurrent dual-carrier reception from $(F_C \pm F_M)$ is achieved by modulating the RF clock at F_C with a CW source at F_M. It offers a narrowband matched RF interface only at the frequencies of interest while reflecting OB signals, which greatly improves the OB linearity. For rapid CS spectrum scanning, the RF clock is modulated by a PN source at F_M, resulting in wideband conversion-gain profiles. Assisted by CS DSP, the receiver can detect a few signals over a wide RF span. Disabling the clock modulation simply reverts the receiver back to a standard FTNC receiver for single-carrier reception with excellent OB linearity.

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Dr. Kinget was an elected member of the IEEE Solid-State Circuits Adcom from 2011 to 2016. He has served as a member for the Technical Program Committee of the IEEE Custom Integrated Circuits Conference from 2000 to 2005 and 2016 to 2018, the Symposium on VLSI Circuits from 2003 to 2006, the European Solid-State Circuits Conference from 2005 to 2010, and the International Solid-State Circuits Conference from 2005 to 2012. His research group has received funding from the National Science Foundation, Semiconductor Research Corporation, the Department of Energy (ARPA-E), and the Department of Defense (DARPA) and an IBM Faculty Award. It has further received in-kind and grant support from several of the major semiconductor companies. He was an inaugural recipient of the IEEE Solid-State Circuits Society Innovative Education Award in 2020. He was a co-recipient of several awards, including the Best Student Paper Award-1st Place at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, the First Prize at the 2009 Vodafone Americas Foundation Wireless Innovation Challenge, the Best Student Demo Award at the 2011 ACM Conference on Embedded Networked Sensor Systems (ACM SenSys), the 2011 IEEE Communications Society Award for Advances in Communications for an outstanding article in any IEEE Communications Society's publication in the past 15 years, the First Prize ($100K) at the 2012 Interdigital Wireless Innovation Challenge (I2C), the Best Student Paper Award-2nd Place at the 2015 IEEE RFIC Symposium, the Best Poster Award at the 2015 IEEE Custom Integrated Circuits Conference (CICC), and the Best Student Paper Award-3rd Place at the 2018 IEEE RFIC Symposium. He was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2003 to 2007 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2008 to 2009. He was an IEEE Distinguished Lecturer of the Solid-State Circuits Society from 2009 to 2010 and 2015 to 2017.