A 0.3-to-1.3GHz Multi-Branch Receiver with Modulated Mixer Clocks for Concurrent Dual-Carrier Reception and Rapid Compressive-Sampling Spectrum Scanning

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***Abstract* — A flexible RF receiver is introduced that uniquely uses CW-modulated clocks for the down-conversion mixers in its mixer-first and low-noise transconductance branches, thereby enabling tuned matching and reception concurrently at two RF carriers. Turning off the modulation reverts the receiver back to single-carrier operation, whereas using PN sequences to modulate the mixer clocks enables rapid, wideband compressive-sampling spectrum scanning. All three functions are accomplished within a single unified architecture. A prototype of the multi-branch modulated-mixer-clock receiver was developed in 65nm CMOS and operates from 0.3 to 1.3GHz. For single-carrier reception, the receiver delivers 15MHz RF bandwidth, 42dB conversion gain, 3.3dB NF, +3.3dBm B1dB, and +12.2dBm OB-IIP3. Concurrent dual-carrier reception at 500MHz and 900MHz offers -8.4dBm B1dB and <6dB NF. In rapid CS spectrum scanning mode, the receiver achieves 66dB dynamic range with -75dBm sensitivity over a 630MHz RF span within 0.71us and consumes 18.5nJ per detected signal.**

I. Introduction

Ever-increasing wireless throughput demands drive the need to perform concurrent signal reception from multiple carriers that are hundreds of MHz apart. Different receiver architectures have been proposed to address this challenge. The frequency-translational quadrature-hybrid receiver [1] can aggregate two carriers with a low NF by introducing an off-chip hybrid coupler. Its broadband impedance matching offers no selectivity at RF and thus limits out-of-band (OB) linearity. The gain-boosted N-path filter (NPF) receiver [2] aggregates two carriers and offers RF selectivity by placing two NPF filters in feedback. However, the active feedback limits both in-band (IB) and OB linearity. The FTNC receiver [3] offers a tuned RF impedance and good OB linearity by translating the baseband impedance to RF with its mixer-first branch. Its input impedance is 50Ω inside the desired band but low outside, making the parallel combination of multiple FTNC receivers impractical for multi-carrier reception.

In this paper, we explore how modulating the driving clocks of the down-conversion mixers offers unique abilities to a flexible multi-branch modulated-mixer-clock (MMC) receiver. It leverages several advantages of aforementioned receivers and additionally provides a rapid spectrum scanning feature [4]. With a continuous-wave (CW) clock modulation, the lowpass baseband impedance in the mixer-first branches (Fig. 1) is translated as a tuned response at F_{RF1} and F_{RF2}, offering RF selectivity, good OB linearity, and concurrent reception from these two RF carriers. Two LNTA branches are incorporated into the system to offer noise cancellation

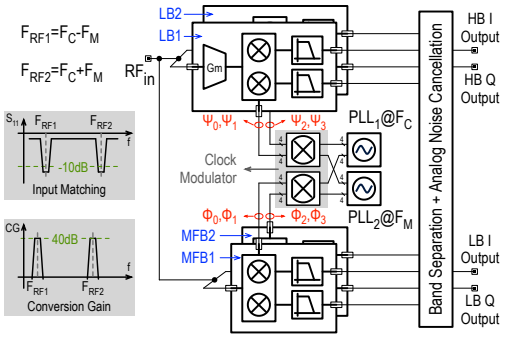


Fig. 1. Diagram of the proposed multi-branch modulated-mixer-clock receiver

for better noise performance. With a pseudo-noise (PN) clock modulation, a widespread conversion gain profile is realized that enables the rapid compressive-sampling (CS) spectrum scanning feature with a superior combination of detection sensitivity and energy consumption. Without any clock modulation, the receiver is a single-carrier receiver and delivers excellent B1dB and OB-IIP_3.

II. Multi-Branch MMC Receiver Architecture

Four pairs of tri-level-modulated mixer clocks φ_0 to φ_3 are derived from two 4-phase 25% non-overlapping clocks at F_C and F_M with a digital clock modulator by either flipping, or not flipping, the polarity of the input clocks, or holding both outputs low (Figs. 1 and 2). When flipping the RF clock at a clock rate of F_M, the F_C tone in the RF clock is moved to two separate tones at $F_C \pm F_M$. When one modulated clock is low, one of the other three modulated outputs is switching. While the F_C and F_M clocks do not need to be synchronized, the four clocks φ_0 to φ_3 are still guaranteed to be non-overlapping in the time domain and they have linearly-independent spectra.

Applying φ_0 to φ_3 to the mixer-first branches (MFB_1 and MFB_2 in Fig. 1) translates the lowpass baseband impedance to F_{RF1} and F_{RF2} as dual-band tuned input matching. Meanwhile, the mixers concurrently down-convert the RF input signals at F_{RF1} and F_{RF2} to linearly independent baseband outputs. Simple addition and subtraction separate the I/Q components for each RF carriers, as shown in Fig. 2. Short clock pulses can occur that are potentially too short to turn on the mixer switches; however, these pulses carry little energy and mainly contribute to higher-order inter-mixing components that have significantly lower power levels and do not affect the main operation at $F_C \pm F_M$.

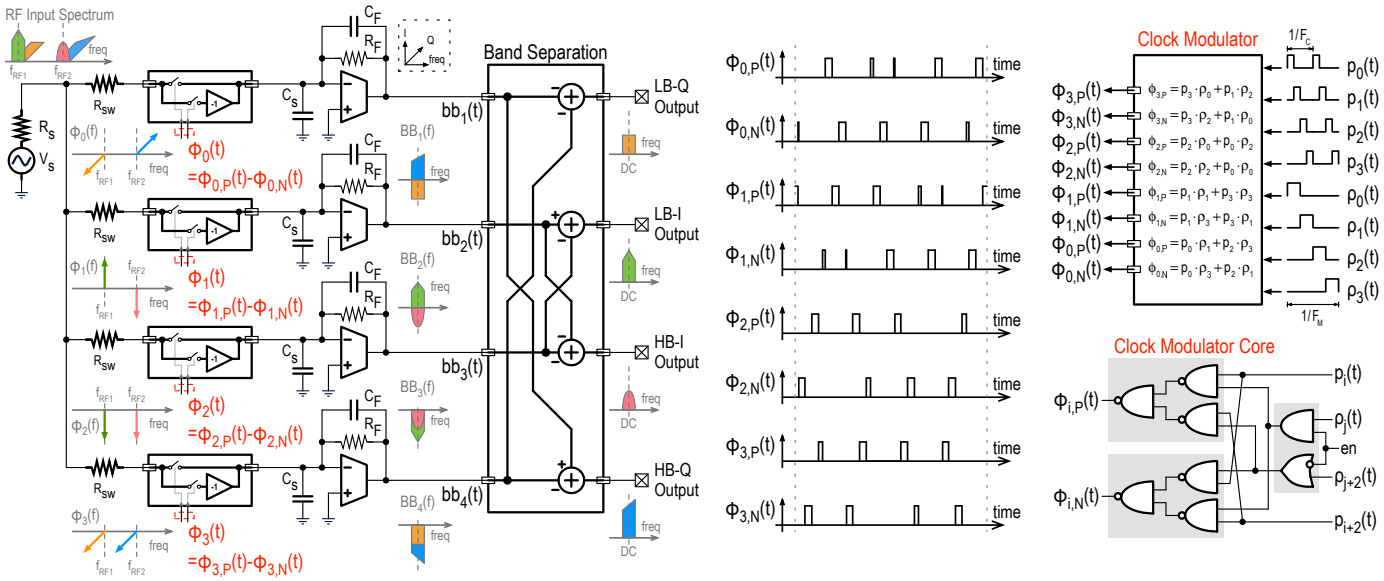


Fig. 2. Conceptual diagram for the operation of the mixer-clock modulation and the two mixer-first branches MFB_1 and MFB_2. A single-ended version is shown, but the circuit implementation is fully differential. Tri-level modulations of an RF clock (at $F_C = (F_{RF1} + F_{RF2})/2$) and a modulation clock (at $F_M = (F_{RF2} - F_{RF1})/2$) results in concurrent input matching at F_{RF1} and F_{RF2} and concurrent reception from these two frequencies.

The addition of two LNTA branches (LB_1 and LB_2 in Fig. 1) driven by the modulated clocks Ψ_0 to Ψ_3 allows for the noise cancellation [3] and improves system's NF. These two groups of non-overlapping modulated clocks $\Psi_{0,1}$ and $\Psi_{2,3}$ are generated with 50% 4-phase F_M clocks modulated with the 25% 4-phase RF clocks at F_C.

III. Multi-Branch MMC Receiver Implementation

The fully-differential MMC receiver prototype shown in Fig. 3 with bias and control circuitry has been implemented on 1.8mm^2 in 65nm CMOS and operates from a 1.2V supply. Each LNTA branch comprises a cascoded common-source (C-S) LNTA, differential passive mixers, and two-stage Miller-compensated TIAs. The cascoded C-S LNTA shown in Fig. 4a provides 88mS transconductance and consumes 13mA. The passive mixers use transmission gates. The baseband TIAs are implemented with 4-bit programmable feedback resistance and 5-bit feedback capacitance for gain and bandwidth control.

Each mixer-first branch consists of RF switches, baseband folded-cascode TIAs, and Cherry-Hooper voltage buffers. The RF switches are placed in a floating-body configuration for small OFF capacitance and biased at a 0.2V source voltage for low ON resistance. The Cherry-Hooper voltage buffers in Fig. 4b have 6-bit programmable degeneration resistance for linearity control and 2-bit programmable feedback resistance for gain control. The baseband TIAs in Fig. 4c and the voltage buffers together consume 4.92mA per branch.

The clock path contains clock dividers, non-overlapping clock generators, a PRBS waveform synthesizer, and two clock modulators. The modulator cores in Fig. 4d are based on custom high-speed NAND and NOR gates. The PRBS synthesizer can generate shift-register-based and LFSR-based PN sequences with various lengths. The LNTA and the mixer-first branches can operate independently with different clock sources or can be driven synchronously with the same source.

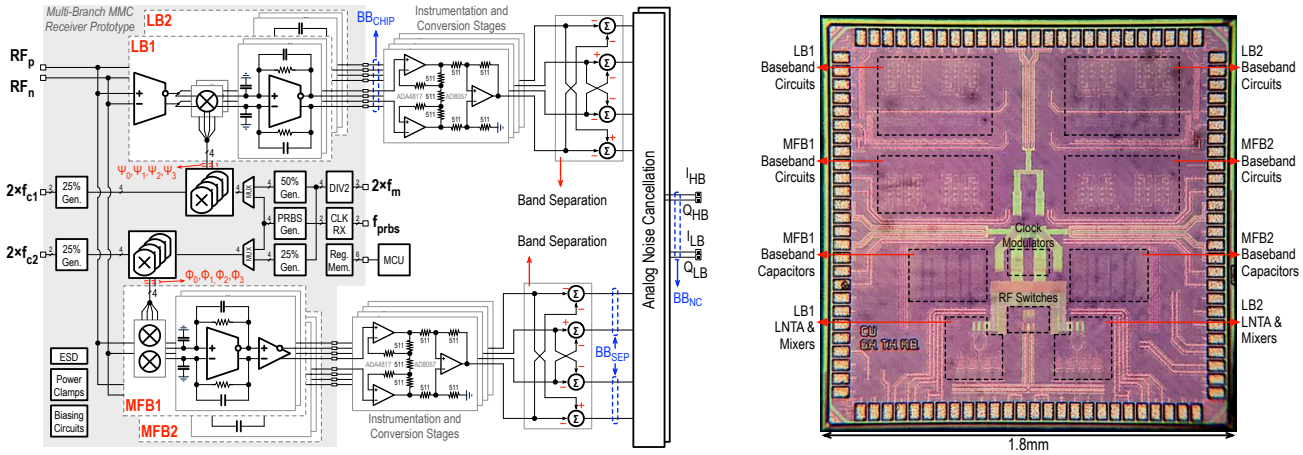


Fig. 3. The multi-branch modulated-mixer-clock receiver system architecture and the 65nm CMOS die micrograph. The fully-differential receiver prototype occupies an active area of 1.8mm^2 and operates from a 1.2V power supply.

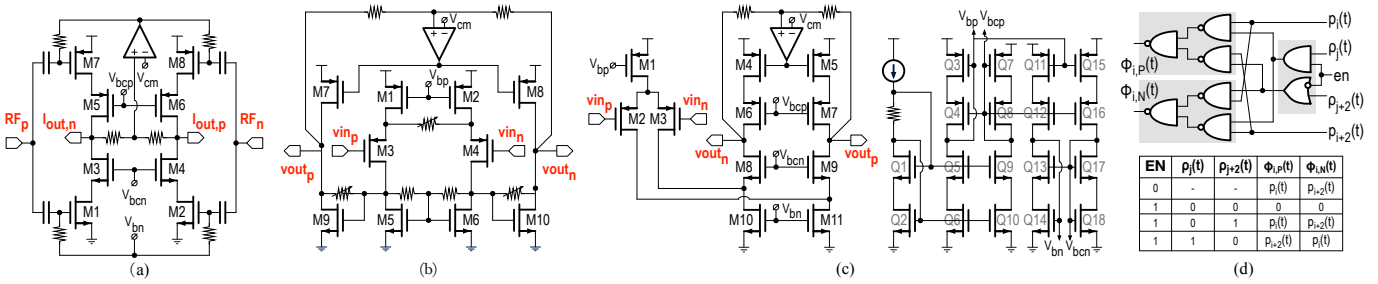


Fig. 4. Key circuit blocks of the MMC receiver, including (a) cascoded common-source LNTAs, (b) Cherry-Hooper voltage amplifiers, (c) folded-cascode TIA OTA core with biasing circuitry, and (d) clock modulator cores and its truth table.

IV. Experimental Results

The tuned input impedance matching in the MMC receiver offers OB linearity improvements over a broadband matched receiver (like [1]). Fig. 5 shows the swept-B1dB and the input matching, S_{11}, measurements. To provide a baseline, the performance with broadband matching is first measured, where the RF switches in the mixer-first branches are disabled and the RF input is resistively terminated. Then, the mixer-first termination is employed and the MMC receiver now has a tuned impedance matching, resulting in a reduction of the voltage swing from the OB blocking signal at the RF input. Therefore, the OB linearity is improved by up to 10dB in the single-carrier reception mode and by more than 5dB in the concurrent dual-carrier reception mode. We estimate the routing and switch resistance in our prototype to be around 13Ω, resulting in a -3dB and -5dB S_{11} floor in both modes. Better OB matching and further improved linearity are expected with better layout for less routing resistance and advanced technologies for less switch resistance.

In the single-carrier reception mode, only the LB_1 branch and the MFB_1 branch are active and the clock modulation is disabled. The RF clock can be swept between 300MHz and 1300MHz; the conversion gain can be programmable from 25dB to 46.7dB, and the baseband bandwidth can be set from 7MHz to 33MHz. The receiver has 42dB conversion gain at 700MHz with a 15MHz RF bandwidth and +3.3dBm B1dB for a 350MHz offset (Fig. 6a). The measured OB-IIP3 is +12.2dBm with tones at 175MHz and 349MHz offsets. The measured NF is 3.3dB at 700MHz after cancellation.

For the concurrent dual-carrier reception, both LNTA and mixer-first branches are active and the clock modulation is enabled. The modulation clock can be set from 100MHz to 300MHz, thus supporting concurrent dual-carrier reception with a carrier separation from 200MHz to 600MHz. The conversion gain to the chip baseband outputs (BB_{CHIP} in Fig. 3) decreases by 3dB since the clock modulation bifurcates the RF clock to F_{RF1} and F_{RF2}. Concurrent down-conversion is shown with different modulation clock rates in Fig. 6b. For

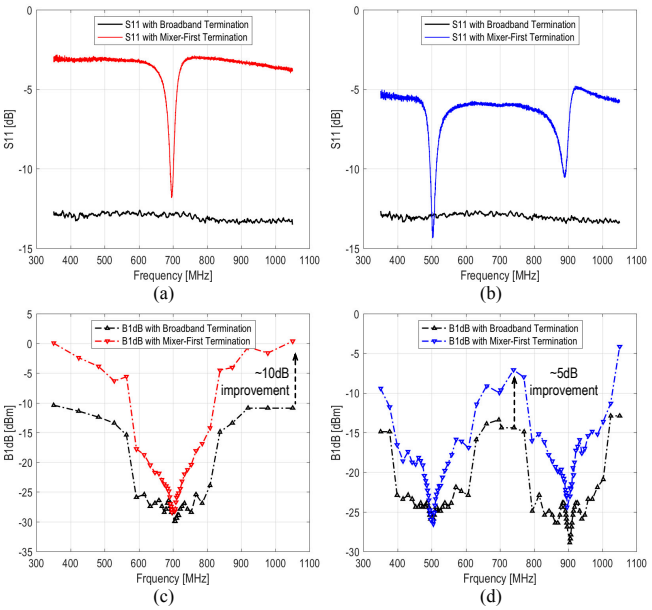


Fig. 5. A comparison of return loss [(a), (b)] and swept-B1dB performance [(c), (d)] of the MMC receiver for a broadband resistive termination versus a tuned mixer-first termination in the single-carrier reception mode at 700MHz and in the concurrent dual-carrier reception mode at 700MHz ± 200MHz.

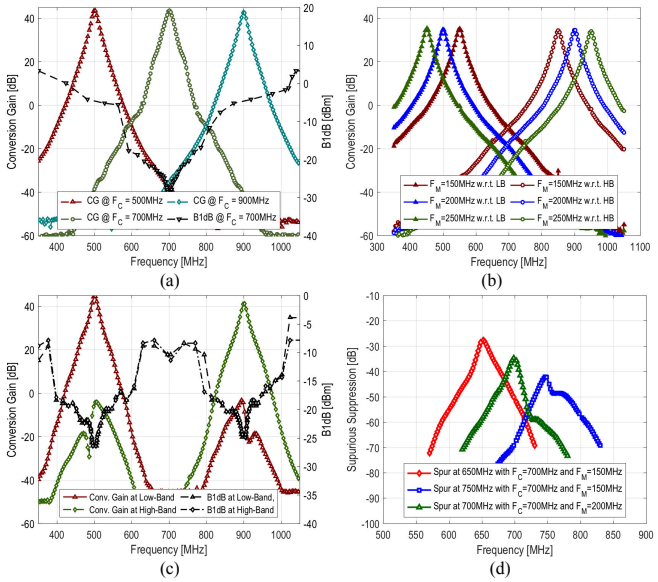
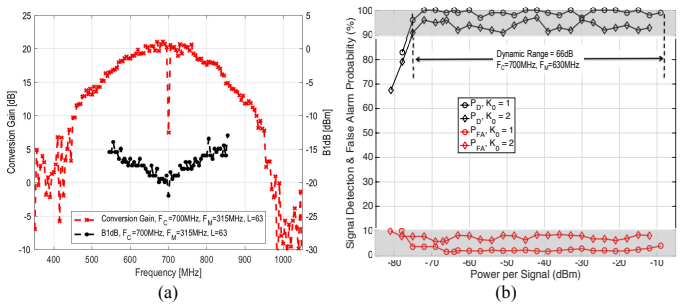


Fig. 6. Measured receiver performance: (a) conversion gain and B1dB in the single-carrier reception mode, (b) demonstration of concurrent dual-carrier reception at BB_{NC} with varying F_M, (c) conversion gain and B1dB at BB_{NC} from 500MHz and 900MHz in the concurrent dual-carrier reception, and (d) spurious suppression at BB_{NC} in the concurrent dual-carrier reception mode.



(a) (b)

Fig. 7. Measurements for rapid CS spectrum scanning: (a) conversion gain and B1dB profiles with F_M = 315MHz and length-63 sequences; (b) P_D and P_{FA} vs. input power level for detecting one and two ($K_0 = 1, 2$) input signals.

dual-carrier reception at 500MHz and 900MHz, the measured mid-band B1dB is better than -10dBm. After band separation, the conversion gain increases by 3dB and is the same as the conversion gain under the single-carrier reception mode. The rejection between two bands is 46dB after standard calibration for gain and delay mismatches. The measured NF at BB_{NC} (Fig. 3) is 4.6dB at 500MHz and 5.9dB at 900MHz, respectively. Spurious responses exist in the system due to the higher-order inter-mixing components in the modulated clocks. But they have significantly lower gain, and >30dB spurious suppression is observed in Fig. 6d. More suppression is expected with higher-order clocking systems [3].

In the rapid CS spectrum scanning mode, only the mixer-first branches are active. The mixer-clock modulation is enabled and the RF clock F_C at 700MHz is modulated with a maximal-length PRBS sequence of length L=63 clocked at F_M = 630MHz, resulting in a widespread conversion gain as shown in Fig. 7a. The RF input span extends from $(F_C - F_M/2)$ to $(F_C + F_M/2)$ and signals from all L channels are simultaneously down-converted to baseband. With CS DSP, the spectral locations of a few strong signals within the input span can be rapidly found. The measured sensitivity for a signal detection probability $P_D > 90\%$ and a false alarm probability $P_{FA} < 10\%$ is -75dBm and the dynamic range is 66dB over a 630MHz bandwidth with 75 samples per measurement. More signals can be detected with more sequences [4].

V. Comparison to the State of the Art

The performance of the multi-branch MMC receiver is summarized and compared in Table 1. In the single-carrier reception mode, the MMC receiver delivers excellent B1dB and OB-IIP_3 thanks to the tuned impedance matching and the up-front filtering. The IB-IIP_3 is slightly better than [1] but it is 14dB better than [2]. In the concurrent dual-carrier reception mode, the MMC receiver delivers excellent B1dB. Though [2] consumes less analog power, the MMC receiver offers at least 6x more bandwidth. In the rapid CS spectrum scanning mode, the MMC receiver delivers superior detection sensitivity and energy consumption when compared to other published CS spectrum scanner [4].

Table 1. Multi-branch MMC receiver performance summary and comparison with other concurrent dual-carrier receiver and CS spectrum scanner

Metric	This Work	[1]	[4]	[2]	[3]
Design Type	MMC	FTQH	DRF2IC	GB-NPF	FTNC
RF Frequency [MHz]	300 ~ 1300	600 ~ 2200	600 ~ 3000	300 ~ 1400	100 ~ 3300
Max. Gain [dB]	46.7	48	41.5	38.5	N/R
BB Bandwidth [MHz]	7 ~ 33	6 ~ 35	20	1	3
Number of Clock Phases	4	8	4	4	8
Clock Power [mW/GHz]	12.0	10.5	N/R	N/R	8.0
CMOS Technology	65nm	65nm	65nm	65nm	28nm
Active Area [mm2]	1.8	1.1	0.56	0.31	5.2
Single-Carrier Reception Mode					
Noise Figure [dB]	2.7 ~ 4.4	0.9 ~ 1.8	3.6	3.4 ~ 4.9	1.8 ~ 3.8
IB-IIP3 [dBm]	-12.1	-12.5	-11.0	-26.0	N/R
OB-IIP3 [dBm]	+12.2	+8	+4	+7.5	+11.5
B1dB-CP [dBm]	+3.3	-10	-2	-11.8	-2.5
Analog Power [mW]	39.4	96.0	46.5	25.5	36.0
Concurrent Dual-Carrier Reception Mode					
Noise Figure [dB]	4.6 ~ 5.9	1.3 ~ 3.2	N/A	3.4 ~ 4.9	N/A
B1dB-CP [dBm]	-8.4	-10		-11.8	
Analog Power [mW]	78.8	96.0		25.5	
Rapid CS Spectrum Scanning Mode					
Detection Range [MHz]	385 ~ 1015	N/A	635 ~ 2840	N/A	N/A
Number of Branches	4		4		
Scan Time [us]	0.71		1.2		
Enery per Scan [nJ]	36.9		132		
Enery per Detected Signal [nJ]	18.5		22.0		
Sensitity [dBm]	-75		-71		
Dynamic Range[dB]	66		66		
N/R = Not Reported			N/A = Not Applicable		

VI. Conclusions

The multi-branch MMC receiver presented in this paper offers a single unified architecture for high-performance single-carrier and concurrent dual-carrier reception, and rapid CS spectrum scanning by modulating the mixer clocks. With a CW clock modulation, the receiver realizes dual-band tuned RF input matching for excellent OB linearity and enables concurrent dual-carrier reception. With a PN clock modulation, the receiver widely spreads the conversion gain profile and can detect a few strong signals within a wide RF span. These features render the proposed multi-branch MMC receiver a promising front-end solution for great reconfigurabilities and tunabilities.

Acknowledgment

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