

A Technology/Circuit Co-design Framework for Emerging Reconfigurable Devices

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Abstract—Reconfigurable devices are gaining increasing attention as a viable alternative and complementary solution to the prevalent CMOS technology. In this paper, we develop a device and circuit-level co-design framework for evaluating and exploring the performance of emerging reconfigurable devices. We use reconfigurable FET as a case study by creating a cell library and performing logic synthesis and physical design to investigate the impact of device-level parameters, such as supply voltage and nanowire diameter, on the circuit-level performance. Results show that optimal device-level parameters exist, whose values are highly dependent on the overall circuit-level performance, such as energy, delay, area, or energy-delay-area product.

Keywords—reconfigurable FET, synthesis, device/circuit co-design, delay, area, energy, energy-delay product

I. INTRODUCTION

CMOS technology is currently the mainstream chip manufacturing technology, which has been strictly following Moore's law for decades and continuously evolving. Due to the transistor scaling challenge at sub-5nm technology node, it is difficult to design high-performance chips with low energy consumption and a compact area [1]. The reconfigurable field effect transistor (RFET) is an emerging multi-gate device, which can change the polarity of the device through an additional voltage-controlled gate, making it switch between an N-type and a P-type FET [2, 3]. This characteristic allows RFET to achieve a logic-rich functionality with a highly compact area and makes RFETs a potential solution to augment or even replace CMOS [4].

Over the years, significant progress has been made in RFET research, particularly at device and circuit levels. Many physical structures can realize RFET, such as silicon nanowires (SiNW) [2, 5], germanium nanowires (GeNW) [6], graphene field effect transistors [7], and spin-based devices [8]. All these devices have reconfigurable characteristics and are capable of making logic gates with fewer transistors, potentially leading to a smaller circuit area and even lower circuit delay. At the circuit level, logic circuits based on RFET reconfigurable gates have demonstrated significant advantages in terms of area, delay, and energy consumption [9, 10]. In addition, several RFET-based

logic cell libraries, including physical layout designs, have been proposed to reduce cell area significantly [11], and complete PDK files have been developed [12]. Synthesis flow based on these advancements has continued to prove the advantages of RFET in large-scale circuit design [13-15].

Although these works have made great progress, most of them only study the physical model of RFET separately from the circuit design and synthesis. To truly understand the potential benefits of emerging RFET technologies, it is critical to consider device and circuit design simultaneously through device/circuit co-design. A faster device does not necessarily guarantee a better circuit performance, because a circuit using such a device could be limited by footprint area or power consumption. It may thus be misleading to optimize individual devices based solely on intrinsic metrics without considering their circuit-level implications and goals. For example, if the design goal is a high-speed circuit, the current-carrying capacity of the nanowire must be improved. Therefore, a larger diameter with a higher supply voltage is needed, but a larger diameter increases the cell area, which increases the chip area and interconnect length.

In this paper, we develop a comprehensive cell library based on various physical parameters of RFET and use it as the input to the logic synthesis and physical design for a variety of circuit benchmarks. In addition, we will explore key device parameters of RFETs, including supply voltage, nanotube diameter, and cell area, and how they interact with different circuit applications under different design scenarios. The major contributions of this work are highlighted below.

- We design a comprehensive set of logic cell libraries using RFET physical models.
- We develop a technology/circuit co-design framework for evaluating and exploring the performance of emerging reconfigurable devices.
- We perform a large design space exploration for RFET-based circuits to show valuable insights to device technologists for designing more suitable device parameters for optimal circuit-level performance under various application scenarios.

II. MODELING APPROACH

As shown in Fig. 1, REFT can switch between N-type and P-type and maintain a high degree of symmetry, which makes logic gates composed of RFETs use fewer transistors to achieve the same function compared to CMOS. Fig. 2 shows an example of NAND gates and XOR gates based on RFETs that use fewer transistors than gates made of CMOS. More importantly, the gate formed by REFT can be reconfigured into a logic gate with other functions, for example, a NAND gate can be used as a NOR and a minority (MIN) gate at the same time [9].

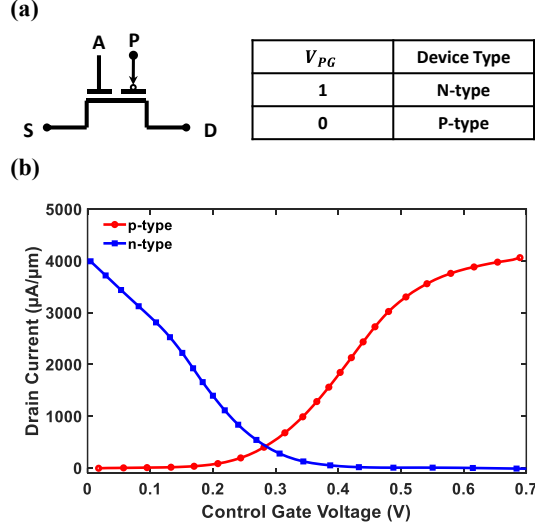


Fig. 1. (a) RFET device symbol, which can be switched between N-type and P-type by applying different gate voltage on the program gate. (b) Drain current versus control gate voltage for N- and P-type RFETs [12].

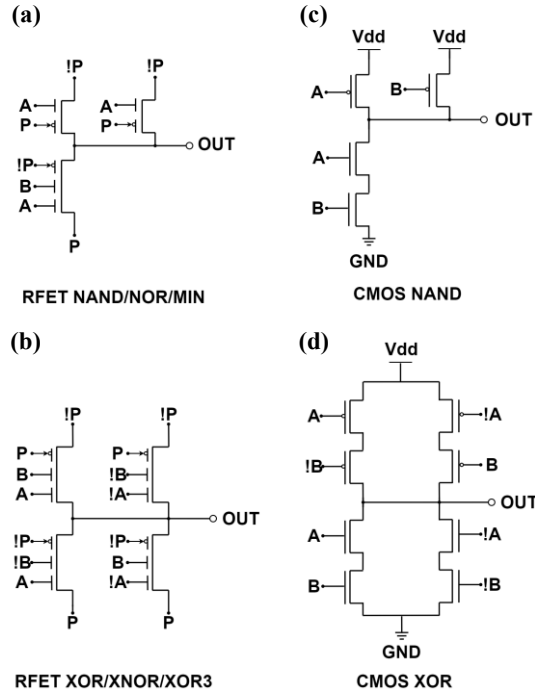


Fig. 2. (a) NAND and (b) XOR gates consisting of RFETs, which also can be reconfigured into NOR and MIN by applying different voltages. (c) and (d) are counterpart logic gates based on CMOS that use more transistors [9].

A. Cell-Level Modeling

To enable a large design space exploration, we develop a comprehensive set of logic cell libraries using emerging RFETs. First, we established the logic gate layout design rules of RFET based on the ASAP 7nm PDK [16, 17] to calculate the area of each logic gate. An example of NOR gate is shown in Fig. 3 when the nanowire diameter is 7nm. We use the basic cell based on 12 silicon nanowires, which are composed of four layers with three nanotubes in each layer. Since the diameter of the nanotube directly affects the height of the cell, we obtained a linear relationship between the area and the nanotube through layout design rules in [16]. Secondly, we extract the timing information based on the electrical properties of RFETs. Many experimental and simulation-based research provides solid

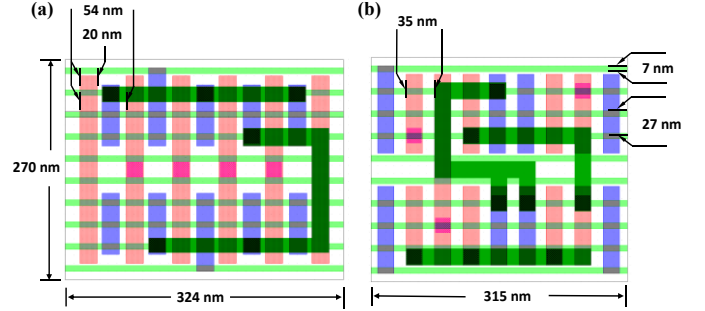


Fig. 3. Layout of a NOR gate using (a) CMOS and (b) RFET, where the light green represents fins/nanotubes and the light red represents input gates.

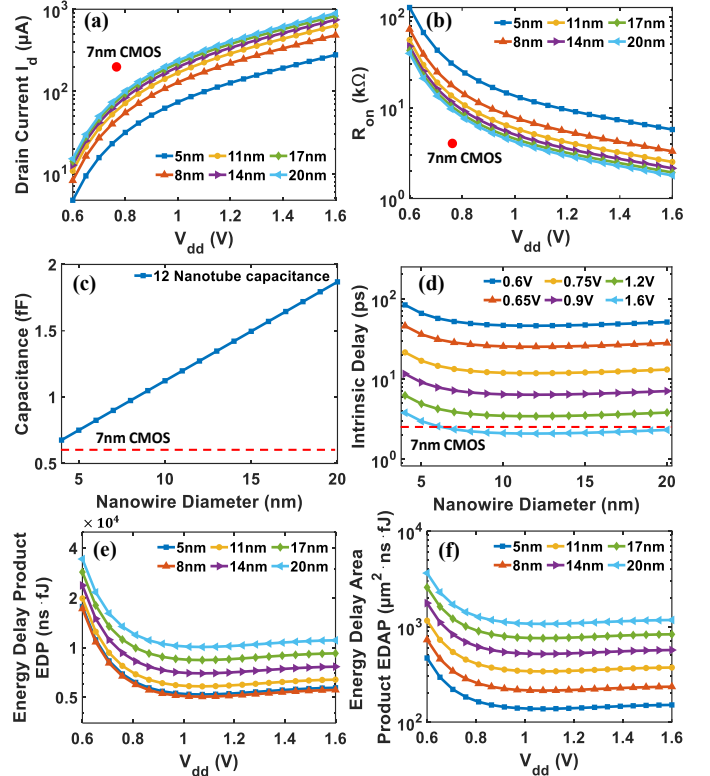


Fig. 4. (a) Drain current, (b) ON resistance, (c) gate capacitance, (d) intrinsic delay, (e) intrinsic EDP, and (f) intrinsic EDAP versus supply voltage under different nanotube diameters for REFT with 12 nanotubes.

physical models. The I-V relationship of RFET shown in Fig. 4. (a) is obtained from SPICE simulation based on the design kit by Gore et al. [12]. The impact of the nanowire diameter on the REFT current follows [18], as shown in Fig. 4. (a), indicating that the current increases with the nanotube diameter. Fig. 4. (b) shows the equivalent ON resistance, and the impact of nanowire diameter on the device gate capacitance follows [19], as shown in Fig. 4. (c). With these device models, we calculate intrinsic delay, energy-delay product (EDP), and energy-delay-area product (EDAP), as shown in Fig. 4. (d) – (f). These models provide the basis for the cell library generation that enables technology/circuit co-design framework for evaluating and exploring the performance of emerging reconfigurable devices.

B. Simulation Framework

To efficiently and accurately evaluate the performance of RFET under different parameters for large-scale digital circuits, we design and implement an industry-standard synthesis and placement/routing design flow using Cadence EDA tools. Additionally, we utilize MATLAB scripts to compile the device library and perform final data processing. The basic approaches are shown in Fig. 5.

III. SIMULATION RESULTS

Based on the modeling approaches in Section II, we perform the logic synthesis and physical synthesis for a series of benchmark netlists and analyzed the influence of device parameters on the circuit-level performance. These analysis results can show how to choose the appropriate RFET device parameters to achieve the balance between the overall circuit area, energy consumption, and speed. In addition, we sweep and investigate the critical reconfigurable cell area and analyzed its impact on various circuit metrics.

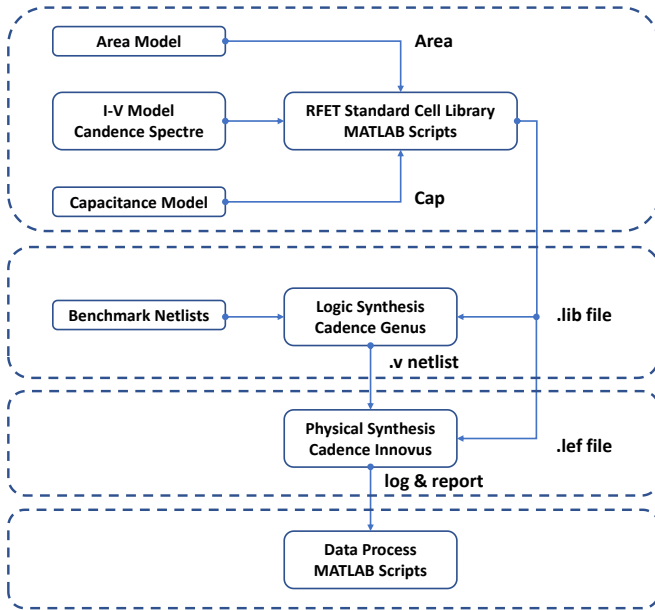


Fig. 5. Technology/circuit co-design framework for logic synthesis and physical synthesis of RFETs.

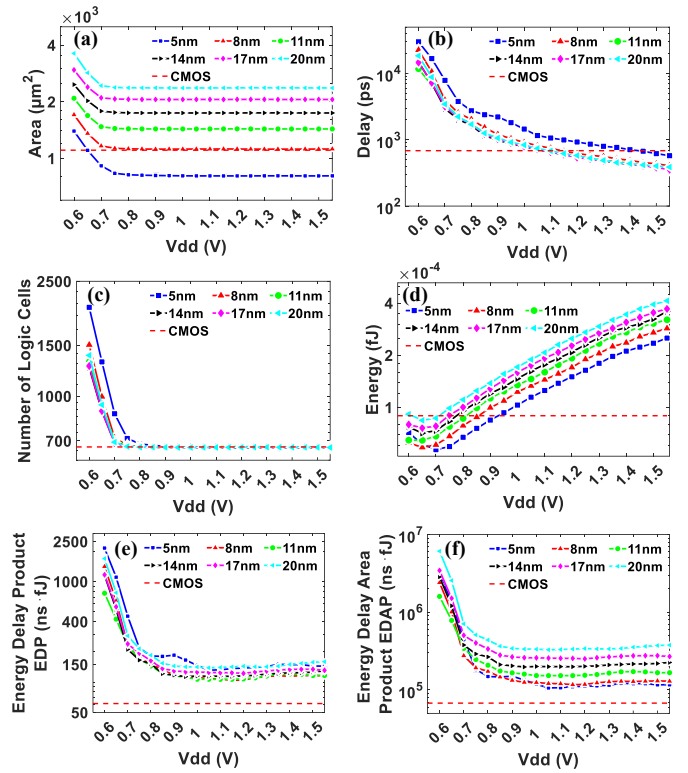


Fig. 6. (a) Area, (b) delay, (c) number of logic cells, (d) switching energy, (e) EDP, and (f) EDAP versus supply voltage under different nanowire diameters for benchmark netlist orig_diffeq1 using RFETs.

A. Impact of Supply Voltage and Nanowire Diameter

As shown in Fig. 6. (a), the overall circuit area of netlist “diffeq” increases with the nanowire diameter. A lower supply voltage also increases the circuit area because the large device resistance increases the circuit delay, as shown in Fig. 6. (b), leading to a large number of inverters to optimize the delay. This behavior can also be observed Fig. 6. (c), which shows a rapid increase in the number of logic gates as the supply voltage decreases, and most of these logic gates are inverters Fig. 6. (d) – (f) show circuit energy, EDP, and EDAP, showing that a smaller nanotube diameter reduces energy consumption and EDAP, and RFETs with a diameter around 8nm provide the best EDP.

In summary, the delay of the REFT circuits is larger than that of the CMOS circuit due to the lower ON current, which also leads to a disadvantage in terms of EDP and EDAP compared to CMOS. However, RFET circuits have advantages in terms of the circuit area and energy consumption thanks to the compact and efficient RFET logic implementation.

B. Synthesis Result with Optimal Vdd and Diameter

Fig. 7 shows the comparison of circuits using CMOS and RFETs using (1) default design parameters and (2) parameters under optimal EDP. Under the optimal EDP design point, the delay of RFET circuits is further optimized and becomes comparable to their CMOS counterparts, as shown in Fig. 7. (e). At the same time, the energy consumption and area of circuits are increased due to the higher supply voltage. Fig. 7. (g) lists

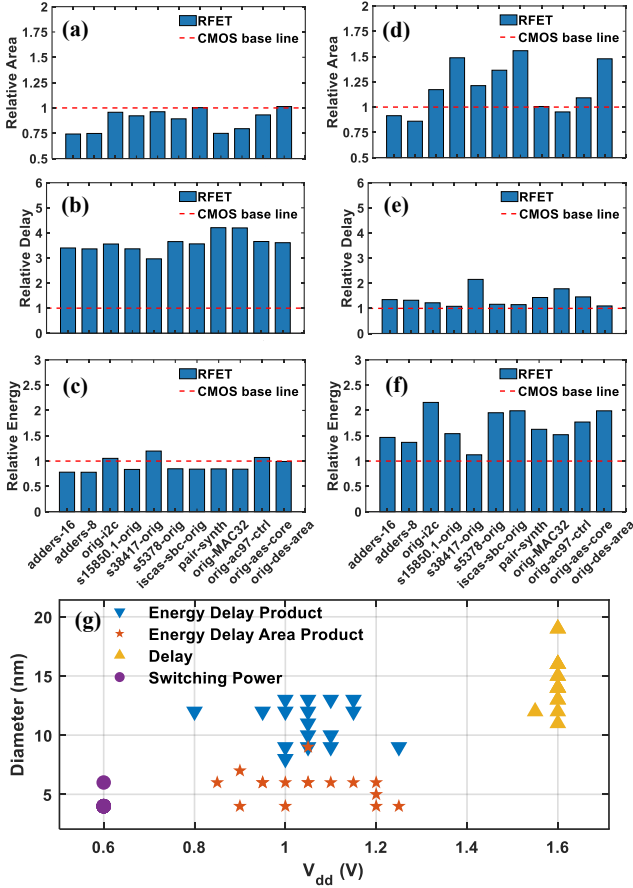


Fig. 7. Relative (a) area, (b) delay, and (c) energy for various REFT-based circuit benchmarks compared to CMOS. (d)-(f) show the same relative performance metrics under optimal EDP. (g) shows the optimal supply voltage and nanotube diameter for various performance metrics as optimization target.

the distribution of optimal supply voltage and nanotube diameter optimized for different circuit metrics. It can be observed that using a supply voltage of $\sim 1V$ and a nanotube diameter of $\sim 10nm$ provides a proper balance between energy consumption and delay.

C. Impact of Target Cell Area

Since RFETs have the flexibility of implementing different logic functions with different design [13, 20], we sweep several RFET logic cell area to investigate the impact of cell area on the overall circuit-level performance. Fig. 8 shows various performance metrics versus normalized cell area that scales the original cell area by $0.5\times$ to $1.5\times$. Here, the target cells under the investigation are NAND2x1/NOR2x1/MIN3x1. The increase of cell area not only influences the total circuit area but also increases the total interconnect length and capacitance, resulting in larger circuit switching energy consumption and delay, as shown in Fig. 8. (b) and (d). In Fig. 8. (c), the overall cell usage first decreases and then increases with the cell area because when the cell area is very small, the EDA tool utilizes many of these cells to optimize the overall area and maintains a small delay. Fig. 8. (g) shows the cell usage breakdown with the increase of cell area for three benchmark circuits, where one can clearly observe an increase in the target cell usage as the cell area is scaled down.

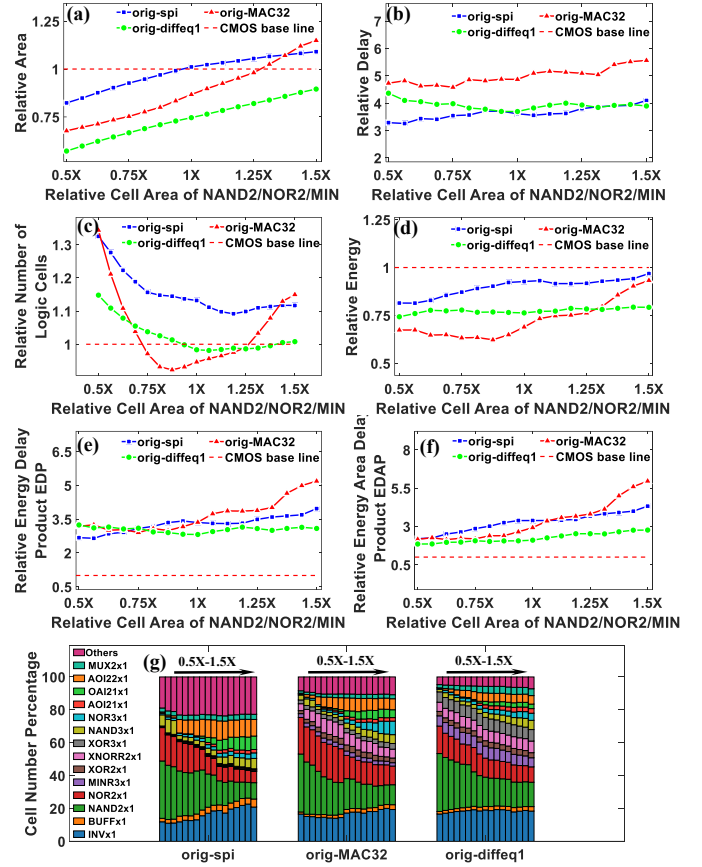


Fig. 8. Relative (a) area, (b) delay, (c) number of logic cells, (d) energy, (e) EDP, and (f) EDAP compared to CMOS when sweeping the area of cell NAND2x1/NOR2x1/MIN3x1 for three benchmark netlists. (g) shows the cell usage breakdown as the target cell area increases for three benchmark netlists.

IV. CONCLUSION

In this paper, a comprehensive modeling and optimization framework is developed to analyze and benchmark the performance of emerging RFETs with various device parameters. Multiple logic gate libraries are designed based on device-level physical modeling. Key device parameters are investigated, including the supply voltage, the diameter of the nanowire, and the logic cell area, to optimize circuit-level performance, including delay, energy, area, EDP, and EDAP. The result shows that optimal device-level parameters exist to balance energy consumption and delay. In addition, the design of a compact REFT cell layout is critical to overall circuit performance. The proposed framework is generic and can be applied to any emerging reconfigurable technologies. Although the delay of RFETs investigated in this paper is not comparable with 7nm CMOS, there exist other candidates that can achieve low on-resistance, such as GeNW which can maintain the reconfigurable advantage while achieving a small delay.

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