Emerging Reconfigurable Logic Device Based FPGA Design and Optimization

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***Abstract* —Reconfigurable devices are gaining increasing attention as a viable alternative and supplementary solution to the prevailing CMOS technology. In this paper, we develop a more efficient Field-Programmable Gate Array (FPGA) based on the reconfigurable field-effective transistor (RFET). We use the multi-gate characteristics of RFET to redesign the key components of FPGAs, namely SRAM-controlled multiplexer (MUX) and look-up tables (LUTs). The compact structure of the proposed design requires fewer transistors and leads to reduced delay and energy dissipation of the overall FPGA system. In addition, we develop a framework to perform a large design space exploration across various device-level and system-level parameters. A series of benchmark tests show that under the optimal design, up to 70% and 50% reduction can be achieved in delay and energy-delay product (EDP), respectively, compared to the traditional CMOS counterparts.**

Keywords—reconfigurable FET, field-programmable gate arrays (FPGAs), SRAM-controlled multiplexer, technology/system co-design, delay, area, energy, energy-delay product

I. INTRODUCTION

FPGAs are specialized integrated circuits that offer a unique approach to digital logic implementation. They consist of configurable logic blocks (CLBs) connected by programmable routing resources, containing various components, such as look-up tables (LUTs) and flip-flops to enable dynamic reconfiguration of logic functions [1, 2]. In addition, FPGAs are more cost-effective, have shorter time-to-market, and are better suited for small to medium-scale production, offering significant flexibility in chip design compared to application-specific integrated circuit (ASIC) chips.

Although FPGAs have excellent flexibility, their structure also brings several drawbacks. Since the FPGA requires a large number of routing resources to connect each reconfigurable unit, a significant portion of the chip area is used for routing, which also leads to a significant delay and energy overhead [3]. Many studies try to improve the overall area utilization and reduce delay and power consumption by changing the architecture of FPGA. Marrakchi et al. developed the tree-based FPGA which can greatly reduce the area [4]. Chtourou et al. introduced a mesh of clusters FPGA [5]. Ebrahimi et al. propose a power-efficient architecture for FPGAs based on a combination of reconfigurable hard logic and a small-input LUT [6]. However, most existing work only focuses on optimizing the FPGA from the architectural point of view, and limited work has been studied at device or gate levels. As traditional CMOS technologies approach the end of Moore's Law, many novel beyond-CMOS device concepts have been proposed, which brings new opportunities to create more efficient reconfigurable routing and logic components for FPGAs.

The reconfigurable field effect transistor (RFET) is an emerging device controlled by multiple gates [7-9]. Its program gate controls the polarity of the device, allowing it to switch between N- and P-type semiconductor. There are many physical implementation methods of RFET, such as silicon nanowire (SiNW) [9, 10], germanium nanowire (GeNW) [11], etc. RFET can be used to form efficient reconfigurable logic gates, and many researchers have demonstrated its potential advantages in designing efficient digital circuits [12]. RFET can implement all existing circuits composed of CMOS and achieve significant improvements in certain aspects, such as area, delay, and energy consumption [13].

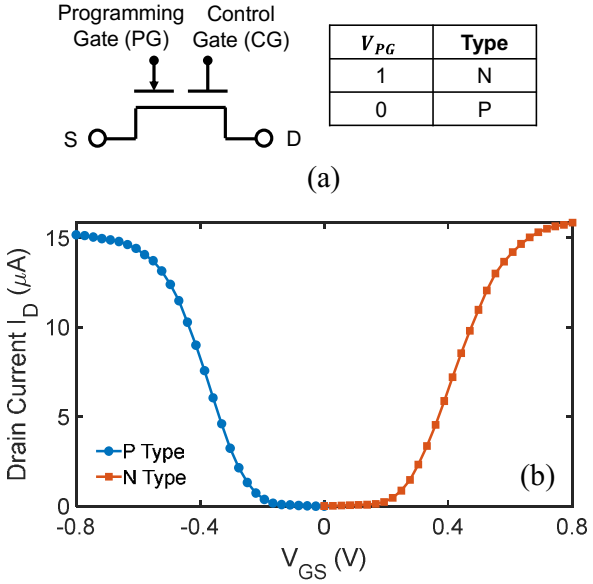
Many studies proposed emerging reconfigurable devices, such as RFETs, and their unique logic cells to improve the performance of FPGAs. For instance, Jamaa et al. proposed a FPGA design with reconfigurable logic gates using double-gate carbon nanotube transistors (CNFETs) [14]. Such a structure has a better performance gain, but its advantage mainly in the fine-grained case. This may lead to a larger delay, area, and energy for the global routing of the system and limit the practical usage. Gaillardon et al. designed a novel FPGA architecture based on SiNW RFETs [15], which arranges reconfigurable logic gates in a specific topology to form an efficient computation cluster to replace traditional LUTs. This architecture allows a single cluster to contain multiple reconfigurable logic gates, which can be used to optimize circuit performance by replacing global routing with more local routing. However, such an architecture may not be very efficient in the gate usage because a large number of reconfigurable gates are used for buffers or even left unconnected, leading to a waste in computational resources [16]. Cheng et al. tried to design hybrid topologies, allowing efficient

mapping of any function on nano-grain cells based architectures [17]. They proposed several highly efficient topologies to connect reconfigurable logic cells, which can enhance the gate usage. However, limited efforts have been made to the optimization of the global routing, which may lead to a large performance overhead of the FPGA.

In this paper, we take advantage of the multi-gate characteristics of RFET and its reconfigurable characteristics to design a more compact multiplexer (MUX) and LUT that plays an important role in FPGA systems. Built upon Verilog-to-Routing (VTR) open-source tools [18], the proposed technology/system co-design framework allows a large design space exploration across multiple hierarchies of FPGA, including device, gate, interconnect, and system levels. We will explore key device-level parameters, such as the number of control gates and supply voltage, and quantify their impacts on the system-level performance. A larger number of control gates allows fewer devices to achieve the same functionality, however, the footprint area of each device becomes larger. Such design trade-off cannot be simply performed only at the device or gate levels, and a technology/system co-design is critically needed to fully understand the true benefits brought by RFET for optimal system-level performance under different application scenarios.

The major contribution of this paper is listed as the following.

- We design a variety of efficient SRAM-controlled multiplexers and LUTs based on multi-gate RFET and demonstrate their trade-offs in area, delay, and energy consumption.
- We develop an efficient technology/system co-design framework for FPGA to enable optimization across various levels of hierarchies.



V_{PG}	Type
1	N
0	P

Fig. 1. (a) RFET device symbol, which can be switched between N- and P-type by applying different gate voltage on the program gate. (b) Drain current versus control gate voltage for N- and P-type RFETs [11].

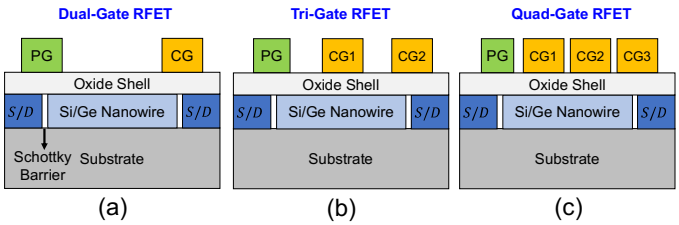


Fig. 2. Schematic of (a) dual-gate, (b) tri-gate, and (c) quad-gate RFET transistors based on Schottky or hybrid Schottky/thermionic controls [20]. The program gate is represented in light green, and the control gate is represented in yellow.

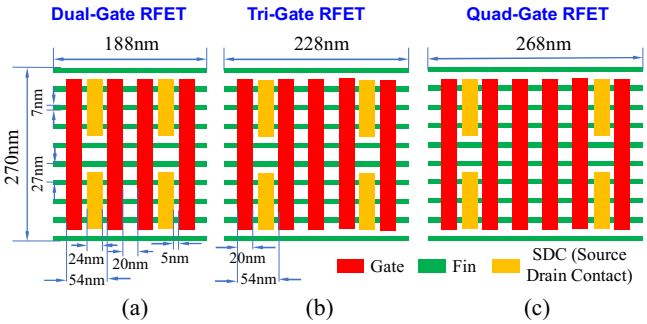


Fig. 3. Layout of (a) dual-gate, (b) tri-gate, and (c) quad-gate RFET transistors. Here, we follow the layout design rules specified by ASAP 7nm [23].

- We perform a large design space exploration for RFET-based FPGAs to show valuable insights to device technologists for designing more suitable device parameters for optimal system-level performance under various application scenarios.

II. Modeling Approach

This section first introduces the principles of RFET devices and their electrical characteristics. Based on the unique programmable polarity and intrinsic multi-gate characteristics of RFETs, compact and efficient multiplexers and LUTs are constructed. Next, the basic architecture of FPGAs is presented, as well as an analysis of bottlenecks limiting current FPGA technology, which demonstrates the advantages of RFET-based multiplexers and LUTs. Last, the proposed technology/system co-design framework will be illustrated.

A. RFET Device-Level Characteristics

Unlike conventional FinFETs or gate-all-around (GAA) devices, RFETs can change the polarity of the device by applying different voltages to the programmable gate, making it possible to switch between N-type and P-type [19]. In addition, since RFETs operate based on Schottky barriers in metal-semiconductor contacts, there is a high degree of symmetry in the I-V curves of N- and P-type devices. As shown in Fig. 1, a dual-gate RFET can be equivalent to a series connection of two transistors, and the RFET conducts only when the same voltage is applied to both gates [7]. Here, device reliability and processes are not considered.

In addition to dual-gate RFETs, there are many other types of RFETs based on more control gates that operate on hybrid Schottky/thermionic barriers [20], as shown in Fig. 2. These

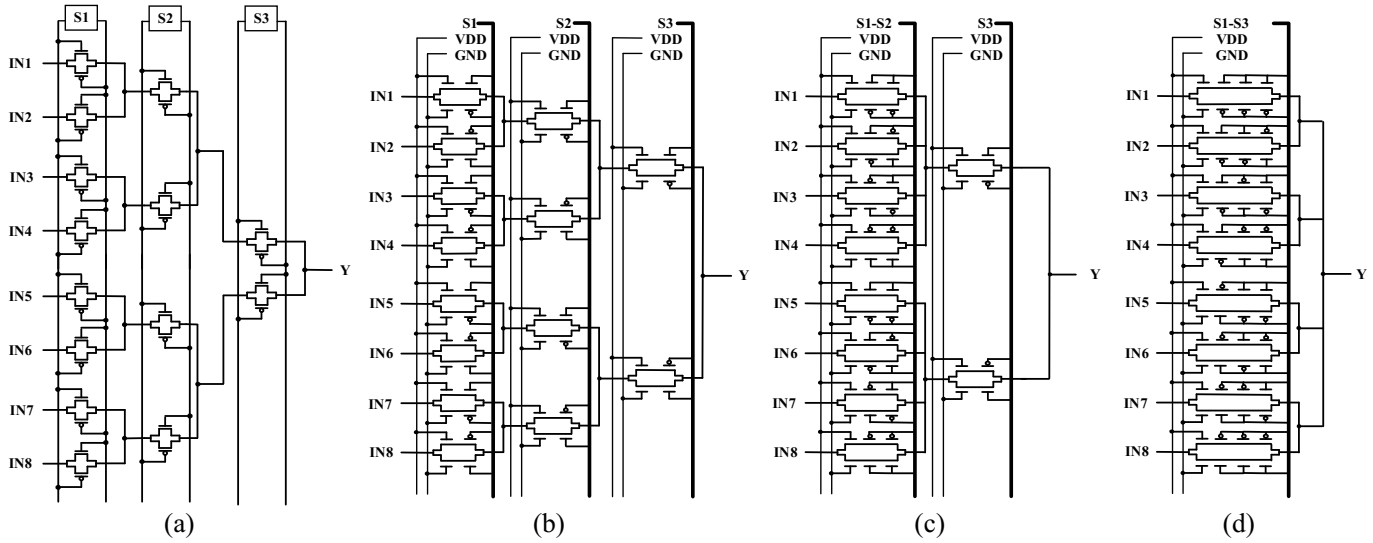


Fig. 4. (a) Traditional CMOS-based 8-to-1 multiplexer, where each column is controlled by an SRAM. (b) Multiplexer based on dual-gate RFETs, where the program gate is used for polarity control and only one control gate determines the ON/OFF states of RFETs. (c) Multiplexer based on tri-gate RFETs, where two control gates are used for the first stage pass transistors. (d) Multiplexer based on quad-gate RFETs, where three control gates are used, and all SRAMs are applied on the single stage of pass transistors. For each RFET-based transmission gate, the top and bottom transistors are fixed to N- and P-type, respectively.

multi-gate structures are demonstrated both theoretically and experimentally [21, 22]. Although these RFETs differ slightly in their control principles as well as their structure, the common behavior is that when the device is programmed for a certain polarity, all of the remaining control gates must maintain the same control voltage to turn the transistor on. Using quad-gate RFET in Fig. 2(c) as an example, when the programming gate is set to logic 1 (Vdd), the device is N-type, and all CG1-CG3 need to be set to logic 1 to keep the RFET at the ON state.

According to the ASAP 7nm PDK design rules [23], combined with the actual size of the device of RFET, individual transistor layout based on different numbers of control gates is designed, the layout of a multi-gate structure is shown in Fig. 3. The relationship between the RFET-based transistor area and the number of RFET control gates can be obtained accordingly. Here, the RFET gate distance is set to 20nm considering the physical size of the RFET, and the capacitance of the device can also be simulated [24]. We assume both CMOS and RFET devices consist of a single layer of 3 fins, and the extracted capacitances for both devices are similar. The current-voltage relationship of RFET is adopted from previous works [11, 25] and the corresponding CMOS current-voltage relationship is simulated with ASAP 7nm PDK.

B. RFET-based Multiplexer

In modern digital circuit design, especially in FPGAs and other reconfigurable architectures, transmission gates are commonly used to connect logic cells and implement LUTs [1]. RFETs can be used to realize more compact MUXes due to their multi-gate characteristics. As shown in the example in Fig. 4(a), an 8-to-1 multiplexer requires three SRAMs to control three stages of pass transistors. If the conventional CMOS-based pass transistor is replaced by an RFET pass transistor, fewer transistors and stages can be realized, potentially leading to a

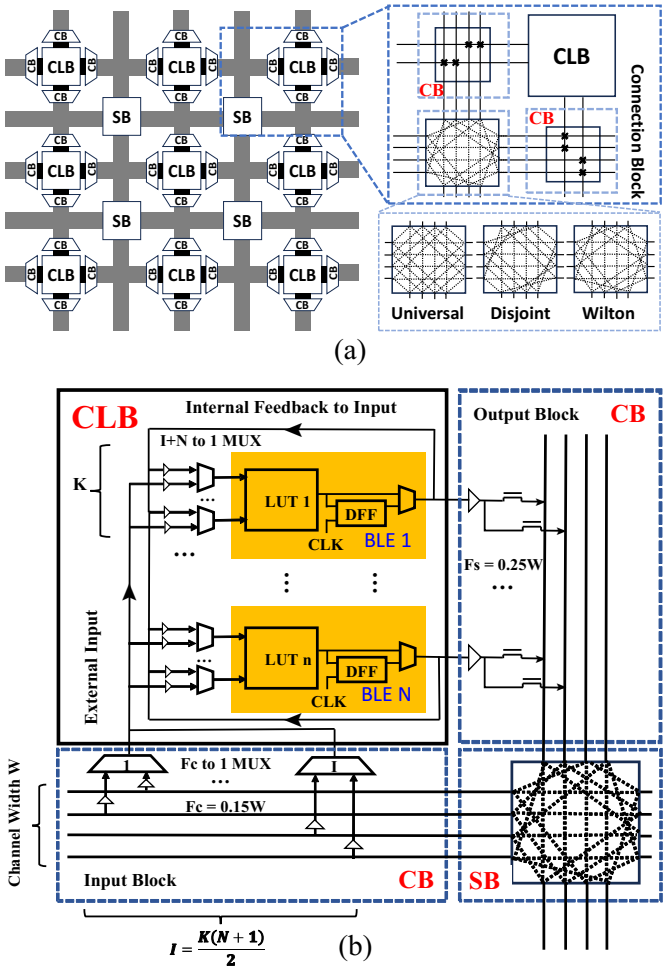


Fig. 5. (a) A generic FPGA architecture and (b) detailed logic cluster structure.

smaller footprint area and critical path delay. As shown in Fig. 4(b)-(d), the RFET-based pass transistor consists of two multi-gate RFETs, the program gate of top/bottom transistor is fixed to Vdd/GND, leading to an N-/P-type transistor. The ON/OFF states of the RFET transistor depend on whether the program and control gate are applied with the same voltage, making it possible to realize the conduction of RFET under a specific set of SRAM combinations.

For a dual-gate RFET-based MUX shown in Fig. 4(b), only one control gate is used to control the switching of the pass transistor, which is similar to the CMOS counterpart in terms of structure and performance. For Fig. 4(c) and (d), as the number of control gates of the RFET increases, multiple control gates can be integrated into the same RFET. This reduces the total number of transistors as well as the number of transistors on the critical path, leading to a smaller critical path delay. Because of the similar structure, compact RFET-based logic circuits can be used to build not only multiplexers but also LUTs, which is one of the key building blocks of FPGAs.

C. FPGA Architecture and Modeling

FPGAs consist of an array of CLBs and programmable interconnects to implement various logic functions, as shown in Fig. 5 [1]. The interconnects provide pathways for signals to flow between these blocks. The CLB consists of N basic logic elements (BLEs), which are the basic reconfigurable logic elements. Each BLE includes a D flip-flop, MUX, and a *K*-input LUT, and each input of LUT comes from an $I + N$ to 1 multiplexer, where *N* is the number of feedback signals from CLB local outputs and *I* is the number of global input signals. Ahmed and Rose's paper has given the best *I* value with different numbers of BLEs per CLB and LUT input size [2], as shown in (1).

$$I = (N + 1) \times \frac{K}{2} \tag{1}$$

In terms of global routing, input/output connection blocks are used to connect logic blocks and routing channels. To reflect the flexibility of the connection block, two parameters are defined, namely F_c is the input connection flexibility and F_s is the output connection flexibility. Here, we set $F_c = 0.15W$ and $F_s = 0.25W$, where W is the number of routing channels.

The switch box consists of programmable routing switches and is used to form connections for the horizontal and vertical routing channels. There are several types of switch boxes, as shown in Fig. 5(a). Disjoint style has been used in the Xilinx XC4000 series, and Universal style and Wilton style require fewer routing tracks and a smaller logic area [26]. All these styles have trade-offs among performance metrics, and the Wilton style is used in this paper. The resistance and capacitance of wire segments, which are measured in units of CLB block length, change with the size of the CLB. Here, we estimate the interconnect capacitance and resistance per unit length of copper wires by following existing work [27].

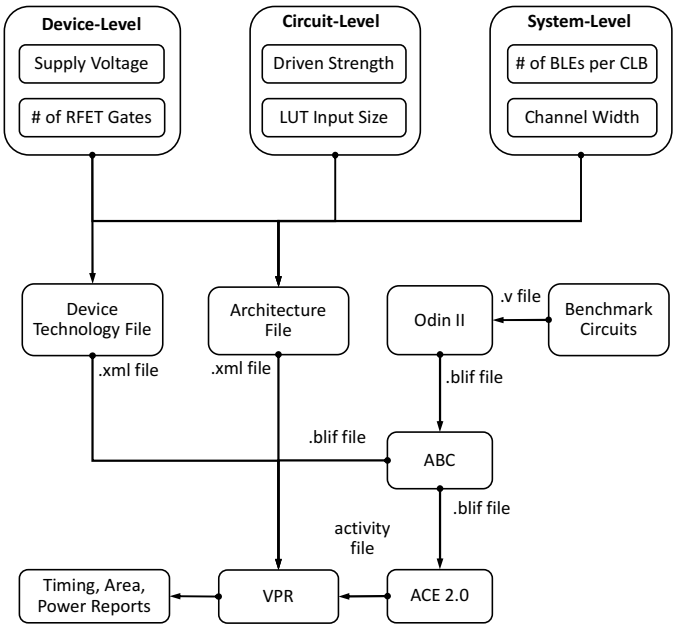


Fig. 6. Technology/system co-design framework for FPGA using emerging reconfigurable device technologies.

D. Technology/System Co-Design Framework

To effectively and efficiently enable a large design space exploration, we develop a technology/system co-design framework, shown in Fig. 6. The input of the framework includes (i) a technology file, which determines device-level characteristics, such as ON and OFF resistance and capacitance, (ii) an architecture file that includes gate-, interconnect-, and system-level information, such as MUX resistance/capacitance, interconnect resistance/capacitance, LUT input size, the number of BLEs per CLB, etc., and (iii) a high-level hardware description file that defines the circuit functionality. For the circuit simulation, we adopt several open-source tools for the conversion of netlists and related calculations. The Verilog Hardware Description Language (VHDL) file is converted to a BLIF netlist file by Odin II [28]. Then, ABC, an open-source synthesis and verification tool [29], is used to optimize the netlist file and perform technical mapping to the corresponding LUT structures. For a given LUT-based input netlist file, we adopt VPR, an open-source tool for designing FPGAs [18], to perform LUT clustering, placement, and routing. For the switching energy calculation, the activity file is generated by ACE2.0, which generates the effective activity factors for each connection in an FPGA system based on the circuit netlist generated by ABC. We utilize scripts to automate the optimization process by integrating the aforementioned open-source tools to form a complete technology/system co-design framework. The final output report files include optimized critical path delay, total area, and energy dissipation of the FPGA.

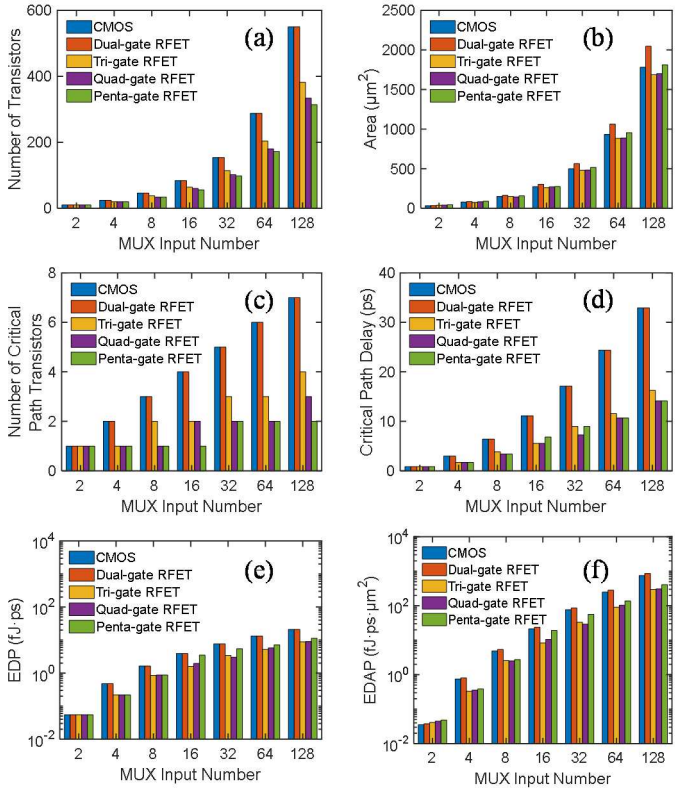


Fig. 7. Impacts of the number of RFET gates on cell level performance. (a) The number of transistors per MUX, (b) total area considering device layout, (c) the number of transistors on the critical path, (d) critical path delay, (e) EDP, and (f) EDAP versus the number of MUX inputs for different device options.

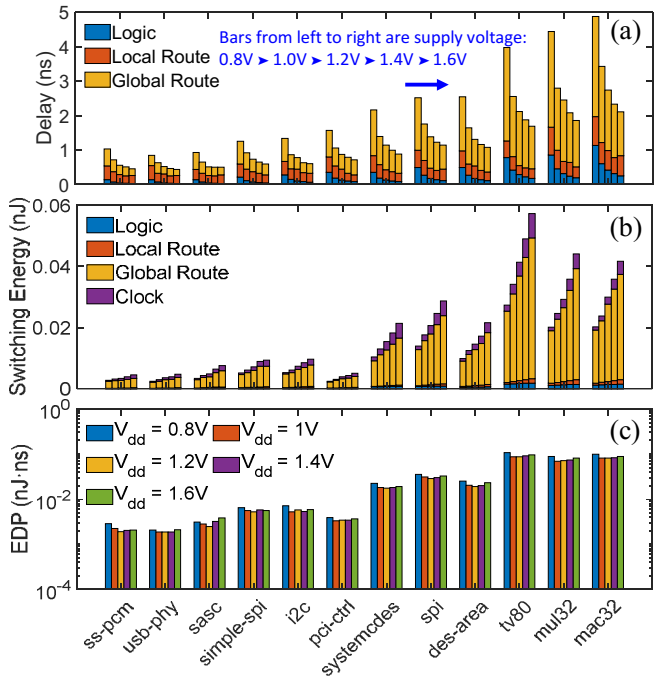


Fig. 8. (a) Delay, (b) switching energy, and (c) EDP under various supply voltage for different circuit netlists. Here, the system uses tri-gate-based structure with 10 BLEs per CLB using 6-input LUT for each BLE.

III. Simulation Results

In this section, we will use emerging multi-gate RFET devices to design FPGAs based on the simulation framework described in Section II and benchmark them against CMOS counterparts. Various device-level parameters, such as Vdd, the number of RFET input control gates, and several circuit/system-level parameters, including the number of BLEs per CLB and LUT input size, will be analyzed in detail. Finally, the RFET-based FPGAs will be analyzed to achieve the best performance.

A. Cell-Level MUX Performance Comparison

Based on the design of MUX using multi-gate RFETs illustrated in Section II B, we quantify the impact of the number of RFET control gates on the MUX performance in terms of area, delay, energy, energy-delay product (EDP), and energy-delay-area product (EDAP). Fig. 7 shows that the number of RFETs per MUX decreases as the number of control gates increases, which can be verified by the circuit schematic shown in Fig. 4. An optimal MUX area can be observed using 3 or 4 control gates for RFETs, which is slightly better than CMOS MUXes, because the individual RFET area increases with the number of control gates, while the total number of transistors decreases with the number of control gates.

Based on the Elmore delay model, the critical path delay of the circuits is shown in Fig. 7(d). Because RFET-based MUXes have fewer transistors on the critical path, up to 50% delay reduction can be realized compared to CMOS MUXes when the number of MUX inputs is larger than 2. In terms of the overall EDP and EDAP, the results show that depending on the number of MUX inputs, RFETs with either 3 or 4 control gates have the best overall performance, where over 50% reduction can be observed compared to CMOS counterparts.

B. System-Level Performance

In this subsection, we will perform a large design space exploration to quantify the impact of various design parameters and optimize those parameters for optimal system-level performance. Unless specified elsewhere, the default system configuration uses tri-gate RFET devices with 0.8V Vdd, and each CLB contains 10 BLEs with a 6-input LUT in each BLE.

1) Impact of Supply Voltage

To explore the impact of the RFET supply voltage on the overall system performance, we simulate the FPGA results by varying the supply voltage from 0.8V to 1.6V. Fig. 8 shows that in general, the critical path delay and switching energy are dominated by the global routing because of the long interconnect length. As the supply voltage increases, the critical path delay decreases because a higher supply voltage provides a smaller ON resistance and reduces the RC delay. The smaller delay comes with the cost of larger switching energy as the supply voltage increases. Therefore, an optimal supply voltage of around 1.2V can be observed to minimize the overall EDP of the system, which makes a proper balance between delay and energy consumption.

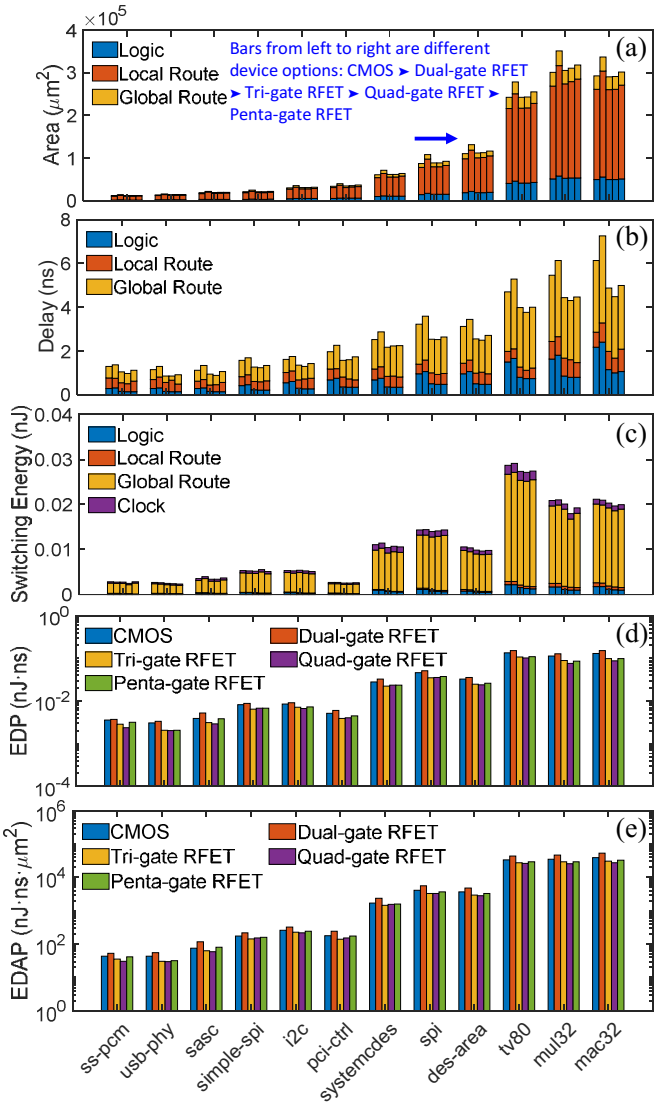


Fig. 9. (a) Area, (b) delay, (c) switching energy, (d) EDP, and (e) EDAP under various devices for different circuit netlists. Here, the system is under 0.8V Vdd and uses 10 BLEs per CLB using 6-input LUT for each BLE.

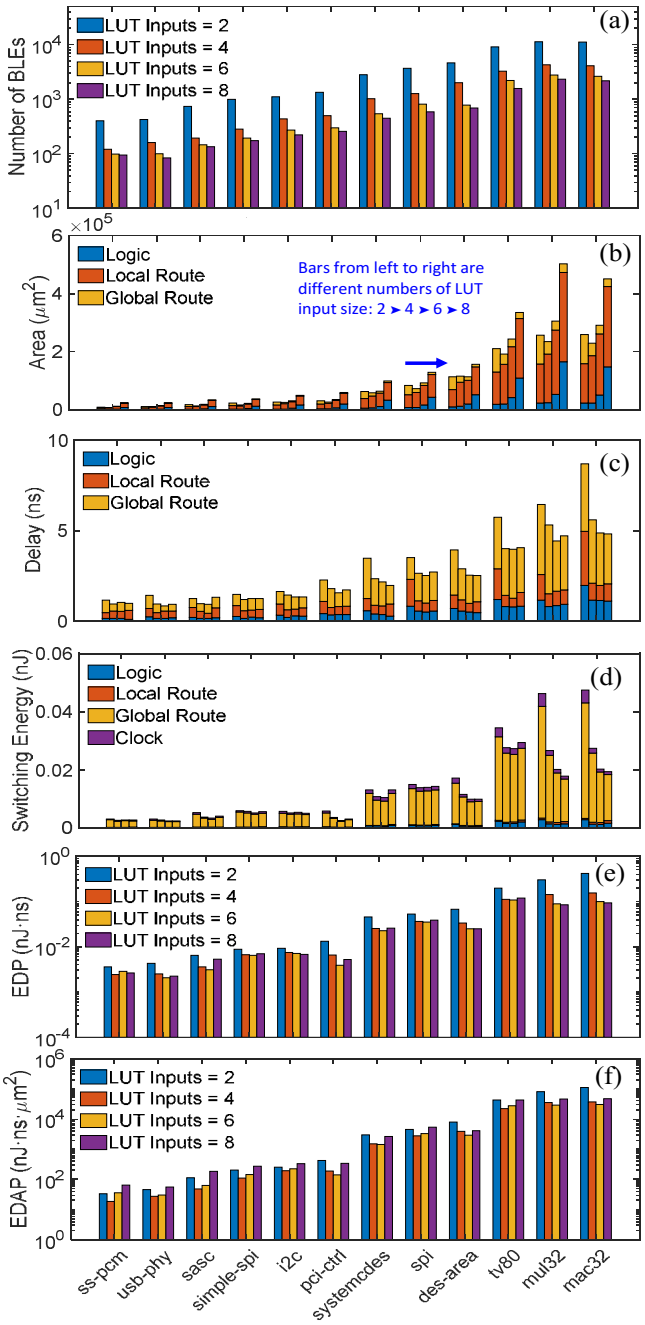


Fig. 10. (a) The number of BLEs, (b) area, (c) delay, (d) switching energy, (e) EDP, and (f) EDAP under various LUT input sizes for different circuit netlists. Here, the system is under 0.8V Vdd with tri-gate-based structure using 10 BLEs per CLB.

2) *Impact of the Number of RFET Control Gates*

To translate the MUX-level performance shown in Fig. 7 to the overall system-level metrics, Fig. 9 shows the performance comparison among CMOS and RFETs with different numbers of control gates. Since the single transistor area of RFET is larger than CMOS, the total area of RFET-based FPGA is larger than CMOS-based FPGA even though the RFET can reduce the total number of transistors.

However, when the number of RFET control gates is 3 or 4, all parameters of the circuit, except for the total area, are better than CMOS counterparts, especially for the critical path delay. For most circuit netlists, up to 40% reduction can be observed for FPGAs using RFETs with 3 or 4 control gates. While the delay is reduced, the overall switching energy shows some improvement, which is caused by the reduction of energy consumed by the LUTs and local routing MUXes. This ultimately leads to a significant improvement in the overall performance in EDP and EDAP of RFET-based FPGAs compared to their CMOS counterparts.

3) *Impact of the Number of LUT Inputs*

The input size of the LUT is an important parameter to balance the local and global routing of an FPGA. A large LUT input size reduces the number of LUTs needed during the circuit synthesis, which may reduce the critical path delay and energy dissipation. However, if the LUT input size is too large, it will

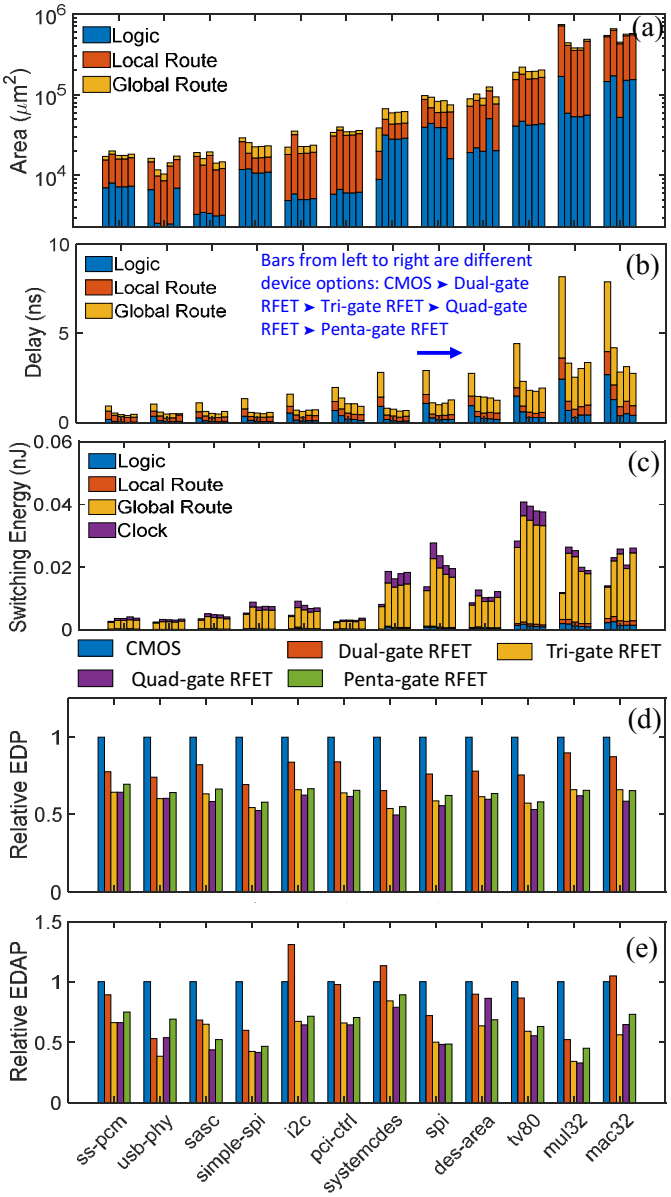


Fig. 11. Optimized (a) Area, (b) delay, (c) switching energy, (d) relative EDP, and (e) relative EDAP under various devices for different circuit netlists. Here, the system operates under the optimal Vdd with optimal LUT size and optimal numbers of BLEs per CLB.

dramatically increase the BLE area and have negative impacts on the system-level performance. As a result, Fig. 10 shows that optimal LUT input sizes exist for several circuit benchmarks to minimize the overall EDP and EDAP. In general, the system prefers to use a smaller LUT input size to minimize EDAP due to the large area overhead for a large LUT input size.

As shown in Fig. 10(a), the number of BLEs required by the system decreases as the LUT size increases, but eventually saturates as the LUT size increases. This leads to the trend in Fig. 10(b) that the system area first decreases due to the smaller number of BLEs and then eventually increases due to the larger area per BLE. In terms of overall performance, the 4-input LUT and 6-input LUT possess the best performance.

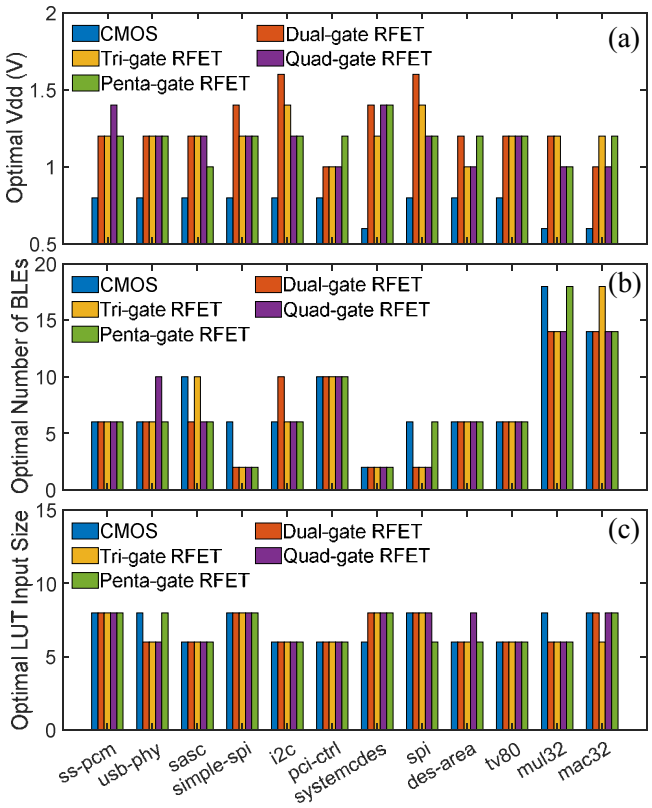


Fig. 12. Optimal (a) Supply voltage, (b) the number of BLEs per CLB, and (c) LUT input size to minimize the overall EDP of FPGAs using various device options for a variety of circuit applications.

C. *Optimized System-Level Performance Comparison*

Previous results have demonstrated that the performance of RFET-based FPGA systems highly depends on various parameters across hierarchies. To comprehensively evaluate the RFET-based FPGA system and benchmark against its CMOS counterpart, we choose EDP as the optimization target and investigate the optimal device- and system-level parameters to minimize the overall system-level target metric.

Although RFET-based FPGA architectures do not have a switching energy advantage over CMOS-based FPGAs at the optimal EDP design point, they have significant advantages in terms of delay, and up to 70% reduction can be observed in Fig. 11 compared with CMOS counterparts under the optimal supply voltage and system/circuit size. This large delay improvement is mainly due to (i) the unique multi-gate feature of RFETs that allows a smaller number of RFETs on the critical path and (ii) a higher optimal supply voltage of RFET, as can be observed in Fig. 12. Overall, up to 50% and 65% savings in EDP and EDAP, respectively, can be observed for RFET-based systems. From Fig. 12, depending on the circuit application, the optimal LUT size and supply voltage are around 6~8 and 0.6~1.6V, respectively, across various device options, and the optimal number of BLEs per CLB varies more substantially.

IV. Conclusion

In this paper, we design a compact RFET-based MUX and LUT for FPGAs by taking advantage of the unique feature of multi-gate structure. In addition, we develop an efficient technology/system co-design framework to perform a large design space exploration across different hierarchies. Results show that the device-level parameters, such as supply voltage and the number of RFET control gates, as well as circuit/system-level parameters, including LUT input size and the number of BLEs per CLB, have a large impact on the system-level performance. Under the optimal design, up to 50% improvement in EDP and EDAP can be observed for RFET-based FPGAs compared to their CMOS counterparts, where a majority of the improvement comes from the smaller critical path delay thanks to the multi-gate feature of RFET devices.

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