A Five-level Hybrid Modular Multilevel Converter with High Efficiency and Power Density

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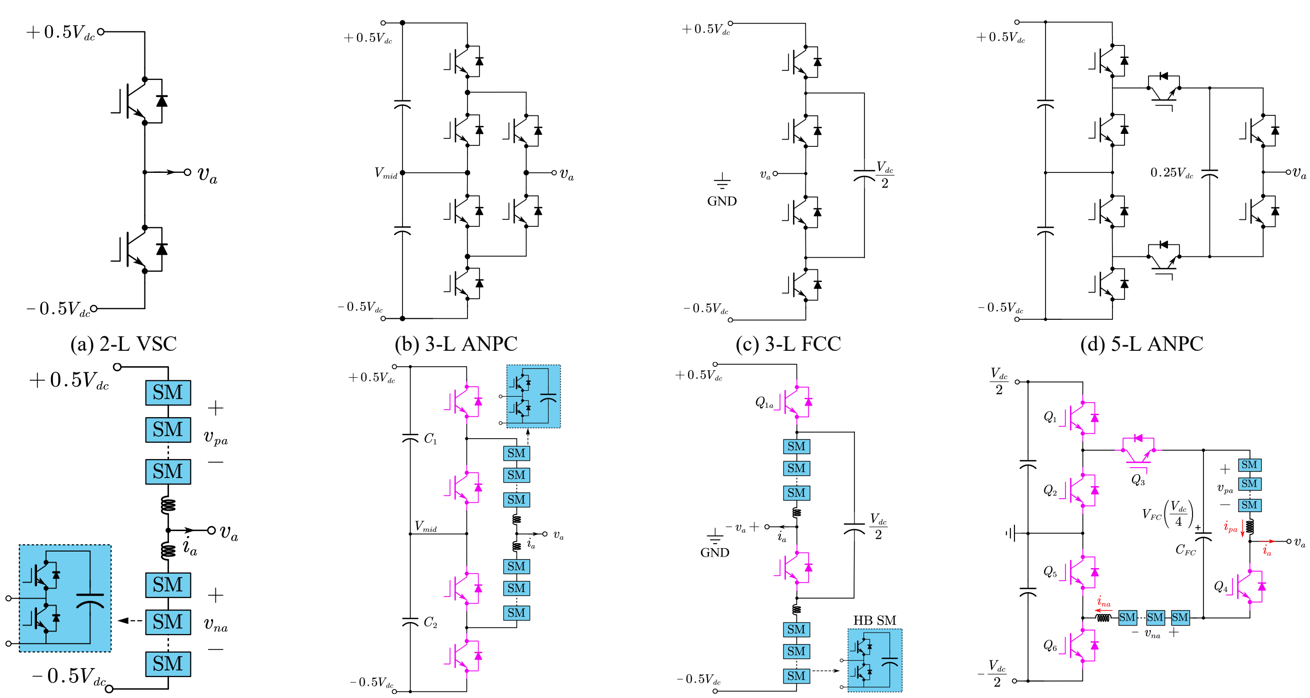
***Abstract*— This paper presents a novel five-level hybrid modular multilevel converter (5-L HMMC) for the medium voltage (MV) applications as a member of HMMC family. Compared with the traditional modular multilevel converter (MMC), 5-L HMMC can reduce the number of MMC SMs by fourfold while retaining the excellent output power quality. And it also avoids the limitation of power loop inductance in the traditional 5-L converter due to the line-frequency operation of 5-L stack. Therefore, 5-L HMMC can keep the key benefits of modularity, reliability, and excellent harmonic performance from chain-link, while significantly reducing the power losses, costs, and volume. The feasibility of proposed converter is also verified by the simulation and experimental results.**

Keywords*— *Five-level hybrid modular multilevel converter (5-L HMMC), HV switch, chain-link (CL).

I. Introduction

Modular Multilevel Converter (MMC) is one of the most attractive topologies for medium voltage (MV) and high voltage (HV) applications due to its flexibility, modular structure and excellent power [1-3]. However, the large number of chain-link submodules (SM) in MMC (Fig 1.(e)) create many drawbacks, such as the doubled device number and large capacitor size, hence resulting in bulky converters and higher construction cost [4-6]. On the other hand, the conventional multilevel converter has less device-count and higher power-density but suffers from the loop inductance influence due to the complex switching commutation loops, which limits the switching-frequency and results in a poor output power quality [7-10].

In order to combine the advantages of two types of multilevel converter, some hybrid topologies were proposed with the following principles [11]. Some low-voltage (LV) SMs in MMC are replaced with the high voltage (HV) switches for smaller footprint and lower cost. Moreover, the chain-link (CL) composed of SMs is used to shape the ac voltage, so that the ac output quality is kept same as MMC. While the HV switches should operate at low frequency for ease of device-stacking and high reliability.



(a) 2-L VSC (b) 3-L ANPC (c) 3-L FCC (d) 5-L ANPC

(e) MMC (f) 3-L HMMC (g) FC-HMMC (h) proposed 5-L HMMC

Fig. 1 Derived HMMC topologies from traditional multilevel converter.

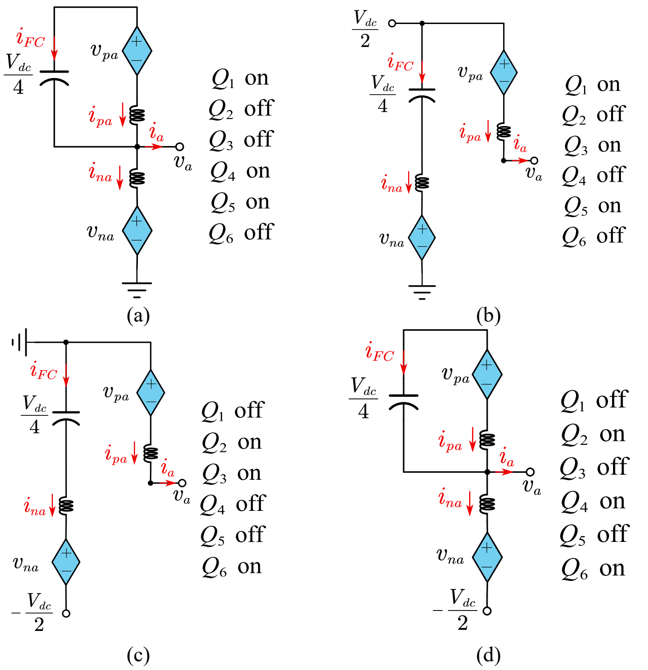


Fig. 2 Four working modes of single-phase 5-L HMMC, (a) mode 1, (b) mode 2, (c) module 3, (d) mode 4.

Based on this idea, the alternate arm converter (AAC) was first proposed by combining the two-level VSC with CL [12] [13]. It is intended for a compact design with fault-blocking capability. However, a specific “sweet-spot” operation is required for the voltage balancing, and a big dc side filter is necessary to remove the dc bus current ripple. In addition, the utilization of three-level stack derives the modular embedded multilevel converter (MEMC) [14] and a family of three-level hybrid MMC (3-L HMMC) (Fig 1.(f)) [15-22], the flying capacitor HMMC (Fig 1.(g)) [23] and hybrid-leg MMC [24]. However, up to now none of five-level stack has been utilized to construct the new hybrid MMC topologies.

This paper proposes a novel 5-L HMMC, which evolves from the 3-L HMMC. Its operation principle is elaborated and the CL current allocation is designed to balance the CL and flying capacitor (FC) voltage. Besides, the performance of 5-L HMMC is evaluated and compared with the traditional HB MMC and 3-L HMMC. The simulation results of a 500 MVA 10 kV MV case and the experimental results of a scale-down prototype are provided to validate the operation.

II. Operation Principle and Arm Current Design

A. Single-Phase Operation of 5-L HMMC

Fig. 1 depicts the topologies of 2-level converter, 3-L ANPC, 5-L ANPC, and the derived MMC versions of conventional MMC, 3-L HMMC and proposed 5-L HMMC. The similar point is replacing one pair of switches with two CLs. In proposed 5-L HMMC, six HV switches $Q_1 \sim Q_6$ are composed of series LV devices, which can be driven using the single-gate driver solution [25], [26]. Whereas the left two switches in 5-L ANPC are replaced with two CLs and the series inductors. The CL consists of N series HB SMs with dc-link floating capacitor C_{sm} and voltage of V_{sm}. A large flying capacitor with voltage of $0.25V_{\mathrm{dc}}$ is connected same with 5-L ANPC. Similar to the 3-L HMMC [10], the HV switches operate at low frequency so that the switching loss and series device difficulty are reduced significantly. There are many possible combinations of six HV switches, but only four of them as shown in Fig. 2 are utilized in this paper. In order to reduce the CL voltage rating, four working modes are assigned according to the ac voltage value as shown in Fig. 3 and the corresponding CL voltages are calculated with (1). It can be seen that the maximum CL voltage is reduced to $0.25V_{\mathrm{dc}}$, which is a quarter of the MMC CL voltage stress V_{dc}.

$$
\begin{cases} v_{pa}^* = 0.25V_{dc} - v_a,\ v_{na}^* = 0.25V_{dc} & \left(0 \leqslant v_a < \frac{V_{dc}}{4}\right) \\ i_{pa} = -i_{FC},\ i_{na} = -i_a \end{cases}
$$
$$
\begin{cases} v_{pa}^* = 0.25V_{dc},\ v_{na}^* = 0.5V_{dc} - v_a & \left(\frac{V_{dc}}{4} \leqslant v_a < \frac{V_{dc}}{2}\right) \\ i_{pa} = i_a,\ i_{na} = i_{FC} \end{cases}
$$
$$
\begin{cases} v_{pa}^* = 0.25V_{dc},\ v_{na}^* = -v_a & \left(-\frac{V_{dc}}{4} \leqslant v_a < 0\right) \\ i_{pa} = i_a,\ i_{na} = i_{FC} \end{cases} \tag{1}
$$
$$
\begin{cases} v_{pa}^* = 0.25V_{dc} + v_a,\ v_{na}^* = 0.25V_{dc} & \left(-\frac{V_{dc}}{2} \leqslant v_a < -\frac{V_{dc}}{4}\right) \\ i_{pa} = -i_{FC},\ i_{na} = -i_a \end{cases}
$$

The ac voltage and current are defined as,

$$
v_a = V_{ac}\sin(\omega t), i_a = V_{ac}\sin(\omega t + \varphi) \tag{2}
$$

The phase angle corresponding to the mode switching point could be derived based on the ac voltage

$$
\begin{aligned} &\theta_0 = \arcsin\left(\frac{V_{dc}}{4V_{ac}}\right), \theta_1 = \pi - \theta_0 \\ &\theta_3 = \pi + \theta_0, \theta_4 = 2\pi - \theta_0 \end{aligned} \tag{3}
$$

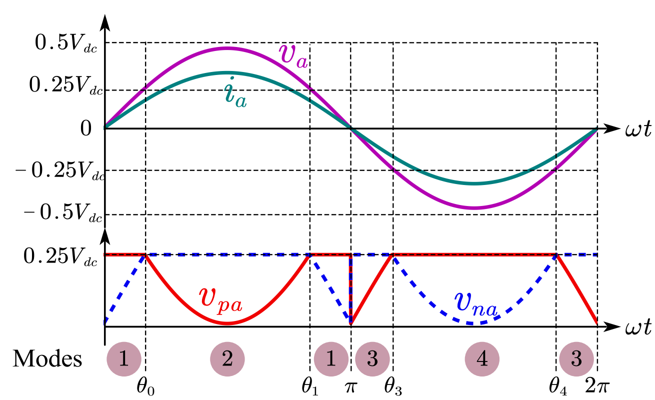


Fig. 3 The working modes and CL voltage waveform of single-phase 5-L HMMC during one line cycle.

B. Current Allocation and Capacitor Voltage Ripple

According to the previous mode assignment, the CL current is determined at certain modes, such as i_{pa} in mode 2 and 3. For example, during the range of (θ_0, θ_1) of mode 2, the upper CL dc-link capacitor voltage V_{cpa} increases with the positive current i_{pa}. However, i_{pa} is flexible in mode 1 and 4. In order to suppress the capacitor voltage ripple, i_{pa} in the mode 1 is designed as 0. While in mode 4, a sinusoidal current with amplitude of I_{m} and a certain offset is designed to smooth the CL current. So the CL current is designed as (4).

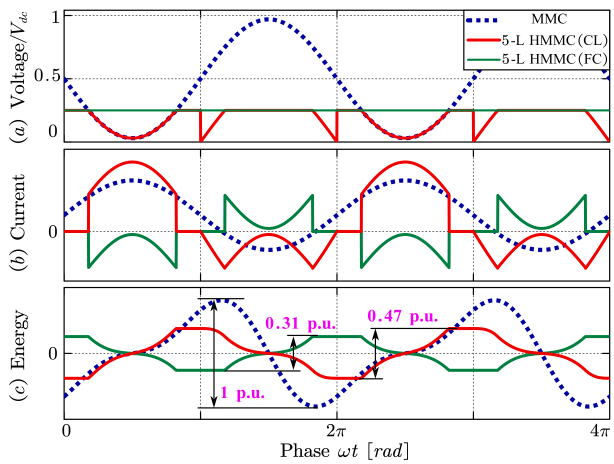


Fig. 4 The normalized CL and FC voltage, current and energy comparison between 5-L HMMC and MMC.

$$
\begin{aligned}
&i_{pa} = -i_{FC} = 0, (0 \leqslant \omega t < \theta_0,\ \theta_1 \leqslant \omega t < \pi) \\
&i_{na} = i_{FC} = I_m \sin\left(\frac{\omega t - \theta_0}{2\pi - \theta_0}\pi\right) - i_a\big|_{\omega t=\theta_0}, (\theta_0 \leqslant \omega t < \theta_1) \\
&i_{na} = i_{FC} = 0, (\pi \leqslant \omega t < \theta_3,\ \theta_4 \leqslant \omega t < 2\pi) \\
&i_{pa} = -i_{FC} = I_m \sin\left(\frac{\omega t - \theta_3}{2\pi - \theta_0}\pi\right) + i_a\big|_{\omega t=\theta_3}, (\theta_3 \leqslant \omega t < \theta_4)
\end{aligned} \tag{4}
$$

The normalized CL and FC voltage and current waveforms of 5-L HMMC and MMC are plotted in Fig. 4. It can be seen that the CL energy ripple of 5-L HMMC is only 31% of MMC.

C. *Performance Comaprison*

Arm voltage stress is directly related to the device number used in HMMC. The number of SMs in each CL is selected based on the rated dc link capacitor voltage V_{SM}.

$$N_{5\text{-L HMMC}} = \frac{0.25V_{dc}}{V_{SM}} \tag{5}$$

$$N_{MMC} = \frac{V_{dc}}{V_{SM}} \tag{6}$$

The HV switch requirement is related to the blocking voltage V_{br} of each device. Supposing a blocking utilization factor of 70%, the device number for six HV switches could be expressed in (7) and (8).

$$N_{5\text{-L HMMC}(Q_{1,2,5,6})} = \frac{0.5V_{dc}}{0.7V_{br}} \tag{7}$$

$$N_{5\text{-L HMMC}(Q_{3,4})} = \frac{0.25V_{dc}}{0.7V_{br}} \tag{8}$$

A specific case of 20 kV dc bus voltage is performed here, where 1.7 kV device is employed in SM and 6.5 kV IGBT is utilized in HV switch. In this way, the total device number for three topologies are given in Fig. 5. Obviously, 5-L HMMC has the lowest number of devices, implying the significant reduction of cost and volume.

The amplitude of I_m is determined based on the energy balance of CL and FC. Therefore, multiplying the voltage and current yields the CL output power, and the integral of power indicates the energy fluctuation via (9).

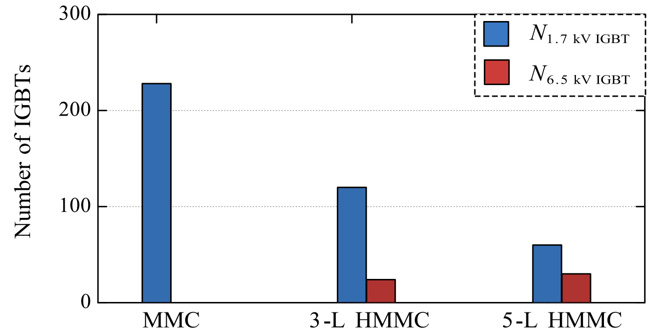


Fig. 5. Comparison of device number for three topologies with 20 kV dc bus.

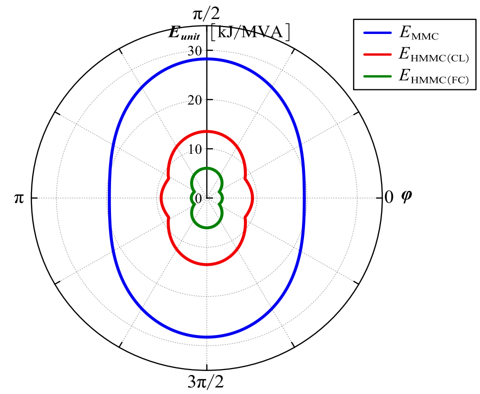


Fig. 6 Numerical analysis of the energy requirement (in kJ/MVA) in the 5-L HMMC and MMC, depending on the ac current phase angle.

$$E = \int_0^{\omega t} (v_{pa} i_{pa}) d(\omega t) \tag{9}$$

It can be observed that the energy of 5-L HMMC is balanced for CL and FC by using the proposed current allocation. The SMs capacitor size is one of the major parameters, which drives the initial investment, weight and size of the MMC. The required CL capacitor energy storage E_{CL} is related to the energy deviation ΔE_{CL} and capacitor voltage deviation coefficient ε in per unit value.

$$E_{CL} = 6N\frac{C_{sm}V_{sm}^{\ 2}}{2S} = \frac{3\Delta E_{CL}}{2\varepsilon S} \tag{10}$$

where S denotes the system apparent power. As for the FC, the capacitor energy storage E_{FC} could be derived similarly.

$$E_{FC} = \frac{3\Delta E_{FC}}{\varepsilon S} \tag{11}$$

where ΔE_{CL} represents the energy deviation of the FC.

The power factor has the influence of CL current, and the total dc-link current of VSC. So the relationship between energy storage E_{unit} and the phase angle φ is plotted in Fig. 6 with ε = 10%. Compared to MMC, the total capacitance reduction based on Fig. 4 at unity power factor is,

$$1 - (47\% + 31\% \cdot 0.5) = 37.5\% \tag{12}$$

The FC does not contribute to the conduction loss and only CL and IGBT loss are calculated as below,

$$P_{con} = V_{on(CL,\ HV\,switch)} \cdot I_{rms(CL,\ HV\,switch)} \tag{13}$$

Where $V_{\text{on(CL, HV switch)}}$ denotes the on-state voltage drop of CL or HV switch, which is estimated to be proportional to the device voltage rating. While $I_{\text{rms(CL, HV switch)}}$ represents the rms value of current flowing through CL or HV switch. More accurate loss calculation could refer to [17]

Above all, the performance of four topologies at unity power factor is summarized in Table I. Compared to the HB-MMC, 5-L HMMC can save 12.5% devices, 37.5% capacitor and 41% conduction losses.

TABLE I
Comparison between MMC and FC-HMMC at unity power factor

Topology		Device voltage	Current (rms)	Capacitance
MMC	CL	1 p.u.	1 p.u.	1 p.u.
3-L HMMC	CL	0.5 p.u.	0.93 p.u.	0.55 p.u.
	HV switch	0.5 p.u.	0.93 p.u.	--
5-L HMMC	CL	0.25 p.u.	1.23 p.u.	0.47 p.u.
	HV switch	0.625 p.u.	0.37 p.u.	--
	FC	--	--	0.155 p.u.

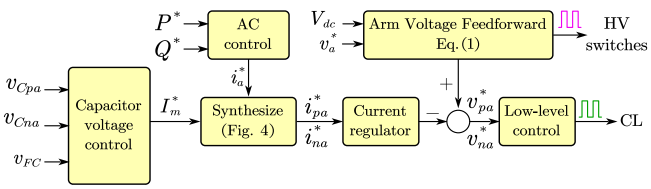


Fig. 7. Overall control block diagram of FC-HMMC as inverter.

D. Control Method

The overall control block diagram of a single-phase 5-L HMMC presented in Fig. 7. The ac side controller calculates the desired ac current based on the active and reactive power reference P^* and Q^*. The sum of upper and lower CL dc-link capacitor voltages are denoted as v_{Cpa} and v_{Cna}, respectively. Capacitor voltage control generates the current reference I_{m}^* to maintain the CL and FC voltage at the rated value. The current regulator should track the synthesized current reference and generates the voltage drop across the arm inductor.

Subtracting this value from the voltage feedforward calculation results yields two CL voltage references v_{pa}^* and v_{na}^*. The low-level control is responsible for the individual SM capacitor voltage balancing and the multilevel modulation.

III. Simulation and Experimental Results

To better illustrate the principle of the proposed 5-L HMMC, a MV simulation case was performed and the electrical parameters are listed in Table II. The steady state waveforms with PF = 0.8 and 1 are shown in Fig. 8. The ac currents are satisfactory, and the CL currents fit well with the designed allocation shape, which indicates the good performance of current controller. The five level CL output voltage of phase *a* in Fig. 8(d) is generated through a phase-shift modulation. The CL capacitor and FC voltages in Fig. 8 (e) and (f) are stabled at the rated value. The transient process of ramping up active power is shown in Fig. 9. It can be seen that the capacitor voltage ripple increases under higher power operation conditions but the average value keeps the same, indicating the effectiveness of the voltage balancing scheme.

TABLE II
Specifications of 5-L HMMC Simulation Model

Parameters	Values	Parameters	Values
Dc voltage	10 kV	SM capacitance	1 mF
Power rating	500 kVA	Arm inductor	3 mH
Ac Voltage	4.8 kV	FC voltage	2.5 kV
SM capacitor voltage	1.2 kV	FC capacitance	0.25 mF
HB number per arm	3	Sampling frequency	15 kHz

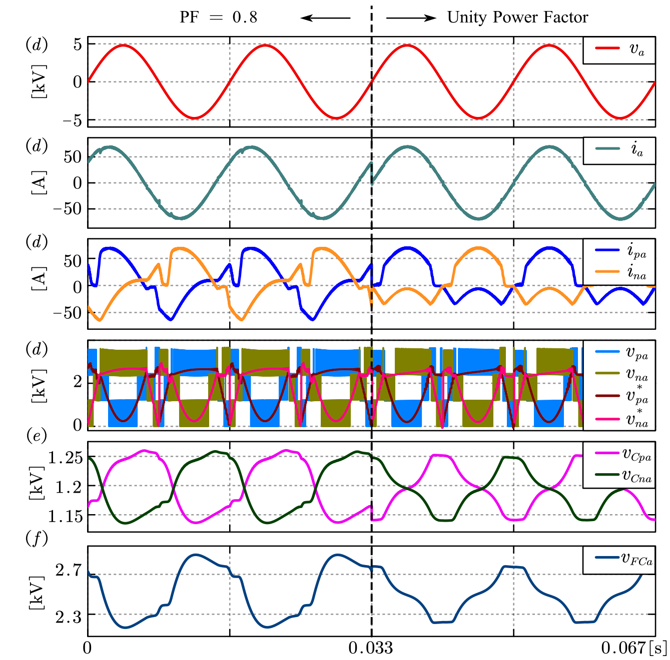


Fig. 8 Steady-state waveforms of single-phase 5-L HMMC, (a) ac side voltages, (b) ac side currents, (c) phase *a* upper and lower CL currents, (d) phase *a* CL and reference voltages, (e) upper and lower CL average capacitor voltages, (f) FC voltage.

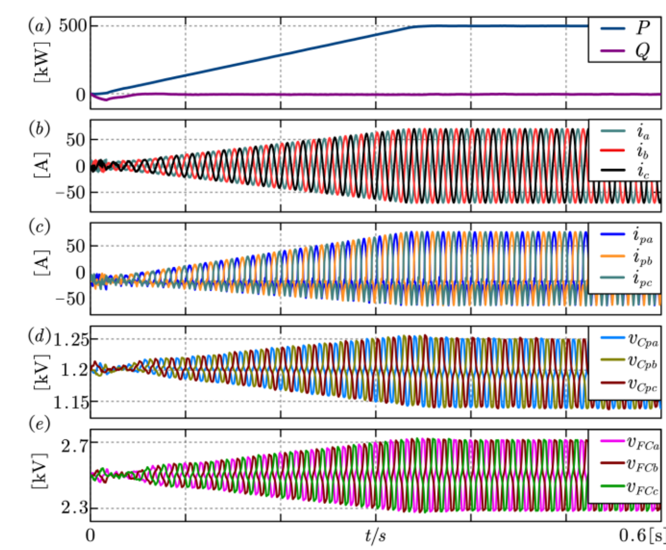


Fig. 9 Dynamic response to the increase of active power, (a) delivered active and reactive power, (b) ac side currents, (c) three-phase upper CL currents, (d) three-phase upper CL dc-link capacitor voltages, (e) three-phase FC voltages.

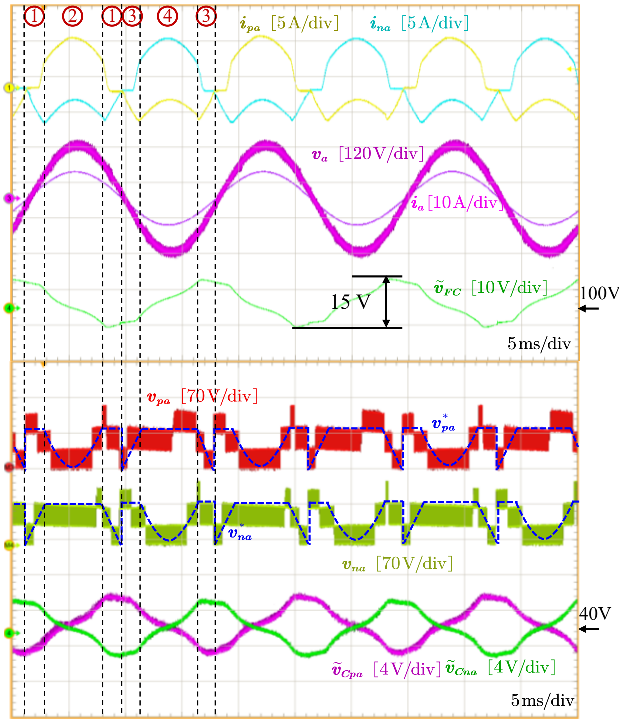


Fig. 10 Steady-state waveforms of 5-L HMMC at unity power factor.

In addition to the simulation, a scale-down prototype was also built. The input dc voltage is 400 V and the ac output voltage amplitude reference is 180 V. Each CL has 3 series HB SMs with 40 V dc-link voltage. A FC with rated voltage of 100V is connected as shown in Fig. 1. The steady-state waveforms of single phase 5-L HMMC are given in Fig. 10. It operates in four modes alternatively. The upper and lower CL currents demonstrate the same shape with the designed pattern, and the ac current has good quality with small distortion. The phase-shift (PS) modulation is employed to generate the four-level CL voltage, which can reduce 75% voltage stress compared to traditional MMC. The capacitor voltage ripple of one SM from upper and lower CLs and FC are also measured, and the dc bias is removed to highlight the ripple shape, which is same with simulation results in Fig. 8.

IV. Conclusions

This paper proposes a novel 5-L HMMC, which belongs to the family of hybrid MMC and is the first five-level member. As the trade-off between the traditional multilevel converter and MMC, all the HV voltage stack in 5-L HMMC operates in line (or double line) frequency, leading to very low switching losses and ease of series connection. The influence of parasitic inductance is also suppressed to simplify the construction difficulty. Compared to MMC, 75% reduction of SM number indicates a significant reduction of the lower cost, conduction losses, and volume, meanwhile retains the excellent output power quality. Therefore, 5-L HMMC shows a great potential in weight or space sensitive MV applications. And this concept could instruct the topology construction of HMMC with higher levels.

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References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[2] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 224-239, 2021.

[3] W. Yao, J. Liu and Z. Lu, "Distributed Control for the Modular Multilevel Matrix Converter," in IEEE Transactions on Power Electronics, vol. 34, no. 4, pp. 3775-3788, April 2019.

[4] J. K. Motwani, B. Fan, Y. Rong, D. Boroyevich, D. Dong and R. Burgos, "Closed-Loop Capacitor Voltage Balancing Scheme for Modular Multilevel Converters Operated in Switching-Cycle Balancing Mode," in IEEE Transactions on Power Electronics, vol. 38, no. 5, pp. 5603-5608, May 2023.

[5] J. Liu, S. Yue, W. Yao, W. Li and Z. Lu, "DC Voltage Ripple Optimization of a Single-Stage Solid-State Transformer Based on the Modular Multilevel Matrix Converter," in IEEE Transactions on Power Electronics, vol. 35, no. 12, pp. 12801-12815, Dec. 2020, doi: 10.1109/TPEL.2020.2992707.

[6] J. Liu, D. Dong and D. Zhang, "Hybrid Modular Multilevel Rectifier: A New High-Efficient High-Performance Rectifier Topology for HVDC Power Delivery," in IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 8583-8587, Aug. 2021.

[7] X. Zhao, R. Phukan, C. -. W. Chang, R. Burgos, D. Dong and P. Asfaux, "Design and Optimization of 2×211-kW SiC-Based Aircraft Propulsion Inverter System with High Power Density and High Efficiency," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1009-1016.

[8] X. Zhao et al., "Design of Ultra-Compact Gate Driver Integrated with Current Sensor and Commutation Path for a 211-kW Three-Level SiC Aircraft Propulsion Inverter," in IEEE Journal of Emerging and Selected Topics in Power Electronics, doi: 10.1109/JESTPE.2023.3247378..

[9] H. Tian, Y. Li and Y. W. Li, "Commutation Scheme of Seven-Level Hybrid-Clamped Converters With Suppressed Deadband-Induced Voltage Spikes," in IEEE Transactions on Industrial Electronics, vol. 68, no. 12, pp. 11663-11672, Dec. 2021.

[10] X. Zhao, C. -W. Chang, R. Phukan, R. Burgos and D. Dong, "An Enhanced PWM Scheme of Three-Level T-Type Inverter for Loss Balance and Reduction," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 231-236.

[11] P. Bakas et al., "Review of Hybrid Multilevel Converter Topologies Utilizing Thyristors for HVDC Applications," in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 174-190, Jan. 2021.

[12] M. M. C. Merlin et al., "The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," in IEEE Transactions on Power Delivery, vol. 29, no. 1, pp. 310-317, Feb. 2014.

[13] M. M. C. Merlin et al., "The Extended Overlap Alternate Arm Converter: A Voltage-Source Converter With DC Fault Ride-Through Capability and a Compact Design," in IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 3898-3910, May 2018.

[14] D. Zhang, D. Dong, R. Datta, A. Rockhill, Q. Lei and L. Garces, "Modular Embedded Multilevel Converter for MV/HVDC Applications," in IEEE Transactions on Industry Applications, vol. 54, no. 6, pp. 6320-6331, Nov.-Dec. 2018.

[15] J. Yang, Z. He, J. Ke and M. Xie, "A New Hybrid Multilevel DC–AC Converter With Reduced Energy Storage Requirement and Power

Losses for HVDC Applications," in IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2082-2096, March 2019.

[16] P. Sun, Y. Tian, J. Pou and G. Konstantinou, "Beyond the MMC: Extended Modular Multilevel Converter Topologies and Applications," in IEEE Open Journal of Power Electronics, vol. 3, pp. 317-333, 2022.

[17] J. Liu, D. Dong and D. Zhang, "A Hybrid Modular Multilevel Converter Family With Higher Power Density and Efficiency," in IEEE Transactions on Power Electronics, vol. 36, no. 8, pp. 9001-9014, Aug. 2021.

[18] J. Liu, D. Dong and D. Zhang, "Control of Hybrid Modular Multilevel Converter and its Capacitor Voltage Balancing," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 800-806.

[19] J. Liu, D. Zhang and D. Dong, "Modeling and Control Method for a Three-Level Hybrid Modular Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 37, no. 3, pp. 2870-2884, March 2022.

[20] J. Liu, D. Zhang and D. Dong, "Analysis of Hybrid Modular Multilevel Rectifier Operated at Nonunity Power Factor for HVDC Applications," in IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 10642-10657, Sept. 2022.

[21] J. K. Motwani, J. Liu, R. Burgos, Z. Zhou and D. Dong, "Hybrid Modular Multilevel Converters for High-AC/Low-DC Medium-Voltage Applications," in IEEE Open Journal of Power Electronics, vol. 4, pp. 265-282, 2023.

[22] J. Liu, J. K. Motwani, R. Burgos, Z. Zhou and D. Dong, "A New Hybrid Modular Multilevel Rectifier as MVAC-LVDC Active Front-End Converter for Fast Charging Stations and Data Centers," in IEEE Transactions on Power Electronics.

[23] J. Liu and D. Dong, "A Flying Capacitor Hybrid Modular Multilevel Converter With Reduced Number of Submodules and Power Losses," in IEEE Transactions on Industrial Electronics, vol. 70, no. 4, pp. 3293-3302, April 2023.

[24] J. Liu and D. Dong, "A Line-Frequency Commutated HV VSC Embedded Modular Multilevel Converter With DC Fault Blocking Capability," in IEEE Transactions on Power Electronics, vol. 37, no. 9, pp. 10727-10737, Sept. 2022.