Second-order Level-crossing Sampling Analog to Digital Converter for Electrocardiogram Delineation and Premature Ventricular Contraction Detection

Xiaochen Tang, *Member, IEEE,* Mario Renteria-Pinon, *Student Member, IEEE,* and Wei Tang, *Member, IEEE*

***Abstract*—This paper presents an electrocardiogram (ECG) delineation and arrhythmia heartbeat detection system using a novel second-order level-crossing sampling analog to digital converter (ADC) for real-time data compression and feature extraction. The proposed system consists of the front-end integrated circuit of the data converter, the delineation algorithm, and the arrhythmia detection algorithm. Compared with conventional level-sampling ADCs, the proposed circuit updates tracking thresholds using linear extrapolation, which forms a second-order level-crossing sampling ADC that has sloped sampling levels. The computing is done digitally and is implemented by modifying the digital control logic of a conventional Successive-approximation-register (SAR) ADC. The system separates the sampling and quantization processes and only selects the turning points in the input waveform for quantization. The output of the proposed data converter consists of both the digital value of the selected sampling points and the timestamp between the selected sampling points. The main advantages are data savings for the data converter and the following digital signal processing or communication circuits, which are ideal for low-power sensors. The test chip was fabricated using a 180nm CMOS process. When sensing sparse signals such as ECG signals the proposed ADC achieves a compression factor of 8.33. The delineation algorithm uses a triangle filter method to locate the fiducial points and measures the intervals, slopes, and morphology of the QRS complex and the P/T waves. Those extracted features are then used in the arrhythmia heartbeat detection algorithm to identify Premature Ventricular Contraction (PVC). The overall performance of the system is evaluated using the MIT-BIH database and the QT database, which is also compared with the recently reported systems. The accuracy, sensitivity, specificity, PPV, and F1 score are 97.3%, 89.6%, 97.8%, 73.3%, and 0.81 for detecting PVC.**

***Index Terms*—Analog-to-digital converter (ADC), Second-order Level-crossing Sampling, Nonuniform Sampling, Sparse Signal, Sensors, ECG delineation, Fiducial Points, Machine Learning**

I. Introduction

CARDIOVASCULAR disease (CVD) is one of the primary challenges in human health, which is also the leading cause of death [1]. To better monitor the health status of the heart, wearable electrocardiogram (ECG) monitoring devices have been expected to track the ECG waveform and classify different types of arrhythmic heartbeats [2]–[6]. However, the current market solutions are not able to perform such tasks without sending raw data to the cloud for further processing. Such operations limit the battery life and the duration of ECG monitoring since wireless communication consumes too much power [7]–[9]. Therefore, on-sensor processing capabilities are anticipated in the next-generation wearable devices. Such devices should be able to obtain the ECG waveform in the digital format and perform preliminary arrhythmia classification. Only the raw waveform of the suspicious arrhythmic heartbeats should be sent to the cloud to save the limited sensor power. Thus, the wearable ECG sensor should contain the analog-to-digital converter (ADC), digital signal processing units, and the radio communication module. Design challenges should be addressed by synergetic efforts across different sub-modules.

Arrhythmia classification systems have been intensively studied based on different algorithms [10]–[13]. Besides wavelet methods [14], recently deep learning methods [15]–[18] have been reported for detecting arrhythmic heartbeats. [19] proposed a low-power heartbeat detection system and [20], [21] proposed analog processing methods for QRS detection. However, deep-learning methods usually don't have interpretable intermediate results for human experts as references, which makes them difficult to be adopted by medical providers in decision-making. Moreover, both deep-learning methods and wavelet methods are difficult to be implemented on sensors since they both need a large size memory for storing temporary data and both have a high computing overhead, which results in high power consumption. To better meet the expectation, an algorithm should use smaller digital memory, have a low computing overhead, and provide interpretable intermediate results that could be understood by human experts. For example, medical providers use fiducial points of the ECG waveform to identify intervals such as QRS complex and PR interval. Such information should be generated by the algorithm for making decisions.

On the hardware side, one of the primary challenges in low-power sensors is that the ADC generates a large number of unessential data that overloads the following digital processing, storage, and communication circuits. For example, Nyquist sampling ADC records digital data at every sampling clock for quantization, which may not be necessary if the input signal is sparse in the time domain. Most recent ECG signal processing methods are based on data sampled by a fixed

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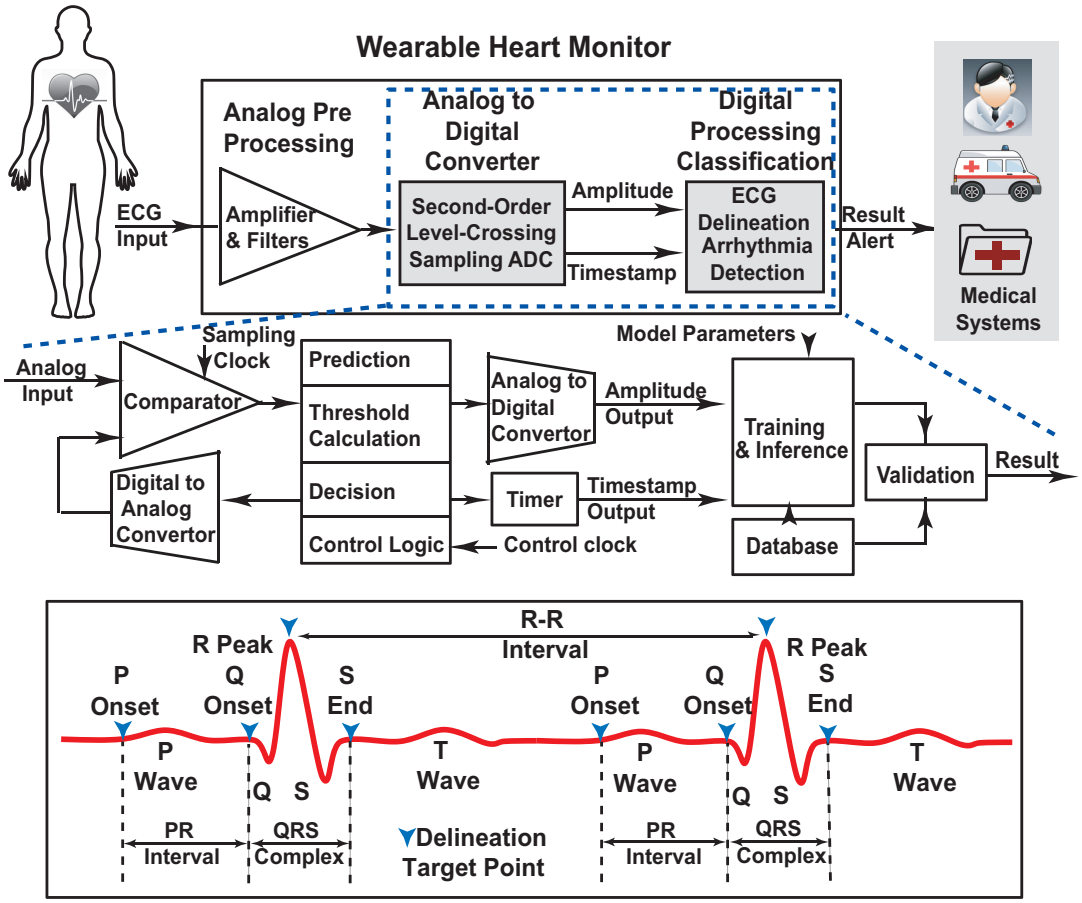

Fig. 1. (Top) Wearable heartbeat monitor system; (Middle) The scope of this work focusing on the second-order level-crossing sampling ADC for delineation and arrhythmia detection, (Bottom) ECG Delineation highlighting the key fiducial points and intervals. Modified from [32].

clock. For example, [22] proposed a neural-network-based cardiac arrhythmia classification system while [23] presents a clinician-like cardiac arrhythmia watchdog system based on detecting the P-QRS-T waves. To reduce the amount of data output, level-crossing sampling ADCs [24]–[28] are proposed. When the input signal is crossing predefined voltage levels, the ADC records one-bit sign data and the timing information of such an event. However, level-crossing Sampling ADCs cannot identify the location of turning points in the input signal [25] since usually the gaps between the sampling levels are much larger than the resolution in a Nyquist sampling ADC. Moreover, level-crossing ADCs may also generate unnecessary samplings when the input signal has a low-frequency high-amplitude baseline wandering or high-frequency low-amplitude noise around the sampling level. Dedicated data compression circuits after ADC may bring additional power and data storage costs [29]. Signal-depended nonuniform sampling methods were proposed to select the turning points based on tracking the slope in the waveform [30], [31]. However, such a method requires complicated analog circuitry for calculating divisions to obtain the slope information, which is susceptible to analog noise and errors.

To address these problems, we propose a second-order level-crossing sampling ADC [33], which selects turning points of the analog input signal for quantization while skipping sampling points that are in a linear portion in either time or amplitude domain. The proposed ADC computes the digital prediction of a sampling point based on prior quantized or predicted sampling points to decide if quantization is needed for the current sampling point. The decision is made using upper and lower thresholds calculated digitally by the predicted value and a prior defined Delta threshold value. Both the amplitude data of the selected sampling points and the timestamp data between selected sampling points are the output data of the system. By doing so, the ADC greatly reduces the output data amount for sensing sparse signals. Using data generated by the proposed second-order level-crossing sampling ADC including both the amplitude and the timestamp data, we proposed a novel delineation and arrhythmia heartbeat detection algorithms. The main difference between the proposed method and other ECG processing methods is that the proposed system output is nonuniformly sampled digital data sequences. If conventional digital signal processing methods are applied, the system needs to perform interpolation and convert the nonuniformly sampled data to uniform sampled data. Such a process cancels the advantage of the second-order level-crossing sampling which identifies only turning points of the input signal. Therefore, we proposed the triangle-recognizing method for ECG signal processing, including delineation and arrhythmia detection. The proposed algorithm includes

triangle-based filters and a P-wave detection algorithm, which provides interpretable intermedium results for human experts.

This paper is expanded from our previous work [33] of the second-order level-crossing sampling ADC. In this paper, we extended the scope of [33] by adding the processing algorithms including both the ECG delineation and arrhythmia heartbeat detection. The primary contribution of the paper includes: (1) Applying the second-order level-crossing sampling ADC for ECG monitoring; (2) Implementing a real-time data acquisition and reconstruction system on an FPGA to collect data from the second-order level-crossing sampling ADC; (3) Characterizing the delineation and arrhythmia detection algorithms using the data format of the second-order level-crossing sampling ADC. The remaining paper is organized as follows. Section II presents the second-order level-crossing sampling ADC architecture and circuit implementation, as well as the ECG processing algorithm. Experimental results are presented in Section III. Section IV discusses and compares the performance with related works. Section V concludes the paper.

II. Circuit and System Design

The overall system building blocks are shown in Fig. 1. The system focuses on the front-end Analog-to-Digital Conversion (ADC) and the back-end Digital Processing for arrhythmia detection. We assumed that the front-end amplifier and filters provide an amplified analog ECG waveform. The proposed ADC uses prediction and pre-defined thresholds to select turning points from the analog waveform for quantization. The quantized amplitude data and the timestamp data are then sent to digital signal processing units for arrhythmia detection. The arrhythmia detection algorithm uses triangle-recognizing methods to perform delineation and arrhythmia detection. The results from the detection are recorded and compared using the benchmark databases. Also, the comparator needs a sampling clock and the control logic needs a faster clock for prediction and SAR logic. The algorithm needs model parameters stored in the system. The following paragraphs present the circuit and system design of the second-order level-crossing sampling ADC, and the algorithm design using the proposed ADC.

A. Second-order Level-crossing Sampling ADC Architecture

The difference between the conventional Nyquist rate ADC, the level-crossing ADC, and the proposed Second-order Level-crossing ADC is shown in Fig. 2. In the conventional Nyquist rate ADC, each sampling is quantized into multi-bit binary data using the standard quantization process. The output of the Nyquist rate ADC is the digital data sequence of each sampling point as shown in Fig. 2 (a). In the level-crossing sampling ADC, the analog input is compared to a pre-defined group of thresholds. When the input signal is crossing a threshold, the direction of the crossing is recorded as one-bit data (rising or falling). The timing between each crossing is recorded as the timestamp. So its output is one-bit direction data and multi-bit timing data for each sampling as shown in Fig. 2 (b). In the proposed Second-order Level-crossing sampling ADC, sampling is performed using a fixed clock like in a

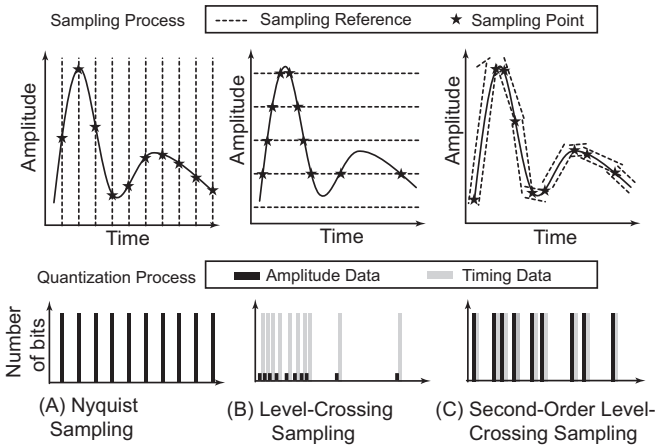

Fig. 2. Comparing the sampling and quantization process of (a) Nyquist Sampling, (b) Level-crossing sampling, and (c) the proposed Second-order level-crossing sampling ADCs.

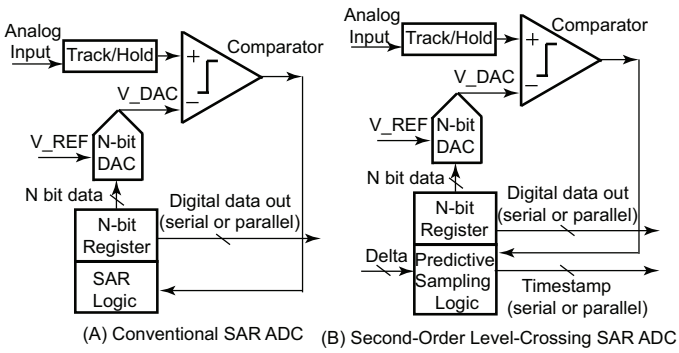

Fig. 3. The digital logic in a conventional SAR ADC (A) can be modified to implement the proposed second-order level-crossing sampling ADC (B).

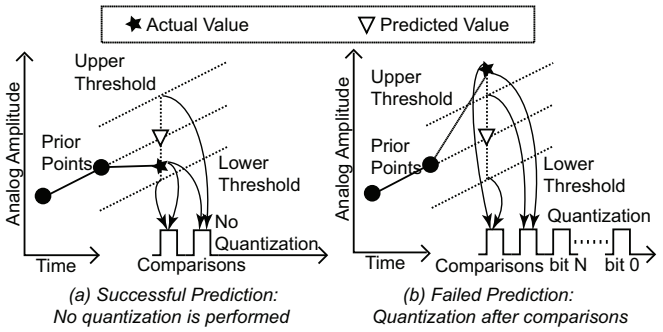

Fig. 4. Prediction and quantization: (A) only two comparisons are needed if the prediction is successful, no quantization is performed; (B) when prediction fails, quantization is performed using the SAR logic.

Nyquist rate ADC. The circuit generates predictions to find the turning points of the analog waveform. Only the turning points in the analog waveform are selected for quantization. The timing between the selected points is also recorded. Therefore, the output of the proposed ADC contains both the multi-bit amplitude data and the multi-bit timestamp data, but only for the turning points, this could greatly save the output data amount when the input signal is sparse in either the time domain or the frequency domain as shown in Fig. 2 (c).

The proposed second-order level-crossing sampling architecture includes the analog comparator, the N-bit DAC, the digital control logic for calculating predictions and thresholds,

and the timer for recording timestamps between quantized sampling points. Fig. 3 presents the difference between the conventional SAR ADC and the proposed second-order level-crossing sampling ADC. The primary difference is in the digital control logic, where the second-order level-crossing sampling system has an extra digital input of Delta and an additional output as the timestamp. The control logic of the proposed ADC predicts the digital value of the analog input from two prior digital values using linear extrapolation, as shown in Fig. 4. Then the control logic calculates the digital values of an upper threshold by adding the Delta value to the predicted digital value. The upper threshold digital value is converted into analog value using the DAC, and then compared with the analog input. Similarly, a lower threshold is generated by subtracting Delta from the predicted digital value, which is also converted into analog value and compared with the analog input.

If the analog input is within the window between the upper threshold and the lower threshold, the prediction is successful and no further quantization is performed by the ADC. The system uses the predicted value as the digital results of the current sampling. The successfully predicted digital value is stored for the next prediction. If the analog input is out of the threshold window, the prediction fails. In such a case, full quantizations must be made for the current sampling and the next sampling to restart the prediction process. The quantization result of the first sampling becomes the digital data output while the duration between unsuccessful predictions becomes the digital timestamp output.

In a conventional N-bit SAR ADC, for each sampling, the control logic needs to use the DAC N times. The comparator also needs to perform N comparisons. In contrast, the second-order level-crossing sampling ADC only uses the DAC and comparator twice for the upper and lower thresholds comparisons if the two comparisons are both successful. In such a case, no further Digital-to-Analog conversions and comparisons are necessary. Nevertheless, if the prediction is not successful, the prediction and the 2 comparisons are wasted. Therefore, the proposed ADC saves power and data only when the input signal has a higher portion of the linear region, which is generally true for most of the sparse signals.

B. Integrated Circuit of the second-order level-crossing ADC

The proposed second-order level-crossing sampling ADC is designed by modifying a conventional fully-differential 10-bit switched-capacitor SAR ADC similar to [34]. The circuit consists of a comparator, a fully-differential digital-to-analog converter, and a digital control logic. The schematic of the digital-to-analog converter is shown in Fig. 5 (a) and the dynamic comparator is shown in Fig. 5 (b). In our design, the 295 fF Metal-Insulator-Metal Capacitors (MIMCAPs) with an area of 12 μm $\times$ 12 μm are used as unit capacitors, which is also the value of C_0, C_1, C_6, and C_S. As in a split capacitor array, C_2 and C_7 are twice the unit capacitors. C_3 and C_8 are four times the unit capacitors. C_4 and C_9 are eight times the unit capacitors. C_5 and C_{10} are 16 times the unit capacitors. In the DAC, $Ref+$ and $Ref-$ can be connected to either the

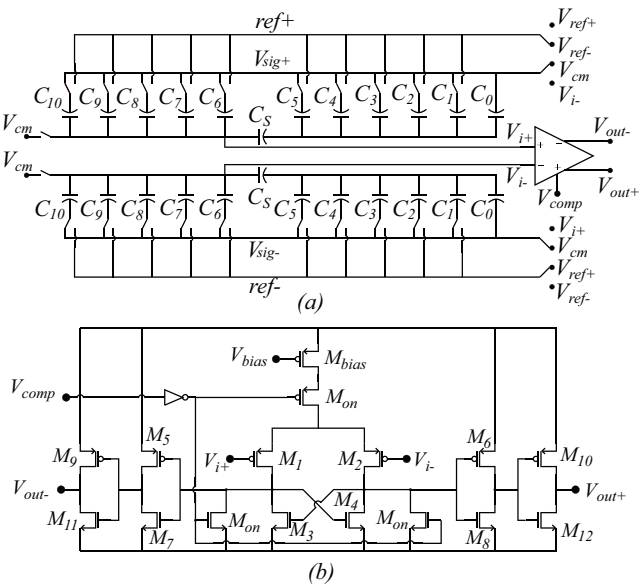

Fig. 5. Schematic of the fully differential DAC (A) and the dynamic comparator (B) in the fabricated second-order level-crossing ADC.

positive reference voltage (V_{ref+}) or the negative reference voltage (V_{ref-}). V_{sig} can be connected to the input signal or the common mode voltage. V_i is the input signal. In the data conversion process, the DAC first converts the upper threshold digital values into an analog voltage. The sampled input voltage is then compared with the high-threshold voltage using the comparator. Then the second data conversion and comparison are performed for the low-threshold voltage. If the input voltage is out of the window formed by the thresholds, the conventional SAR quantization process is enabled for the current sampling and the next sampling. The SAR quantization process needs ten comparisons to determine the 10-bit digital values in a reserved quantization timing window. Otherwise, if the input voltage is in the threshold window, the whole circuit is set in sleep mode. One of the main differences between the proposed second-order level-crossing system and an asynchronous level-crossing ADC is that the proposed system performs sampling at a fixed rate. So the comparator only works at a specific timing window to compare analog values like in a SAR ADC. This is done by the control logic that turns off the comparator using the enable signal $Vcomp$. If the prediction is successful, the comparator is turned off during the reserved timing window for quantization, which greatly saves the comparator power.

C. Real-time ECG Monitoring Algorithms

This section presents a real-time ECG monitoring system based on the second-order level-crossing sampling ADC. The algorithms contain QRS complex detection, ECG delineation, and a premature ventricular contraction heartbeat recognizer. Our idea of performing delineation is to find the triangles that belong to the P wave and the QRS complex. The second-order level-crossing sampling reports the turning points in the analog waveform, which are potential fiducial points. But these points could also be common turning points due to

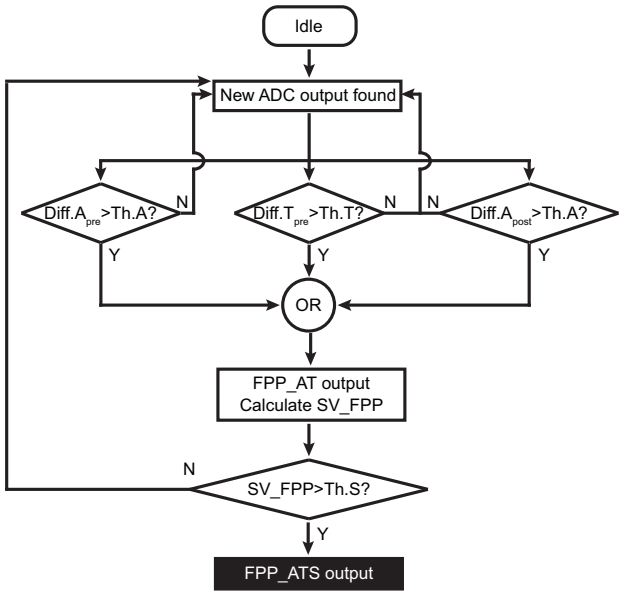

Fig. 6. Fiducial Points Pruning Algorithm Flow Chart.

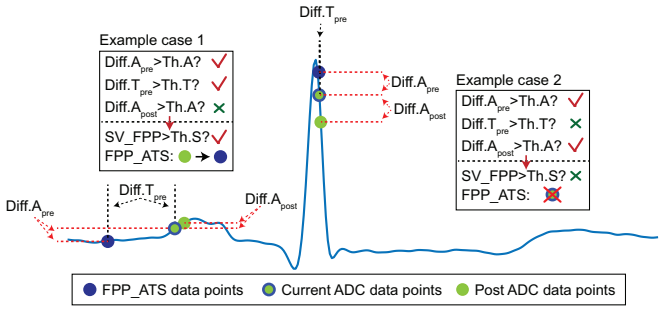

Fig. 7. Visual Illustration of Fiducial Points Pruning Algorithm.

baseline wandering or noise, which are not fiducial points. To determine if a potential fiducial point is a real fiducial point, the system needs to find the triangles of each wave including the onset, peak, and end-point. Only when a triangle meets the requirement (location, height, and width), the three points of the triangle could then be determined as fiducial points.

1) Heartbeat Rate detection: One of the most significant jobs of wearable ECG monitoring systems is detecting heartbeat. Most ECG processing algorithm depends on the successful detection of the QRS complex. In the proposed system, firstly the proposed ADC converts the input ECG signal to the amplitude and timing data of turning points. A proposed Fiducial Points Pruning (FPP) filter eliminates data points that do not contribute much information (may be originated from baseline wandering or noise). Then, a hardware-efficient algorithm, Vertex-side Triangulation Identifier (VsTI), is implemented in the proposed system to form the data into consecutive triangle data patterns. With a Neighbor Triangle Merging (NTM) algorithm, the data volume is further reduced. Thus, with specific triangle patterns recognizing rules, triangles representing QRS complexes are selected, achieving QRS detection and heartbeat rate calculation in real time.

2) Fiducial Points Pruning (FPP) Filter: As shown in the operation flow chart of the FPP filter in Fig. 6, the goal of the proposed FPP filter is to eliminate the neighbor sampling points that may originate from baseline wandering or noises. These data points usually have similar amplitude and appear very close to each other. Moreover, the slopes between these data points with their previous and post data usually have no significant change. The FPP filter operation has two steps. Firstly, the FPP keeps monitoring the second-order level crossing ADC output; when new ADC output data is recorded, FPP calculates the difference between the current ADC output and previous FPP-filtered data. Then it calculates the difference between the current and the next ADC output. The initial ADC data is considered the first FPP data. Then three parameters are calculated: (1) the amplitude difference between the prior FPP data and the current ADC data, which is named as $Diff.A_{pre}$; (2) the amplitude difference between the next ADC data and the current ADC data, which is named as $Diff.A_{post}$; and (3) the time difference between the current ADC data and the prior FPP data, which is named as $Diff.T_{pre}$. After that, $Diff.A_{pre}$ and $Diff.A_{post}$ are compared with a pre-defined amplitude threshold value $Th.A$, while $Diff.T_{pre}$ is compared with a pre-defined timing threshold value $Th.T$. If either the amplitude difference or timing difference is larger than the pre-defined threshold values, the current ADC output and timestamp data are temporarily reserved as amplitude and time data FPP_AT, operation proceeds to the next slope variation check step.

In the slope variation check, by calculating the slope variation $SV\_FPP\_AT = abs(Diff.A_{post}/Diff.T_{post} - Diff.A_{pre}/Diff.T_{pre})$, and comparing the SV_FPP_AT with a defined slope threshold $Th.S$, we obtain the final filtered output (FPP_ATS) so that redundancy data points are further eliminated. If all these comparisons were failed, the system starts searching with a new ADC output. The features of $Diff.A_{pre}$, $Diff.A_{post}$, and $Diff.T_{post}$ are based on the morphology of the ECG signal. To identify the P wave and QRS complex, the algorithm searches possible triangles of these waves. For example, a P wave should have reasonable amplitude, duration, and location. $Diff.A_{pre}$ and $Diff.A_{post}$ are used to identify the amplitude while $Diff.T$ is applied for calculating the timing information. The visual illustration of the FPP algorithm is shown in Fig. 7.

3) Vertex-side Triangulation Identifier (VsTI): With the proposed FPP filter, the filtered data points keep the critical information of the input waveform. Next, we propose the VsTI algorithm to identify the triangle shape in the input waveform. The operation flow chart of VsTI's core algorithm is shown in Fig. 8 and the visual illustration of the algorithm is shown in Fig. 9. The VsTI follows a procedure of triangle identification by searching left-middle-right vertices. During the FPP filter operation, the amplitude and time difference $Diff$, and slope variation of data SV_FPP are calculated and saved. The left vertex $Vertex\_left$ searching starts from obtaining the amplitude and timing difference data of $Diff.A$ and $Diff.T$ in SV_FPP. The system compares $Diff.A$ and $Diff.T$ with defined threshold values $Th_V.A$ and $Th_V.T$ respectively to decide if the current point is $Vertex\_left$. Then, $Vertex\_middle$ is selected by finding the data point that has the maximum amplitude in the following negative SV_FPP vector V_svn. Finally, in the consecutive following

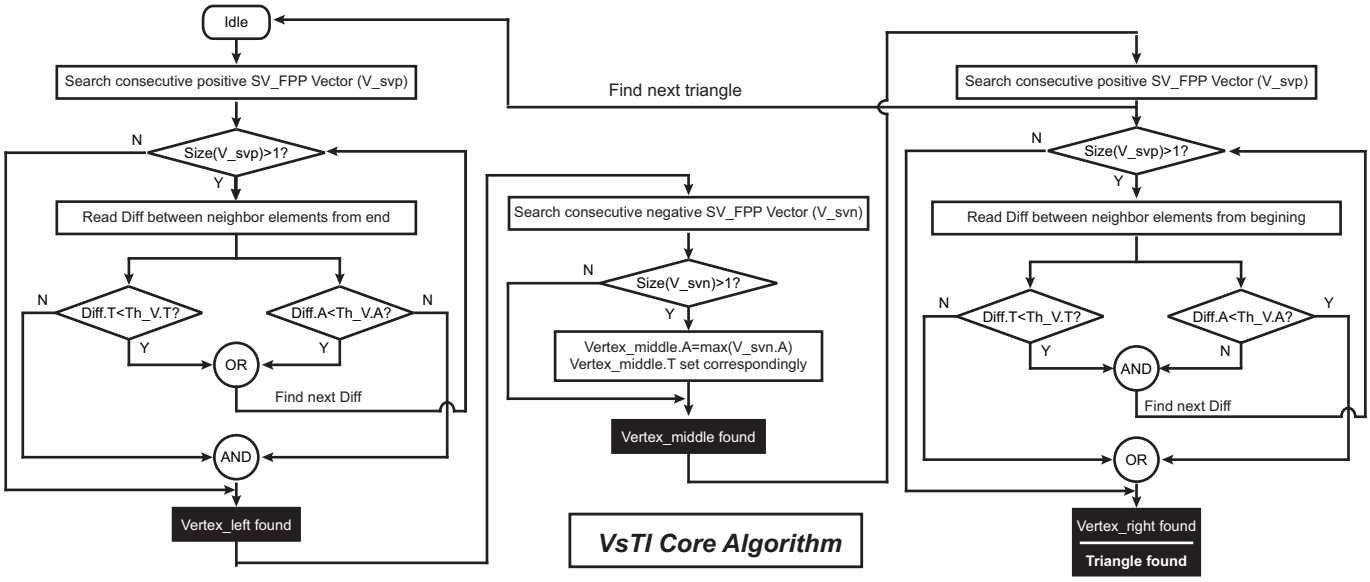

Fig. 8. Vertex-side Triangulation Identifier Algorithm Flowchart.

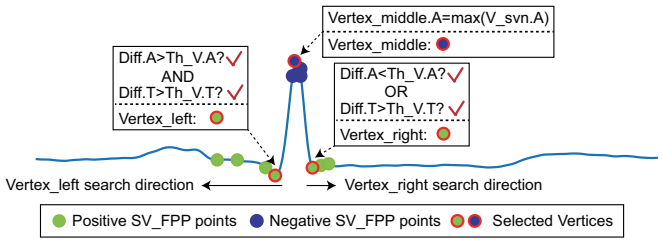

Fig. 9. Visual Illustration of Vertex-side Triangulation Identifier Algorithm.

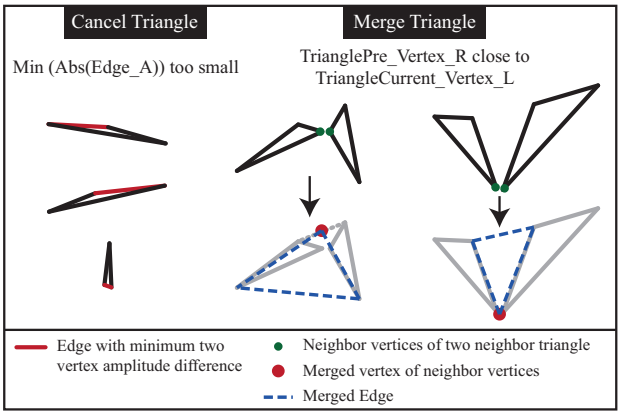

Fig. 10. Neighbor Triangle Merging Algorithm.

V_svp, the first data point of the first grouped data is selected as the $Vertex\_right$. It is noticed that the last V_svp is also used to identify the $Vertex\_left$ of the next triangle data pattern.

The proposed VsTI algorithm also includes a neighbor triangle merging algorithm (NTM) to reduce the triangle pattern volume further, as described in Fig. 10. Minimum edge length is used to approximately evaluate the area of VsTI-identified triangles. If the triangle has one side that is smaller than the defined threshold in time or amplitude, the triangle is abandoned. Moreover, if two neighbor triangles are very close to each other, they are merged as shown in Fig. 10. The side selection of the merged triangle is decided by identifying the amplitude pattern of $Vertex\_left$ and $Vertex\_right$, and the $Vertex\_middle$ is calculated using the mean value of the two neighbor vertices.

4) QRS Complex detection: Once triangle data patterns are generated by the proposed VsTI, QRS complexes are selected from the triangles based on two rules: 1) the base of the triangle should be shorter than the defined QRS duration threshold; 2) approximate triangle height (calculated by the amplitude difference between $Vertex\_middle$ and the mid-point of $Vertex\_left$ and $Vertex\_right$) should be greater than the defined QRS height threshold. These two rules can effectively identify the QRS complex from the input ECG waveform.

D. ECG delineation and PVC identification algorithm

Using the same method for QRS complex detection, we perform ECG delineation with the help of VsTI, but with different threshold values for the identification of triangle data patterns and triangle merging. Then, the triangles found within the specific timing window ahead/following the detected QRS complex are regarded as P/T waves. Next, we can extract fiducial point timing information by mapping each waveform's onset/peak/end with $Vertex\_left$, $Vertex\_middle$, and $Vertex\_right$ of each triangle. By doing these, the system locates all fiducial points and completes the ECG delineation.

Premature Ventricular Contraction (PVC) is a type of arrhythmia; usually, when the ventricles contract prematurely, or before the normal heartbeat initiated by the sinus node, the QRS complex that represents the depolarization process of ventricles appears in different morphology. PVC may cause palpitations, chest discomfort, shortness of breath, or no symptoms [35]. Thus in some cases, PVCs can be used as indicators of the level of stress, caffeine, alcohol, or underlying heart disease. PVC can usually be identified as a bizarre QRS complex between normal QRS complexes. The duration of the QRS complex in PVC is usually longer than 120 ms. The R

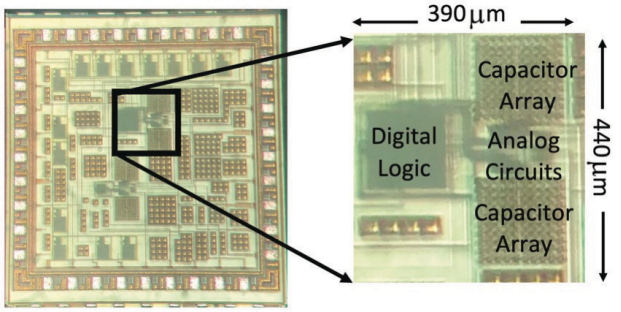

Fig. 11. Chip microphotograph with the highlighted core area.

peak in PVC is usually not aligned with the location of other R peaks, which results in variations in RR intervals. Since PVCs are usually sporadic events, the average heartbeat rate can be normal. Therefore, we applied three rules for detecting PVCs from normal heartbeats: 1) calculated heartbeat rate is 60-100 beats/min; 2) QRS duration larger than 120 ms; 3) Pre/Post RR interval has obvious difference and Pre RR interval is shorter. All these rules can easily be calculated using the Second-order Level-crossing sampling ADC data by simply calculating the duration of RR intervals and QRS complex after delineation. We propose a light-weighted PVC identification algorithm as our arrhythmia detection case study, by taking advantage of the proposed FPP filter and VsTI algorithm. The light-weighted algorithm checks the morphology of the detected QRS complex and ECG delineation results and is implemented hardware-efficiently.

III. Experimental Result

The prototype chip was fabricated using a 180 nm CMOS process. The chip microphotograph is shown in Fig. 11. The whole chip is 1.5 mm $\times$ 1.5 mm including the test structure and the pad frame. The Core area of the ADC is 390 μm x 440 μm. The power supply is 1.8 V. The functionality of the chip can be evaluated using two methods, one without the timestamp and one with the timestamp. In the first method, without using the timestamp output, if the prediction is successful, the chip sends the predicted value as the data output, which usually forms linear slopes. If the prediction fails, the chip performs full quantization as a regular SAR ADC and sends the actual digital value as the data output. Quantization events are also recorded in a digital pulsethe sequence. Most of ECG signal bandwidth is within 100 Hz [36]. The sampling frequency is 1 kHz and the internal clock for the SAR and prediction logic is 16 kHz. The FPGA has a data buffer that imports the data from the chip. We used the Opal Kelly FPGA Board which uses the USB2.0 protocol to send data from the FPGA to the computer. The digital output was sent to an external DAC for the reconstruction of the analog input. Fig. 12 (top) presents the measured result of a 1-Hz 900 mVpp ECG signal from a signal generator with different Delta values. The predicted output signal shows that with a 900 mV amplitude ECG signal, a 50 mV Delta is able to keep the morphology of the waveform for arrhythmia heartbeat detection. A 200 mV Delta is not acceptable since it introduces distortion in the reconstructed waveform.

A. Real-time Data Acquisition and Reconstruction

The above data acquisition method using the predicted digital output does not take advantage of timestamps in data saving. A real-time data acquisition system using the timestamp is developed and its block diagram is shown in Fig. 13. In the system, an FPGA integration module is used to realize output data acquisition. Two first-in-first-out (FIFO) memory arrays are implemented on the FPGA. Memories are used to temporarily store the amplitude data and the timestamp information for later data packet communication. The length of each array is 10 bits and there are 2^N array elements on each memory. Both amplitude data and timing information are saved continuously when there is a quantization event. In a worst-case scenario, for example, at a sampling rate of 1000 samples per second and 2^{12} = 4096 array elements, the memory should save at least 4 seconds of data.

Real-time data acquisition is achieved by pipe-lining data from the FPGA integration module to a computer using an Application Programmer's Interface (API), designed in C++. When the program starts in the computer, the FPGA is programmed and the fabricated chip starts working. Data is first stored in the respective memories. When the memory arrays are full, data transfers from the FPGA to the computer and saves in a CSV file. To comply with the communication protocol of the integration module, synchronous communication is done by transferring 2-byte words at a time until the whole memories are transferred. Output signal reconstruction starts by processing the data in the CSV file. First, the 10 bits of amplitude data and the 10 bits of timing information are extracted from the file. The amplitude data binary numbers are transformed into voltage values. The timing binary numbers are transformed into milliseconds by first converting the binary values to decimal values, then multiplying each number by the sampling time (1 ms), and performing a cumulative sum of all values. Data is then plotted using the calculated amplitude and timing values. The reconstruction of the output signal of the proposed system is done by linear data interpolation.

The real-time data acquisition experiment using the timestamp is composed of a RIGOL 4102 waveform generator that creates a 1Hz ECG signal with an amplitude of 900mV and a DC offset of 900mV. This signal is fed into the fabricated chip, where a 10-bit SAR ADC is implemented with the proposed second-order level-crossing sampling logic. The data is read by an Opal Kelly XEM6001 integration module. The XEM6001 uses a Xilinx Spartan-6 FPGA and the system clock used for communication is set at 48MHz. The custom API used for data acquisition is designed in C++, using the FrontPanel API modules compatible with the XEM6001. Communication is done via USB 2.0. Data transfers from the FPGA memories to a CSV file, every time the memories are full. The transfer clock is equal to the system clock of the integration module. Meaning, the whole memory is transferred orders of magnitude faster than the data being saved on the FPGA, minimizing the loss of data. Once the data is saved in a CSV file, MATLAB is used to process and plot the data. Fig. 14 shows the experiment setup.

Real-time data acquisition of a Nyquist sampling conven-

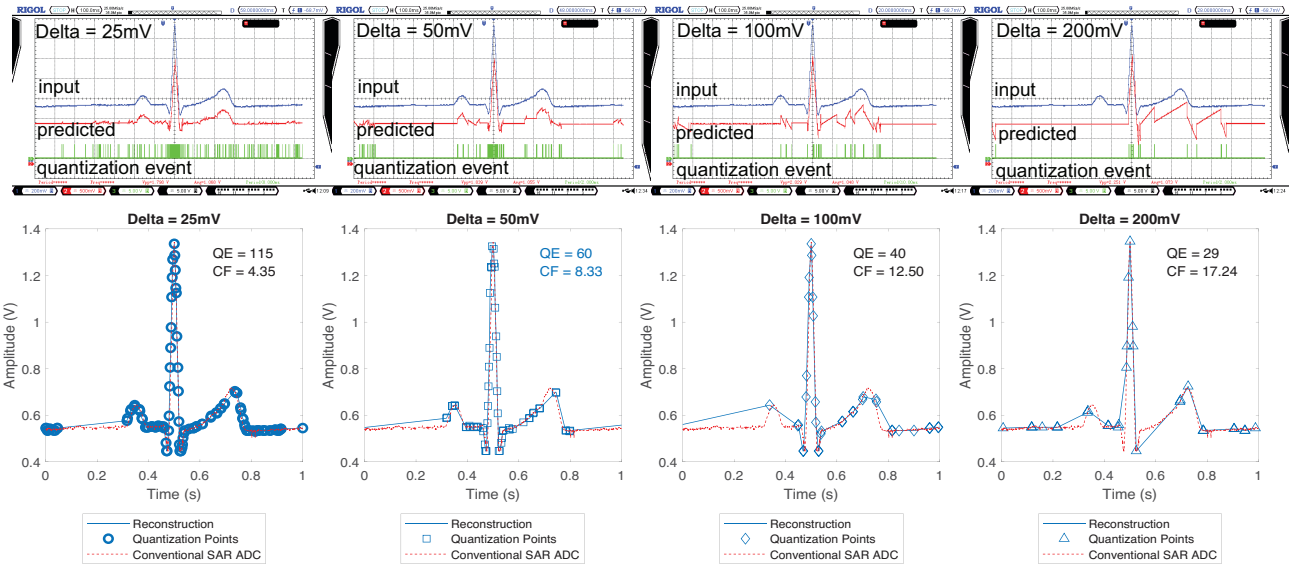

Fig. 12. (Top) Measured input and predicted waveform of the second-order level-crossing sampling ADC with different Delta values. A smaller Delta results in more quantization events. (Bottom) Reconstructed waveform comparison using the second-order level-crossing sampling system against a Nyquist sampling SAR ADC at different Delta Step values. QE represents the number of quantization events, CF represents the data Compression Factor.

tional SAR ADC is necessary for data-saving calculations and waveform morphology comparisons. To compare results, Data is obtained by using a 10-bit ADC test structure inside the fabricated chip, whose logic is implemented at the FPGA. Fig. 12 (bottom) presents the reconstructed waveforms of an ECG input using both the proposed ADC and a conventional SAR ADC at different delta steps. For a target application of real-time ECG signal acquisition, fiducial or turning point quantization is the key task. Delta values of 100 mV or 200 mV are not acceptable since they introduce distortion in the reconstructed waveform and lose important features like the onset of the P wave or the Q point. A 50 mV or 25 mV delta value is acceptable since they keep the morphology of the waveform with all fiducial points. As shown in the reconstructed waveforms, the selected sampling points are based on the slope variation of the input signal instead of a fixed clock or voltage level. As shown in the figure, a data compression factor of 8.33 is achieved at a delta step of 50 mV while still achieving an acceptable output.

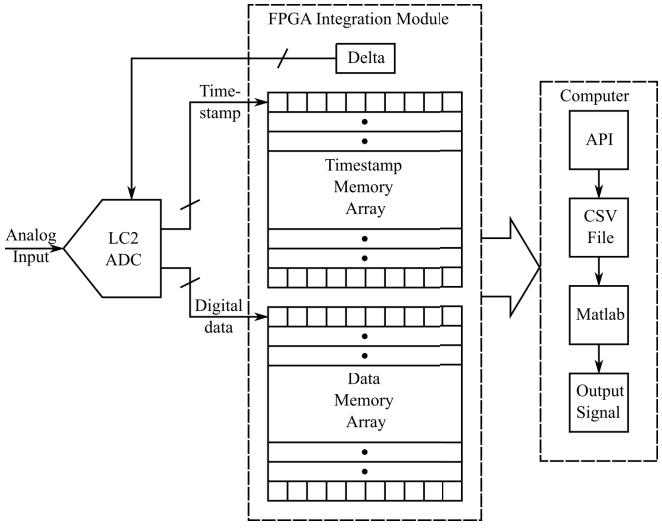

Fig. 13. Block diagram of the proposed system.

B. ECG Delineation and PVC heartbeat detection

An example of data volume reduction because of the proposed FPP filter is shown in Fig. 15. In Fig. 15 (a), a normal heartbeat within record 101 of the MIT-BIH arrhythmia database, from 117.5s to 118.5s, compared with the original sampled signal that includes 360 data points, the proposed second-order level-crossing sampling ADC has only 77 data points. With the help of FPP filter, only 27 data points are preserved for following data processing. In Fig. 15 (b), the main information of the PVC example beat from record 233 is mainly concentrated within 2.85s to 3.5s, compared with the

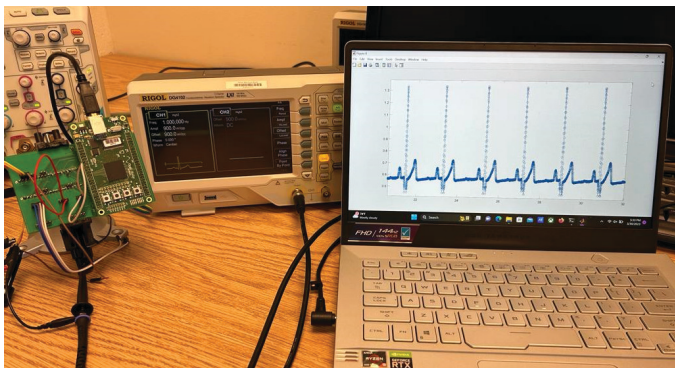

Fig. 14. Experiment Setup showing real-time data acquisition using the timestamp. The input analog signal is reconstructed and plotted on the computer.

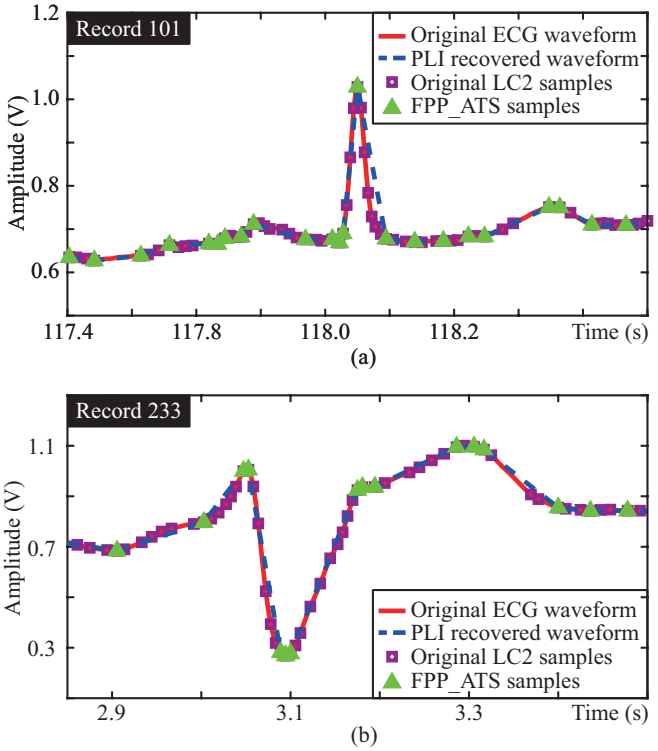

Fig. 15. Example processing result of the Fiducial Points Pruning algorithm.

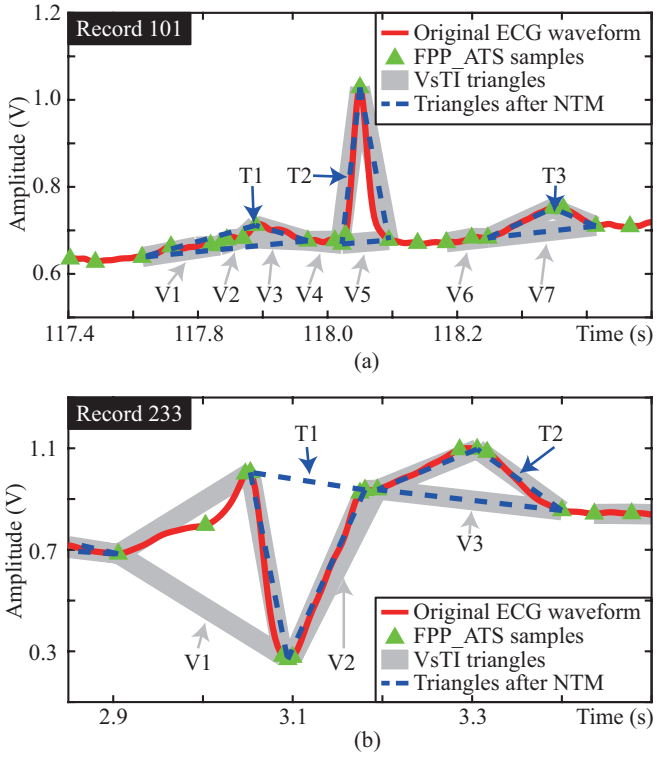

Fig. 16. Example processing result of the Vertex-side Triangulation Identifier and Neighbor Triangle Merging algorithm.

originally 234 samples, the proposed ADC generates 58 data points, and FPP reduces this number to only 16. Moreover, the remained data points after applying FPP filter are all turning points that include significant information. Even with the simplest piecewise linear interpolation, FPP-filtered data depicts the signal without obvious distortion.

An example of VsTI's core and NTM algorithm is shown in Fig. 16 with input signals the same as the FPP description in Fig. 15. As shown in Fig. 16, all important waveforms (P/QRS/T) of the ECG signal are identified. If there are baseline noises as shown in Fig. 16 (a), seven triangles are detected. With the help of NTM, triangles with at least one short side are canceled (V2, V4, and V6), and some triangles are merged (V1 and V3) to form a more condensed triangle data pattern. As shown in Fig. 16 (b), triangles are merged to form a new inverted triangle that has $Vertex\_middle$'s amplitude smaller than both $Vertex\_left$ and $Vertex\_right$. The QRS complexes detection algorithm containing just two simple rules is validated using the MIT-BIH database. As shown in Table II, the algorithm demonstrates high performance in QRS detection, small false positive (FP) and false negative (FN) numbers, achieving 98.85% sensitivity (Se) and 98.75% positive predictive value (PPV), respectively. The QT database (QTDB) is used to validate the delineation algorithm, and the results are shown in Table III. Except for localizing $T-end$, all other fiducial points detection achieve over 90% sensitivity performance with less than 20 ms timing error (which is hardly recognized with eyes by doctors, with standard ECG printing associated with 40 ms resolution). Compared with other high hardware complexity algorithms, the proposed method achieve comparable delineation result with simple and lightly weighted

TABLE I
MODEL PARAMETERS OF ALGORITHMS WITH TYPICAL VALUES.

Algorithm	Parameter	Explaination	Typical Value
2nd LC	Delta	Amplitude Threshold of Prediction Error	50mV
FPP	Th.A	Amplitude Threshold of FPP Algorithm	30mV
	Th.T	Timing Threshold of FPP Algorithm Error	40ms
	Th.S	Slope Threshold of FPP Algorithm	2.4V/s^2
VsTI	Th_V.T	Timing Threshold of VsTI Algorithm	20ms
	Th_V.A	Amplitude Threshold of VsTI Algorithm	60mv

algorithm implementation. In the algorithms, the model parameters are selected by simulation results. Typical values of model parameters for the MIT-BIH database can be found in Table I.

With the help of processed results from QRS complex detection and ECG delineation, we obtain the PVC recognition performance as shown in Table V. Compared with other methods that are achieved in complicated machine learning algorithms, the proposed lightweight method achieves middle-level PVC recognition performance. Since the total data from the proposed second-order level crossing ADC can achieve similar results can be only a few percent of the data from a conventional Nyquist sampling ADC, the computing overhead is lower than the conventional feature-based processing or neural-network-based processing. Moreover, the proposed method uses the foundational principle for PVC recognition and the results are interpretable. Thus, the method is more

TABLE II
HEARTBEATS DETECTION ALGORITHM PERFORMANCE USING MIT-BIH ARRHYTHMIA DATABASE

ID	Total	FN	FP	Se	PPV	ER
100	2273	0	0	100.00	100.00	0.00
101	1865	2	0	99.89	100.00	0.11
103	2084	0	0	100.00	100.00	0.00
105	2572	36	125	98.60	95.30	6.26
106	2027	77	90	96.20	95.59	8.24
108	1763	54	146	96.94	92.13	11.34
109	2532	9	0	99.64	100.00	0.36
111	2124	1	164	99.95	92.83	7.77
112	2539	0	0	100.00	100.00	0.00
113	1795	0	2	100.00	99.89	0.11
114	1879	42	66	97.76	96.53	5.75
115	1953	0	0	100.00	100.00	0.00
116	2412	18	13	99.25	99.46	1.29
117	1535	0	0	100.00	100.00	0.00
118	2278	2	0	99.91	100.00	0.09
119	1987	14	8	99.30	99.60	1.11
121	1863	1	0	99.95	100.00	0.05
122	2476	0	0	100.00	100.00	0.00
123	1518	0	0	100.00	100.00	0.00
124	1619	12	2	99.26	99.88	0.86
200	2601	75	17	97.12	99.33	3.54
201	1963	4	0	99.80	100.00	0.20
202	2136	10	18	99.53	99.16	1.31
203	2980	125	277	95.81	91.16	13.49
205	2656	12	3	99.55	99.89	0.56
207	2332	284	88	87.82	95.88	15.95
208	2955	72	64	97.56	97.83	4.60
209	3005	0	10	100.00	99.67	0.33
210	2650	110	9	95.85	99.65	4.49
212	2748	0	1	100.00	99.96	0.04
213	3251	18	43	99.45	98.69	1.88
214	2262	56	24	97.52	98.92	3.54
215	3363	6	10	99.82	99.70	0.48
219	2154	2	2	99.91	99.91	0.19
220	2048	0	0	100.00	100.00	0.00
221	2427	10	3	99.59	99.88	0.54
222	2483	6	3	99.76	99.88	0.36
223	2605	31	26	98.81	99.00	2.19
228	2053	39	45	98.10	97.81	4.09
230	2256	0	0	100.00	100.00	0.00
231	1571	0	0	100.00	100.00	0.00
232	1780	3	1	99.83	99.94	0.22
233	3079	32	8	98.96	99.74	1.30
234	2753	0	0	100.00	100.00	0.00
total	101205	1163	1268	98.85*	98.75*	2.40*

*Average Value

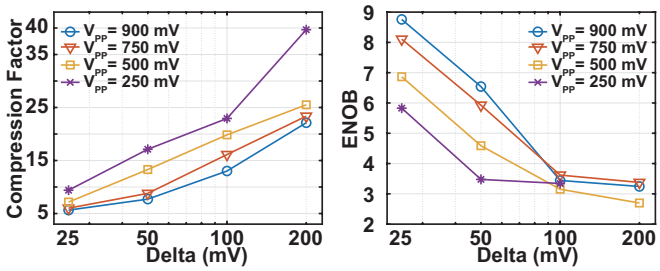

Fig. 17. Compression Factor (a) and ENOB (b) as a function of Delta in the second-order level-crossing ADC.

friendly to doctors for secondary validation and obtaining a solid diagnosis.

IV. DISCUSSION

Conventionally, the Figure-of-Merit for an ADC focuses on power consumption, sampling rate, area, and resolution. However, the power cost and area from an ADC are usually a small portion of the whole system. Also, a high sampling rate and resolution may lead to a large amount of data that overloads the following processing, storage, and communication systems. In the proposed system, only critical turning points are recorded to reduce the output data amount. Moreover, the turning points identified during analog-to-digital conversion contain important features of the input signal, which further reduces the signal processing workload. A comparison table of the reported second-order level-crossing ADC and other comparable nonuniform sampling ADCs is shown in Table IV. Since most ECG signal processing methods use either classical Nyquist sampled data or analog signal processing methods, we could not compare them directly with the proposed method. The proposed method is a digital system but only uses 12% of data compared with a system using data from Nyquist rate sampling ADC. The proposed ECG processing algorithm was synthesized using a 180nm CMOS process. Table VI summarized recent ECG processing hardware cost. Although it is difficult to compare directly since each reference are targeting different functionalities, the proposed ADC provides a high data compression factor compared to a conventional SAR ADC in sensing sparse signals, while its fully digital implementation doesn't need a complicated analog division circuitry for calculating input analog slopes like in [30].

The primary goal of the proposed ADC is to reduce the total output data amount by selecting only the critical sampling points for quantization. Compared with a conventional SAR ADC, the output of the proposed second-order level-crossing ADC contains both the digital amplitude of the selected sampling point and the timing between selected sampling points. Therefore, each sampling data point has more data than in the conventional SAR ADC. For example, a 10-bit timestamp output means the maximum measurable timing between two selected sampling points is 1024 clock cycles. If the ADC has a 10-bit resolution and the timestamp output is also 10 bits, for each sampling point, the data amount is doubled (20 bits) of a conventional SAR ADC. Asynchronous level-crossing sampling ADCs don't have quantization errors but may suffer from the inaccurate recording of timing information [48]. It does not apply to our proposed second-order level-crossing sampling system, since it uses a fixed-rate sampling clock like SAR ADCs. The data-saving performance of the proposed ADC is signal-dependent, which is in favor of signals with wider linear portions. The data-saving performance is usually measured by the compression factor [30], which is defined as the ratio of the total data amount generated by a conventional SAR ADC to the data amount from the proposed second-order level-crossing ADC. The compression Factor also depends on the Delta value and the amplitude of the signal as shown in Fig. 17 (a). With a higher Delta value, the compression factor increases while the Effective Number of Bits (ENOB) decreases, as shown in Fig. 17 (b). The ENOB drop is caused by the fewer sampling points in the proposed ADC. Since the proposed ADC skips the sampling points that are correctly predicted and uses the predicted value to replace the actual value in those points. Since there is a finite error between the predicted value and the actual value, an additional error may be introduced, and the effective number of bits drops. Therefore

TABLE III
COMPARISON FOR DIFFERENT DELINEATION ALGORITHMS ON THE QT DATABASE

		P-onset	*P-peak*	*P-end*	*QRS-onset*	*QRS-peak*	*QRS-end*	*T-peak*	*T-end*
Böck *et al.* [37]	*Se (%)*	98.5	98.5	98.5	100	-	100	100	100
	$m \pm \sigma$	10.6 ± 12	7 ± 9	1.2 ± 11.7	6.7 ± 9.2	-	5.2 ± 10.2	3.3 ± 11.9	-5.6 ± 15.6
Spicher *et al.* [38]	*Se (%)*	99.91	99.91	99.91	99.992	99.92	99.92	99.89	99.89
	$m \pm \sigma$	0.5 ± 15.1	5.1 ± 10.9	0.5 ± 15	0.9 ± 8.5	-4.1 ± 4.6	-0.4 ± 9.6	-4.5 ± 14.7	0.6 ± 20.3
Chen *et al.* [39]	*Se (%)*	-	-	-	-	100	-	99.91	-
	$m \pm \sigma$	-	-	-	-	-	-	1.4 ± 8.2	-
Hesar *et al.* [40]	*Se (%)*	-	-	-	-	-	-	-	-
	$m \pm \sigma$	16 ± 37	5 ± 34	-10 ± 34	-	-	-	-3 ± 24	-16 ± 35
Bote *et al.* [41]	*Se (%)*	98.22	99.34	99.87	100.00	-	99.97	99.89	97.49
	$m \pm \sigma$	22.3 ± 14	13.5 ± 7.3	-0.7 ± 9.5	7 ± 4.3	-	-5 ± 9.9	8.4 ± 14.3	-11.7 ± 15
This work	*Se (%)*	90.4	93.9	95.7	98.3	98.8	94.2	90.2	88.1
	$m \pm \sigma$	8.5 ± 16.3	5.4 ± 10.6	2.0 ± 17.4	5.6 ± 16.5	3.1 ± 7.7	4.7 ± 16.9	-4.3 ± 12.8	5.1 ± 18.4

TABLE IV
NONUNIFORM SAMPLING ADC PERFORMANCE COMPARISON

	Method	Technology	Sampling Rate	Power (nW)	Area (mm)	Resolution	Division	Turning Point	Sampling Value
This Work	2nd Order LC-ADC	180 nm	1 kHz	368 nW	0.39x0.44	10-bit	No	Yes	Multi-bit
TCASI 2020 [30]	Signal-Dependent	180 nm	1 kHz	1700 nW	0.5 x0.27	12-bit	Yes	Yes	Multi-bit
JSSC 2013 [24]	LC-ADC	130 nm	Async	6.5 uW	0.65x0.55	8-bit	No	No	@ Fixed Ref. Level
JSSC 2020 [42]	LC-Delta Modulator	28 nm	Async	146 uW	0.0126 mm^2	N/A	No	No	@ Fixed Ref. Level
JSSC 2022 [43]	LC-ADC	40 nm	2.4 kHz equivalent	14 uW	0.32 mm^2	9.5 equivalent	No	No	@ Fixed Ref. Level
ESSCIRC 2022 [44]	LC-ADC	40 nm	Async	5.38uW	0.012 mm^2	10.4	No	No	@ Fixed Ref. Level
TBCAS 2018 [5]	Delta Modulator	130 nm	1 kHz	360 nW	0.52x0.56	N/A	No	No	Slope Only
CICC 2020 [32]	2nd-Order Delta Modulator	180 nm	1 kHz	151 nW	0.62x0.4	N/A	No	Yes	Slope Only

TABLE V
PERFORMANCE ASSESSMENT COMPARISON OF PVC

	Methods	PVC detection Performance				
		F1	ACC (%)	Sen (%)	SP (%)	PPV (%)
Hou *et al.* [45]	LSTM	-	99.7	97.4	99.9	-
Xu *et al.* [46]	DNN	-	99.7	97.7	99.9	-
Raj *et al.* [3]	SVM + Particle swarm optimization	-	98.6	98.6	-	99.9
Wang *et al.* [47]	CNN	0.57	92.5	48.6	97.5	69.0
This work		0.81	97.3	89.6	97.8	73.3

TABLE VI
COMPARING ECG PROCESSING SYSTEMS.

	This work	TBCAS'23 [21]	TCASII'22 [22]	TBCAS'22 [23]
Technology	180nm Synthesis	65nm Tapeout	180nm Synthesis	180nm Tapeout
Processing Function	Fiducial Points	QRS Detection	Arrhythmia Detection	P-QRS-T Detection
Algorithm	Triangle Searching	Analog Filtering	Digital Neual Network	Feature Mapping
Power	160nW	2.2nW	8.75uW	2.657uW
Area (mm2)	0.06	0.08	1.32	0.55

the Delta value provides an additional parameter to the user for the trade-off between accuracy and data throughput. In our experiment, the compression factor achieves 8.33 for the ECG signal with negligible distortion of the input signal.

Since the proposed system selects fewer sampling points from the input waveform, it may introduce more errors compared to the conventional ADC. Although for the selected sampling points, the digital values of the proposed ADC are the same as in a conventional ADC, the proposed method does not record the actual amplitude of the sampling points where the predictions are successful. The additional error introduced by removing the sampling points depends on the input signal, the Delta value, and the reconstruction methods, which affects the ENOB of the ADC as shown in Fig. 17 (b). This affects the performance of the classification but could be mitigated using advanced signal reconstruction methods. The primary reconstruction methods for nonuniform sampling include but are not limited to linear interpolation, polynomial interpolation, cubic spline interpolation, and Lagrange-Chebyshev interpolation [49]. Using a complicated reconstruction method can reduce errors introduced by nonuniform sampling with a cost of high computing overhead. The proposed ADC samples at a fixed rate and every sampling results in a multi-bit quantization process that records the real amplitude value instead of a single polarity bit in the asynchronous level-crossing ADC. In the worst scenario, if one level-crossing event is missed and not recorded, the next level-crossing event still records the multi-bit real amplitude value. So the error does not pass to the following recordings during reconstruction. Therefore, each conversion error does not result in a significant bit-error-rate increase in the proposed ADC, so the back-end error correction logic for an asynchronous level-crossing ADC is not required.

In real on-sensor system implementation, the input signal

could contain low-frequency high-amplitude baseline wondering and high-frequency low-amplitude noise. This work only focuses on the data conversion and digital processing algorithm, so we assume that the analog-front-end (AFE) circuit contains noise filters and variable gain amplifiers, which is typically true in most AFE solutions. For on-sensor processing, as long as the noise amplitude is less than the Delta value, the system is not affected by the noise. Considering that the Delta value (50-100mV) is usually much higher than the noise amplitude (<10mV), we believe this assumption is valid. The proposed second-order level-crossing ADC achieves comparable ECG delineation and PVC classification performance with other systems that use Nyquist sampling data, which means the data size can be reduced by around ten times without reducing the system performance. The system has potential in future low-power wearable ECG monitoring systems.

V. Conclusion

This paper presented a novel second-order level-crossing sampling ADC that performs key sampling point selection by predicting the sampling value using prior quantization or prediction results. The prediction and sampling selection are performed digitally without complicated analog division circuitry. The circuit is implemented by modifying the control logic of a conventional SAR ADC. The proposed ADC automatically selects the turning point of the input analog signal and records the amplitude and timing information of the selected points. The signal-dependent data compression factor is 8.33 for sensing the ECG signal. ECG processing algorithms based on the output of the proposed ADC are validated for ECG delineation and ectopic heartbeat detection. The proposed ADC and ECG processing algorithm has the potential to greatly reduce computing overhead for the digital processing, storage, and communication circuits in low-power data acquisition systems.

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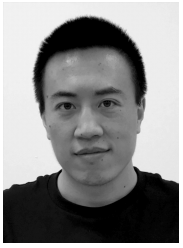

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