Linear Input Range Extension for Low-Voltage Operational Transconductance Amplifiers in Gm-C Filters

Mahmoud A. A. Ibrahim, Marvin Onabajo
Dept. of Electrical and Computer Engineering
Northeastern University, Boston, USA
ibrahim.ma@husky.neu.edu, monabajo@ece.neu.edu

***Abstract* — A second-order G_m-C low-pass filter with a novel large-signal linearization method for operational transconductance amplifiers having low supply voltages is presented. The design technique uses a combination of unbalanced resistively degenerated differential pairs and adaptive biasing to extend the linear range. The presented unity-gain biquad filter cell is intended to be used as a building block in the baseband section of a low-power receiver, and it has been designed in a standard 0.13-µm CMOS technology with a cutoff frequency of 500 KHz. The power consumption of the filter is 39 µW with a supply voltage of 0.6 V. Simulation results show a total harmonic distortion of -40 dB for a 5 KHz input tone with 614 mV peak-to-peak differential swing in the passband of the filter.**

***Keywords* — Operational transconductance amplifier (OTA), large-signal linearization, adaptive biasing, unbalanced differential pair, G_m-C filter, low-voltage amplifiers.**

I. Introduction

The need for self-powered systems continues to increase with the rising demands for biomedical devices, wearable electronic products, and Internet of Things (IoT) integration. Power management circuits have higher efficiency when providing low supply voltages, but the linearity of analog circuits such as operational transconductance amplifiers (OTAs) worsens when they operate with low voltage supplies. These factors drive research towards the development of low-voltage linearization techniques.

OTA linearization approaches can be categorized into two main groups: i) large-signal linearization methods that extend the input voltage range over which the transconductance is relatively constant [1]-[3], and ii) small-signal linearization techniques that minimize the distortion components created with small input signal levels [4]-[6]. With low supply voltages, large-signal linearization becomes very critical due to the lack of voltage headroom for operation within the linear ranges of the transistors. Some of the previous works to increase the linear input range of OTAs include a feed-forward approach in a 65nm CMOS process, but with a 1.2V supply [1]. A bulk degeneration technique is employed in [2], which requires a triple N-well fabrication process and creates device matching constraints due to the use of different wells for the input pair transistors. A technique with three unbalanced differential pairs is described in [3]. The method requires increasing the number (>2) of differential pairs to extend the linear range, which increases power consumption and creates multiple peaks in the transconductance vs. input voltage amplitude characteristics.

This paper is structured as follows: Section II describes the proposed linearization technique with two unbalanced differential pairs and adaptive biasing. Section III contains circuit design details and simulation results for an OTA using the linearization method. Section IV illustrates the implementation and simulation results of a transconductance-capacitor (G_m-C) biquad filter with the OTA design from Section III. Section V contains concluding remarks on the method and results.

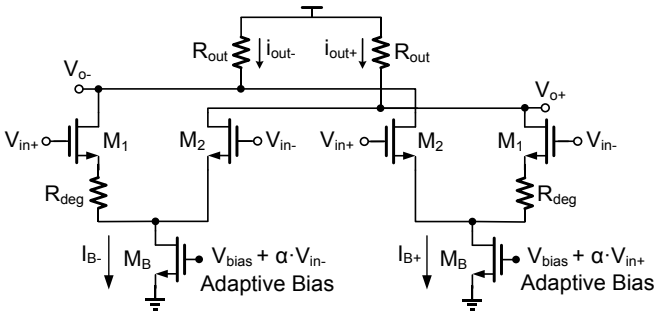

Fig. 1. Unbalanced differential pairs with adaptive biasing.

II. Proposed Technique

The presented large-signal linearization technique entails unbalanced resistive degeneration with adaptive biasing as displayed in Fig. 1. This example amplifier consists of two differential pairs that are both unbalanced by a source degeneration resistor (R_{deg}) for one of the transistors in a pair. This configuration causes the transconductance to have two peaks across the input voltage range while maintaining quasi-flat transconductance characteristics near the center. In addition, the adaptive biasing manipulates the balance of the two pairs according to the differential input voltage by varying the tail current provided by transistor M_B. In contrast to the technique in [3], this approach reduces the number of differential pairs required to extend the linear range, thereby

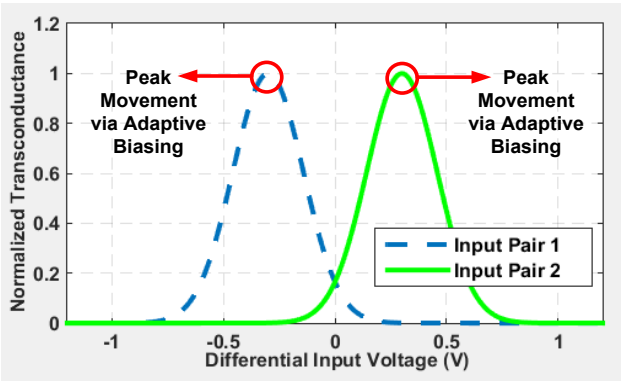

Fig. 2. Illustration of transconductance vs. input voltage characteritics.

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lowering the power consumption. As a result of the adaptive biasing, the proposed unbalanced resistive degeneration also limits the number of peaks in the transconductance versus input voltage curve. The adaptive biasing annotated in Fig. 1 involves feed-forward of the positive and negative inputs to the gate voltages of the tail current sources that provide bias currents ($I_{B+/-}$). Thus, the transconductance peaks of the two transistor pairs move with the input voltage as visualized in Fig. 2 to achieve near-flat transconductance across a wide differential input range with low power consumption.

III. OTA Circuit Design and Results

A. OTA implementation

Fig. 3 shows the schematic of a folded-cascode OTA with the proposed linearization method. This OTA was designed with a 0.6 V supply in 0.13-µm CMOS technology. The threshold voltage of M_1 is 462 mV and that of M_2 is 443 mV. This difference is due to the source-to-bulk voltage change (i.e., increased body effect) with degeneration resistor. The degeneration resistors (R_{deg} = 1 MΩ) were implemented with high-resistance polysilicon resistors from the design kit library, which would require a layout area of 50 µm × 25 µm.

B. Adaptive bias voltage generation

Fig. 4 depicts the schematic of the adaptive bias voltage generator. The nominal biasing current (I_{basic}) is provided by transistor M_{P2}. Another inverter-based current generator consisting of M_{N1} and M_{P1} subtracts or adds current ($I_{-/+}$) according to the input voltage ($V_{in+/-}$). These two currents are summed at the two diode-connected transistors (M_B), of which one mirrors the resulting current to the corresponding tail current transistor (M_B in Fig. 3). The inclusion of the upper diode-connected M_B transistor in Fig. 4 allows the M_{N1} transistor to remain in saturation. The circuit was designed to have a value of $\alpha = 0.2$, where α designates the fraction of the input voltage by which the bias voltage is modulated as annotated in the figures.

C. Common-mode feedback circuit design

Fig. 5 shows the common-mode feedback (CMFB) circuit for the linearized low-voltage OTA. This topology was customized

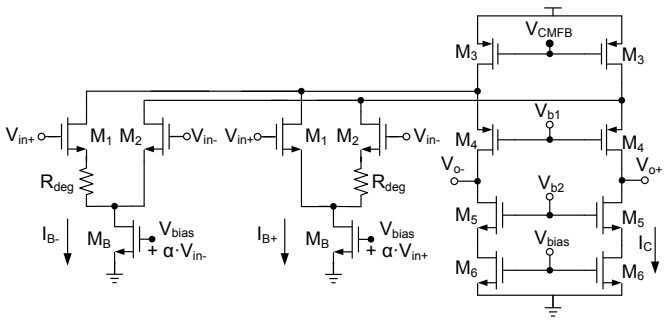


Fig. 3. Proposed linearized operational transconductance amplifier (OTA).

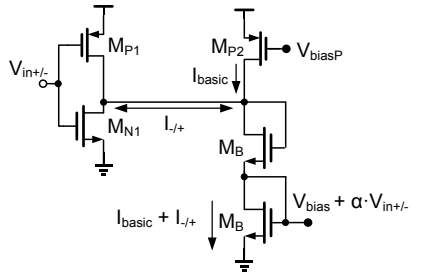


Fig. 4. Adaptive bias voltage generation circuit.

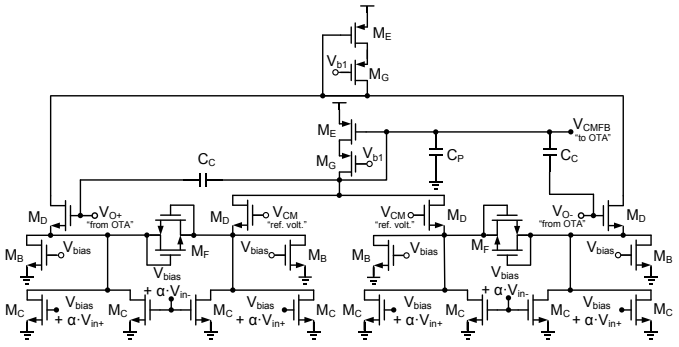


Fig. 5. Adaptive common-mode feedback (CMFB) circuit.

for high linearity with wide input range. Diode-connected transistors (M_F) are used as degeneration resistors to linearize the CMFB circuit, which extends its input range to suit the large voltage swing of the signal ($V_{o+/-}$) from the OTA. The transistors M_G were inserted to terminate the transistors M_E with the same source-to-drain voltage (V_{SD}) condition as their counterparts in the OTA output stage (M_3 in Fig. 3). The capacitors C_C and C_P in Fig. 5 provide frequency response compensation for stability of the CMFB loop, such that the phase margin of the loop is 63°. Since the current in the branches of the linearized OTA varies due to the adaptive biasing, it is necessary to emulate this variation in the CMFB circuit. For this reason, the transistors M_C in Fig. 5 are also connected to the adaptive bias voltage generator in Fig. 4.

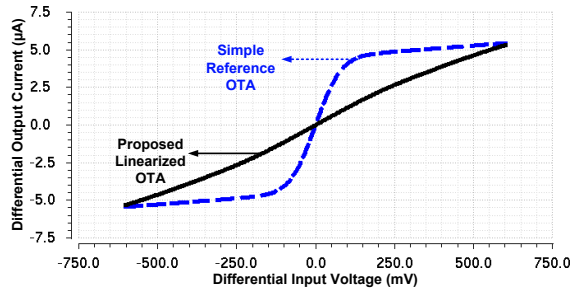
D. OTA simulation results

For comparison purposes, a simple reference OTA and an OTA with conventional resistive source degeneration were designed in the same CMOS 0.13-µm technology, and simulated with device models provided by the foundry. The simple reference OTA is similar to that in Fig. 3, but with only one input pair (instead of two) and without resistor R_{deg}. The resistive source degeneration OTA is also similar to that in Fig. 3, but with only one input pair and with R_{deg} connected at the sources of both input transistors (instead of only one). The power consumption of all OTA designs with CMFB circuits was constrained to the 9-10 µA range to make a fair comparison. The simulated DC gain, unity-gain frequency, and power of the simple reference OTA are 49 dB, 1.8 MHz, and 9.4 µW respectively; and the same parameters of the resistive source degeneration OTA are 41.6 dB, 1.0 MHz, and 9.18 µW. It can be noticed from TABLE I that the unity-gain frequency of the proposed linearized OTA is higher than that of the resistive source degeneration OTA due to the effect of the input feedforward path in Fig. 3 through the

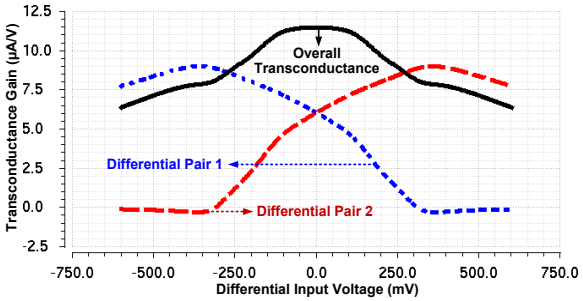
TABLE I. OTA performance comparison (0.13-µm CMOS)

Parameter	Simple Reference OTA	Resistive Source Degeneration OTA	Proposed Linearized OTA
Power	9.40 µW	9.18 µW	9.81 µW
Supply Voltage	0.6 V	0.6 V	0.6 V
Transconductance	55.7 µA/V	23.4 µA/V	11.5 µA/V
DC Gain	49.0 dB	41.6 dB	37.3 dB
Unity-Gain Frequency	1.8 MHz	1.0 MHz	1.5 MHz
Integrated Input-Referred Noise*	39.6 µV	94.6 µV	184 µV
HD3 at 614 $mV_{in(p-p)}$	-24.4 dB	-28.8 dB	-47.6 dB

* Integrated over 500 KHz, which is the bandwidth of the filter in Section IV.



(a)



(b)

Fig. 6. Plots of (a) OTA output currents, and (b) transconductance for each differential pair and their combined output in the linearized OTA.

adaptive bias circuitry in Fig. 4. The plots in Fig. 6 show the differential output current (i_{out+} - i_{out-}) and the steady overall transconductance of the linearized OTA versus its differential input voltage. From Fig. 6(a), it can be seen that the linear input voltage range is extended by a factor of four compared to the simple reference OTA. Hence, the linearized low-voltage OTA is suitable for baseband G_m-C filters and for variable gain amplifiers with large signal swings. Fig. 7 displays the simulated open-loop voltage gain and phase versus frequency of the proposed linearized OTA, which has a DC gain of 37.3 dB and a phase margin of 57.3°.

TABLE I contains a comparison between the simple reference OTA, resistive source degeneration OTA, and the proposed linearized OTA. In each case, a copy of the OTA was cross-coupled (diode-connected) to form a load that results in a voltage gain of unity for the linearity assessment. This configuration was chosen to emulate the operating conditions in the filter with 0 dB passband gain and large output voltage swing. TABLE I reveals the expected linearity improvement from the widely used resistive source degeneration method with the known tradeoffs (reduced transconductance, increased input-referred noise, decreased unity-gain frequency). More importantly, the simulation results show that the proposed linearized OTA topology improves the third-order harmonic distortion (HD3) by around 19 dB compared to resistive source degeneration, with the tradeoffs of approximately doubled noise and halved transconductance.

TABLE II lists the HD3 values with 614 mV peak-to-peak differential input for device corner model cases with optimum

TABLE II. HD3 corner simulation results with 614 $mV_{(p-p)}$ input at 5 KHz

OTA	Simple Reference OTA	Resistive Source Degeneration OTA	Proposed Linearized OTA
Typical	-24.43 dB	-27.16 dB	-47.55 dB
Fast	-19.09 dB	-24.44 dB	-47.39 dB
Slow	-22.95 dB	-27.36 dB	-46.57 dB

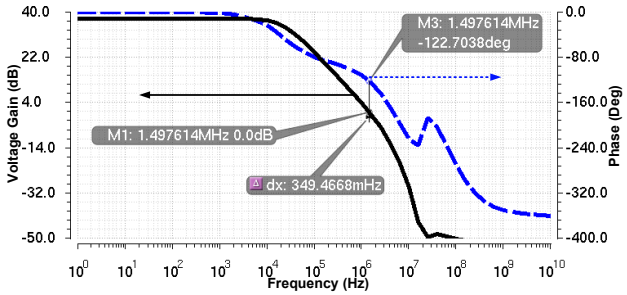


Fig. 7. Open-loop voltage gain and phase responses of the linearized OTA.

bias voltage (V_{bias}) for each case. It can be observed that the proposed linearization method is robust to process variations.

IV. Filter Implementation and Simulation Results

The simple reference OTA and the proposed linearized OTAs were tested in a second-order unity-gain low-pass filter with a cutoff frequency of 500 KHz using the architecture in Fig. 8. This filter has a transfer function of

$$H(s) = \frac{\left(\frac{G_{m2} \cdot G_{m4}}{C_A \cdot C_B}\right)}{s^2 + s\left(\frac{G_{m3}}{C_B}\right) + \left(\frac{G_{m1} \cdot G_{m2}}{C_A \cdot C_B}\right)} \quad . \tag{1}$$

The four OTAs in the filter implementation were all identical to obtain unity gain at low frequencies. The simple reference OTA has a transconductance (G_m) equal to 55.7 μA/V. The corresponding filter was implemented using capacitors (C_A and C_B) with values less than 20 pF. The linearized OTA has a transconductance of 11.5 μA/V, and the values of C_A and C_B are both less than 5 pF to design for the same cutoff frequency.

The simulated frequency response of the filter with the linearized OTAs is displayed in Fig. 9, and Fig. 10 shows its input third-order intermodulation intercept point (IIP3) curves from two-tone tests (f_1 = 5 KHz, f_2 = 5.1 KHz) with different input power levels. For input signals with power levels below -33 dBm, the extrapolated IIP3 is -10.8 dBm. It can be seen from the figure that the IIP3 is better for input power levels between -33 dBm and 0 dBm as a result of the large-signal linearization method. Fig. 11 shows the output voltage spectrum of the linearized filter with a 614 mV_{p-p} sinusoidal input signal at 5 KHz. It has a total harmonic distortion (THD) of -40 dB. In comparison, the filter with simple reference OTAs has a THD of -20.5 dB for the same input signal level.

TABLE III contains a specification summary of state-of-the-art receiver baseband filters and the presented linearized filter. The figure of merit (FoM) values in the table were calculated with equation (2) below (from [7]). The proposed linearization technique resulted in significant improvement of the FoM compared to the previous works.

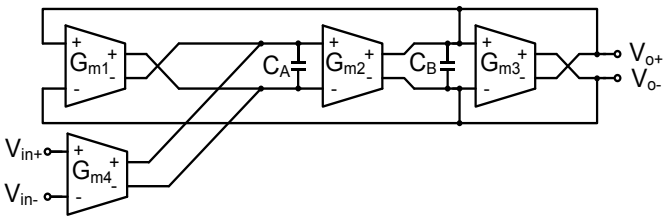


Fig. 8. G_m-C biquad filter.

TABLE III. Filter performance comparison

Parameter	This Work*	[8]**	[9]*	[10]*	[11]**	[12]**
Filter Type	**Biquad**	Butterworth	Butterworth	Complex	Chebyshev	Bessel
Order (n)	**2**	4	3	2	3	4
Technology	**0.13 µm**	0.5 µm	0.35 µm	0.13 µm	0.13 µm	0.13 µm
Cutoff Frequency (f_c)	**0.5 MHz**	0.65 MHz	0.25 MHz	1 MHz	0.5 MHz	2.11 MHz
Supply Voltage (V_{DD})	**0.6 V**	3.3 V	1.8 V	0.8 V	1.2 V	1.2 V
IIP3	**-10 dBm (in-band, 5 & 5.1 KHz inputs)**	22 dBV_P (in-band)	13 dBm (in-band)	-12 dBm (out-of-band)	15.25 dBm (in-band)	21 dBm (in-band)
Integrated Input-Referred Noise	**327 μV_{rms} (1 Hz - 0.5 MHz)**	316 μV_{rms}	89.83 μV_{rms}	5.7 μV_{rms}	342 μV_{rms}	36 μV_{rms}
THD	**-40 dB @ V_{in} = 614 $mV_{in(p-p)}$**	-70 dB	N/A	N/A	-47.6 dB	-40 dB
Dynamic Range, DR (at given THD)	**56.4 dB**	67 dB	57 dB	N/A	53 dB	81 dB
Power Dissipation	**0.039 mW**	0.76 mW	0.24 mW	0.042 mW	0.45 mW	3.4 mW
FoM	**4.14 × 10^{-13} J·V**	144 × 10^{-13} J·V	101 × 10^{-13} J·V	N/A	67.9 × 10^{-13} J·V	59.7 × 10^{-13} J·V

* Simulation results, ** measurement results.

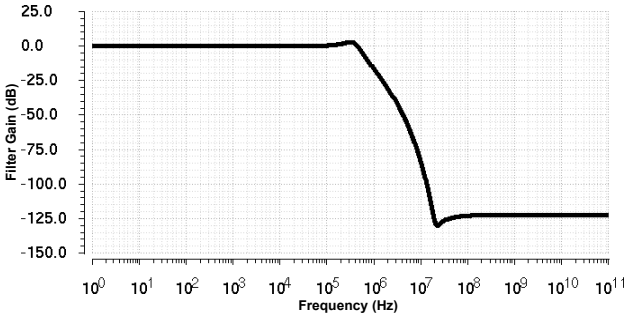


Fig. 9. Voltage gain of the filter vs. frequency.

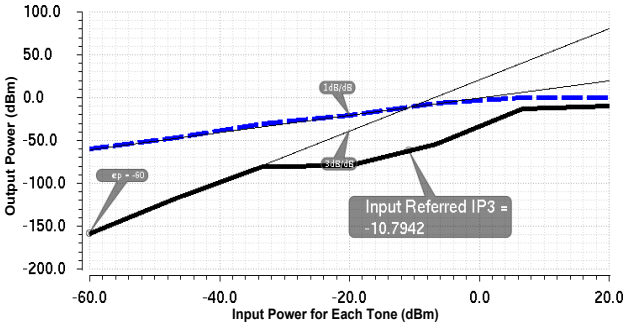


Fig. 10. IIP3 curve with tones at 5 KHz and 5.1 KHz.

$$FoM = \frac{Power \cdot V_{DD}}{n \cdot f_c \cdot DR} \tag{2}$$

V. Conclusion

A large-signal linearization technique for operational transconductance amplifiers was introduced and demonstrated in a prototype G_m-C biquad low-pass filter. The technique leverages the advantages from combining unbalanced resistively degenerated differential pairs and adaptive biasing to extend the linear range of operational transconductance amplifiers. The filter was designed with 0.13-µm CMOS technology and a 0.6 V supply voltage, featuring -40 dB THD with a 614 mV peak-to-peak input signal at 5 KHz. Compared to the state-of-art, the simulation results indicate competitive performance, particularly considering the high linearity with low supply voltage and low power consumption of the presented design.

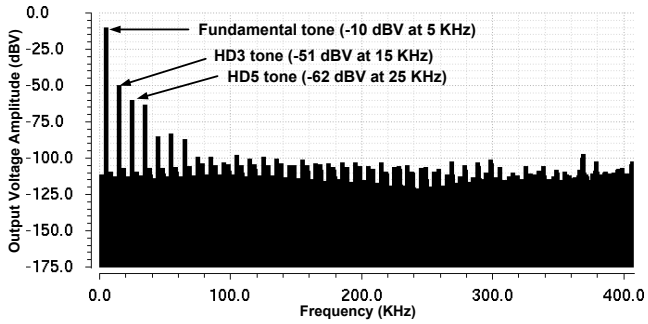


Fig. 11. Filter output spectrum with a 5 KHz 614 $mV_{(p-p)}$ sinusoidal input.

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