A Low-Power Complex Bandpass G_m-C Filter with Dynamic Range Expansion through Adaptive Biasing

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***Abstract* — This paper presents a first-order complex bandpass filter designed with a large-signal linearization technique. A novel adaptive biasing circuit is proposed to extend the linear range of the filter, which was designed in 130nm CMOS technology with a power consumption of 26.1 µW from a 0.6 V supply. The simulated center frequency and bandwidth of the filter are 2 MHz and 600 KHz respectively. It has an image rejection ratio of 22 dB per pole and an out-of-band spurious-free dynamic range of 56.0 dB.**

***Keywords* — Bluetooth low energy (BLE), complex filter, adaptive biasing, source degeneration, large-signal linearization, low power, low voltage.**

I. Introduction

Bluetooth Low Energy (BLE) is an attractive standard for low-power devices such as wearable consumer products and biomedical devices for the Internet of Things (IoT). These devices have limited energy sources due to their sizes and placement. Thus, bias currents and supply voltage of such devices are continuing to be scaled down to prolong battery life. That scaling leads to a degradation of the linear range of analog circuits, which is an issue that has motivated research on linearity enhancement. Previous efforts have focused on the development of methods for linearity enhancement of low-noise amplifiers (LNAs) and RF front-end circuits for low-power receivers using inductive source degeneration and cross-coupling capacitors [1], [2]. In low-power receivers with reduced supply voltages, one of the blocks that severely suffers from linear range limitations is the baseband filter. In this work, a linearization technique has been applied to a complex baseband filter that rejects the image frequency band to avoid interference. For low-power operation, a current-reuse architecture proves to be beneficial because the same bias current is shared among the transconductance cells of the filter [3].

Previous methods have focused on increasing the dynamic range of the filters for applications that permit power consumptions in the milliwatt range [4]-[8]. On the other hand, the current-reuse complex filter architecture proposed in [3] has a power consumption below 50 µW and low input-referred noise. In this paper, a modified version of the adaptive biasing technique from [9] is applied to the filter architecture from [3] to increase the linear range.

The paper is structured as follows: Section II introduces the proposed filter architecture. Section III describes the circuit design of the filter and the new adaptive biasing circuit. Section IV discusses simulation results of the complex filter, and compares these results with prior works. Section V contains a summary and conclusions.

This work was supported in part by the National Science Foundation under award #1451213.

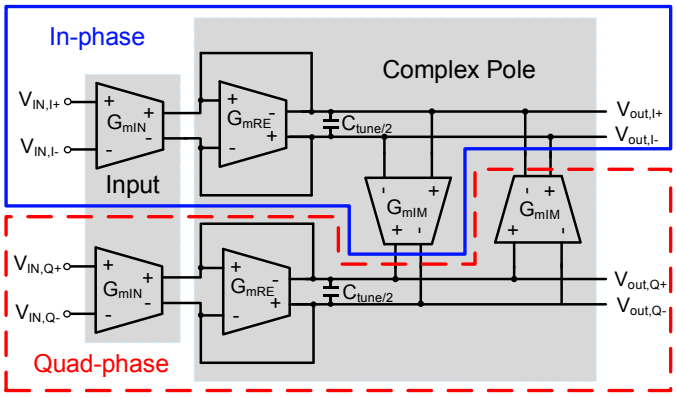


Fig. 1: G_m-C complex filter architecture.

II. Proposed Filter Architecture.

This section describes how a large-signal linearization technique has been realized within the filter from [3] to improve the dynamic range. The operational transconductance amplifier (OTA) from [9] was designed with a modified adaptive biasing circuit that consumes less power and has a wider bandwidth compared to the previous version.

Fig. 1 shows the complex transconductance-capacitor (G_m-C) filter that is described with more detail in [3]. $V_{IN,I+}$,$V_{IN,I-}$ are the in-phase inputs and $V_{IN,Q+}$,$V_{IN,Q-}$ are the quad-phase inputs. The bandpass response is obtained from shifting the real poles (G_{mRE}/C_{tune}) of the lowpass response, where the shift frequency is determined by G_{mIM}/C_{tune} that can be adjusted according to the desired center frequency. In the architecture proposed in [3], the

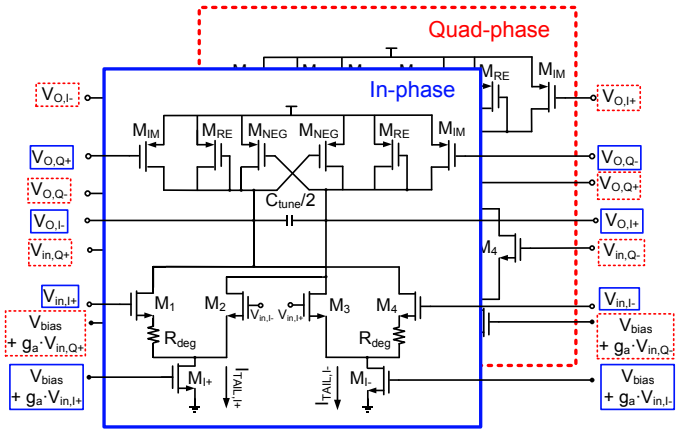


Fig. 2: Current-reuse complex filter with adaptive biasing.

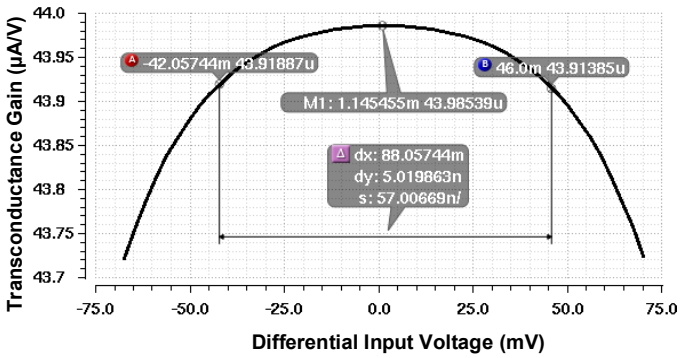


Fig. 3: Overall transconductance of the filter vs. differential input voltage.

input bias current is reused by G_{mRE} and G_{mIM} to save power. As depicted in Fig. 2, this topology can be enhanced by adding adaptive biasing to tolerate larger signal swings. The adaptive biasing [9] regulates the tail currents (I_{TAIL}) of the input differential pairs M_1-M_4 for both in-phase and quad-phase paths according to the applied input signal. Fig. 3 displays the simulated overall transconductance of the filter with adaptive biasing for various input voltage values. Note that, if the gain was 10, a differential input voltage range from -60 mV to 60 mV would correspond to a differential output range from -0.6V to 0.6 V (i.e., rail-to-rail operation with a 0.6 V supply). This wide input range is enabled by the use of two differential pairs (M_1-M_4) that are both unbalanced as described in the next section.

III. Circuit Design Considerations

A. Filter implementation

The input stage of the filter in Fig. 2 consists of two differential pairs for each of the in-phase and quad-phase (M_1-M_4) paths. The source degeneration resistors (R_{deg}) of M_1 and M_4 cause the differential pairs to be unbalanced, and this results in shifted transconductance peaks for each of the input pairs. Adaptive biasing controls the strength of the pairs according to input signal level, which makes the combined transconductance of the two pairs relatively flat across the input range of interest [9]. Transistors $M_{I+/-}$ and $M_{Q+/-}$ provide the bias tail current (I_{TAIL}) for the input differential pairs and the same bias current is reused by transistors M_{IM} and M_{RE}.

The second stage that shifts the real pole to an imaginary pole is implemented using transistors M_{RE}, M_{IM}, and M_{NEG} in Fig. 2. The diode-connected transistor M_{RE} is in parallel with the negative transconductance of M_{NEG} to produce a resultant transconductance of

$$gm_{RE(final)} = gm_{RE} - gm_{NEG} \tag{1}$$

for the differential signal [3]. The bandwidth of the filter is determined by $gm_{RE(final)}/C_{tune}$. Note that the negative transconductance of M_{NEG} increases the quality factor of the filter as evident from the following equation [3]:

$$Q = \frac{gm_{IM}}{gm_{RE} - gm_{NEG}} . \tag{2}$$

For the common-mode signal, the input differential pair sees the diode-connected transistors M_{RE} as its load. Since the effective resistance of M_{RE} is relatively small, this filter architecture does not require a common-mode feedback loop.

The value of the resistor R_{deg} is 770 KΩ in this case. It is implemented with high-resistance polysilicon from the process design kit, which would have a layout area of 39 µm × 24 µm.

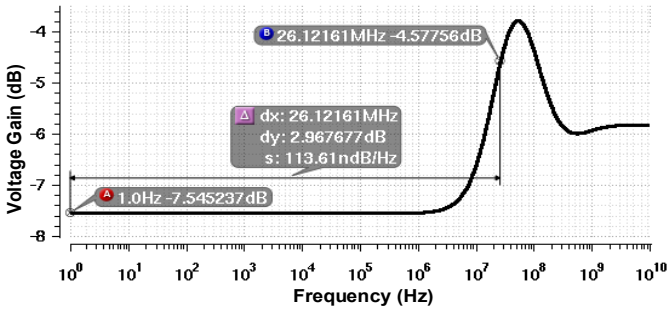


Fig. 4: Frequency response of the adaptive biasing path in [9].

B. Stability

The stability of the filter is defined by the following equation:

$$L(Q,\alpha) = \frac{Q^2(\alpha-1)^2 - 2Q^2\alpha}{1+\alpha(2+2Q^2+\alpha)} , \tag{3}$$

which is a function of quality factor (Q) and α, where α is the ratio gm_{NEG}/gm_{RE}. To maintain stability [3], the value of L(Q,α) must be less than 1. In this design, the values of gm_{IM}, gm_{RE}, and gm_{NEG} are 80.96 µA/V, 51.87 µA/V and 40.24 µA/V respectively. These values result in a Q of 6.96 from equation (2). The transistors M_{RE} and M_{NEG} are sized such that the value of α is 0.77. Inserting the obtained values of Q and α in equation (3) results in L (Q, α) = 0.637, which confirms that stability is assured.

C. Proposed adaptive bias voltage generation

Fig. 4 shows the simulated frequency response of the adaptive biasing path (from the input to the bias voltage) in [9], where the bandwidth determined from DC to the 3-dB frequency corresponds to 26.1 MHz. This adaptive biasing circuit has a limited bandwidth, but it is suitable for lowpass filter applications up to several megahertz. To enable operation at higher frequencies, a modified adaptive bias voltage generation circuit is proposed in Fig. 5. Transistors M_P and M_N form an inverter that either adds or subtracts current ($I_{in,I+/-}$ and $I_{in,Q+/-}$) according to the input voltage level ($V_{in,I+/-}$ and $V_{in,Q+/-}$) for the in-phase and quad-phase paths respectively. Together with the effective transconductance of the inverter stage, the resistor R_{ga} allows to

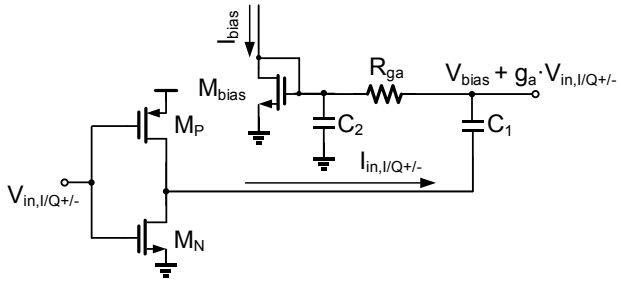


Fig. 5: Proposed adaptive bias voltage generation circuit.

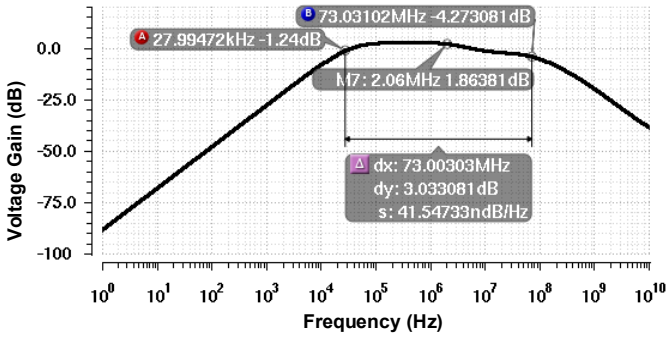
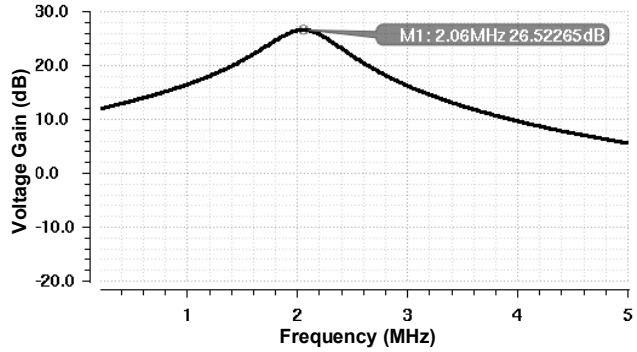


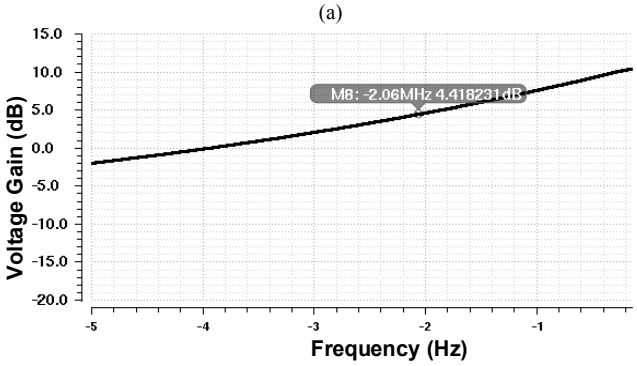
Fig. 6: Frequency response of proposed adaptive bias voltage generation circuit.

control the value of gain g_a in Fig. 5 and Fig. 2, which is the ratio of input voltage by which the bias voltage is modulated. Here, the circuit was designed such that $g_a = 0.1$.

The modulated bias voltage, shown in Fig. 5, is fed to the input of the biasing transistors of the filter (M_{I+}, M_{I-}, M_{Q+} and M_{Q-}) in Fig. 2. The capacitors (C_1, C_2) and resistor R_{ga} determine the cutoff frequencies of the circuit. For the maximum linear range and bandwidth of the adaptive bias circuit, the values of C_1 and C_2 were selected as 20 pF and 10 pF respectively, and the corresponding value of R_{ga} is 7.5 KΩ. Fig. 6 displays the simulated frequency response (from $V_{in,I/Q+/-}$ to $V_{bias} + g_a \times V_{in,I/Q+/-}$) of the modified adaptive biasing circuit. The bandwidth is 73 MHz, which allows the circuit to react to input signals with higher frequencies. It is also noteworthy that the adaptive biasing in [9] was simulated with the proposed filter, which resulted in higher power consumption of 13 µW compared to the new adaptive biasing circuit whose power consumption is 6.1 µW.



(a)



(b)

Fig. 7: Filter response for frequencies with (a) positive offsets from the carrier frequency, (b) negative offsets from the carrier frequency.

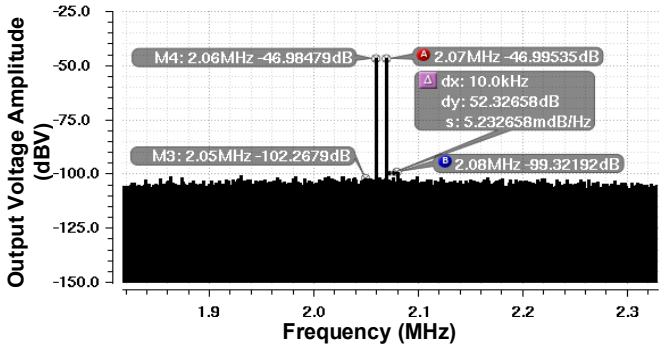


Fig. 8: Output spectrum to assess the in-band SFDR when two tones (input power level of -60.5 dBm each) are placed in the passband of the filter .

IV. Simulation Results

The first-order complex filter was simulated in Cadence with device models for GF 130nm CMOS technology and a reduced supply voltage of 0.6 V. Fig. 7(a) reveals that the passband gain is 26.5 dB, and it can be observed from Fig. 7(b) that the gain in the image band is 4.4 dB. This implies an image rejection ratio (IRR) of 22.1 dB with a single pole. The filter consumes a total power of 26.1 µW with adaptive biasing circuitry.

To assess the in-band spurious-free dynamic range (SFDR), two tones were placed at 2.06 MHz and 2.07 MHz during a simulation with activated transient noise, such that the third-order intermodulation (IM3) products are at 2.05 MHz and 2.08 MHz. Fig. 8 shows the resulting output spectrum, indicating an SFDR of 52.3 dB. The simulated third-order intermodulation intercept point (IIP3) of -36.1 dBm in Fig. 9 was obtained with the same two-tone test frequencies. To evaluate the out-of-band SFDR, two tones were placed at 5.06 MHz and 8.06 MHz such that an in-band intermodulation product is created at 2.06 MHz. Fig. 10

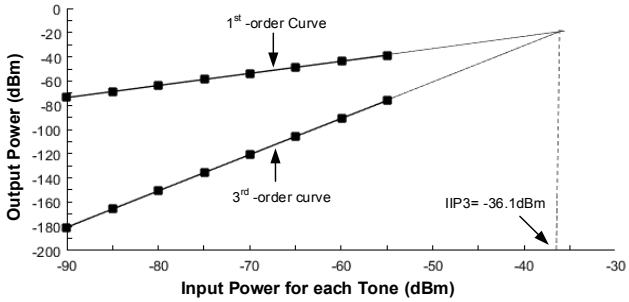


Fig. 9: In-band IIP3 plot with two tones at 2.06 MHz and 2.07 MHz.

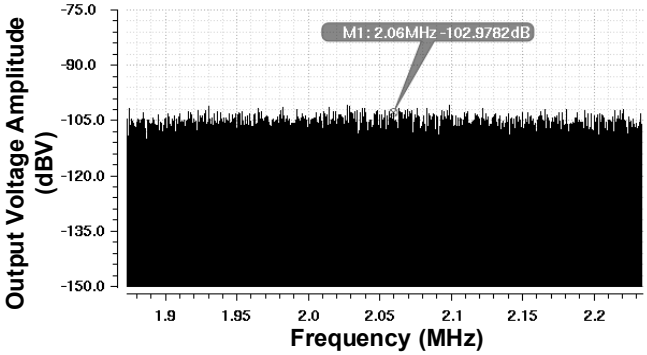


Fig. 10: Output noise floor with a label at the IM3 tone when two tones are placed outside of the band (5.06 MHz and 8.06 MHz with a power level of -40.5 dBm).

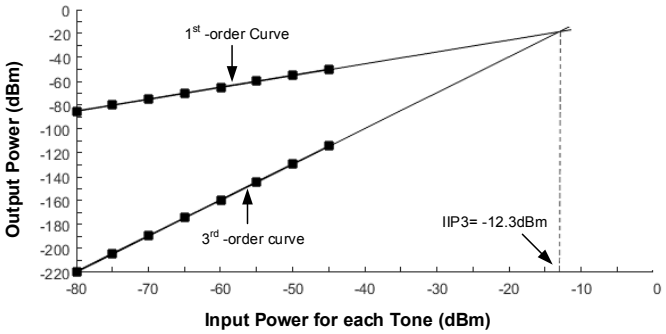


Fig. 11: Out-of-band IIP3 plot with two tones at 5.06 MHz and 8.06 MHz.

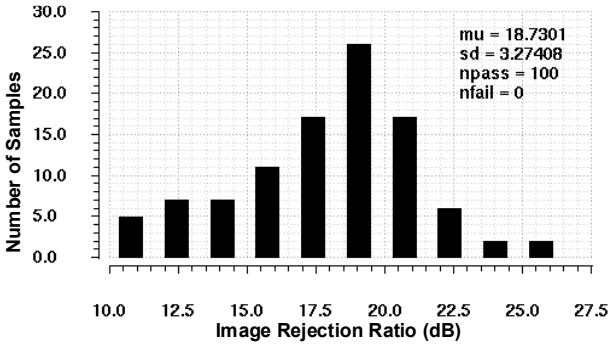


Fig. 12: IRR Monte Carlo simulation results with mismatch and process variation.

displays the simulated noise floor around the center frequency of the filter when the out-of-band tones are applied at the input. The out-of-band SFDR is 56.0 dB, which was obtained from the difference of the maximum output signal (in-band two-tone test as in Fig. 9), which is -47.0 dBV, and the IM3/noise output level when the two out-of-band tones are placed (Fig. 10), which corresponds to -103.0 dBV. Fig. 11 reveals that the out-of-band IIP3 is -12.3 dBm. The simulated integrated input-referred noise of the filter is 27.9 μV_{rms} over its -3dB bandwidth. Fig. 12 displays the histogram of the IRR after 100 Monte Carlo simulations using foundry-supplied device models with mismatch and process variation. The mean and standard deviation of the IRR of this filter stage are 18.7 dB and 3.27 dB, respectively. Note that, as in [3], at least two stages of the topology in Fig. 1 are typically cascaded to obtain higher-order filtering. Hence, the IRR of a multi-stage filter can be sufficiently high in practical applications (e.g., BLE IRR > 21 dB for the two-stage filter in [3]).

The figure of merit (FOM) from [3] is employed here to compare the performance of the filter to other works in the literature:

$$FOM = \frac{Power}{(\#Poles)(SFDR)(\sqrt{fc^2 + (fbw^2)/2})} \quad , \qquad (4)$$

where f_c is the center frequency and f_{bw} is the bandwidth of the filter. Table 1 provides a performance comparison with other reported complex bandpass filters. Since a first-order filter was presented in this paper as a prototype example, several per pole comparisons are included in Table 1. Among the reported complex filters, the proposed filter exhibits a competitive SFDR and FOM despite of its low power consumption and low supply voltage.

V. CONCLUSION

A large-signal linearization technique was applied to a complex bandpass filter, which is based on adaptive biasing with source degeneration using unbalanced differential pairs at the filter input in order to increase the linear range. A new adaptive biasing circuit was presented to extend the frequency range of this design approach from 26 MHz to 73 MHz with reduced power dissipation. The filter was designed in 130nm CMOS technology with a 0.6 V supply voltage. It has a simulated passband gain of 26.4 dB at 2 MHz, a power consumption of 26.1 µW, and an image rejection ratio of 22 dB. Its simulated out-of-band SFDR is 56.0 dB thanks to the large-signal linearization method.

Table 1: Performance comparison

	This work	[3]	[4]	[5]	[6]	[7]	[8]	[10]	[11]
Technology (nm)	130	130	350	350	180	180	350	180	180
Order	1	2	12	12	6	4	12	4	5
Topology	G_m-C	G_m-C	Current Mirror	G_m-C	CA-RC	Active RC	Current Mirror	CA-RC	G_m-C
Bandwidth (MHz)	0.6	1	0.9	1	1	2	1	1	1.17
Center Frequnecy (MHz)	2.06	2	2	2	3	1	1	3	0.995
Gain (dB)	26.4	46	N/A	15	N/A	N/A	N/A	N/A	18.4
Gain/pole (dB)	26.4	23	N/A	1.2	N/A	N/A	N/A	N/A	3.68
Image Rejection (dB)	22.06	34	28	45	54	52	49	56	48
Image Rejection/Pole (dB)	22.06	17	2.3	3.7	9	13	4.08	14	9.6
Supply Voltage (V)	0.6	0.8	1.5	2.7	2.7	1.8	1.5	1.8	1.2
Power Consumption (µW)	26.1	42	4710	12690	2380	5400	3200	1000	640
Power/Pole (µW)	26.1	21	392.5	1057.5	396.7	1350	266.7	250	128
Noise (μV_{rms})	27.9	5.7	N/A	29	89	46	N/A	73	50.4
SFDR (dB) Out-of-band & In-band	56.0 & 52.32	52.7 & N/A	53.8 & 40.4	61.1 & 45.2	75.3 & 64.8	80.5 & 69.8	56.3 & 45.42	77.8 & 65.8	70 & N/A
IIP3 (dBm) Out-of-band & In-band	-12.3 & -36.1	-12 & N/A	N/A & N/A	N/A & N/A	45 & 29.2	47 & 31	-57.5 & -73.86	47 & 29	24 & N/A
FOM (fJ)	0.03	0.05	0.5	0.3	0.002	0.006	0.7	0.001	0.01

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