Instrumentation Amplifier and Current Injection Circuit Design for Input Impedance Boosting in Biopotential and Bioimpedance Measurements

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Abstract:

This paper describes an instrumentation amplifier (IA) architecture with a mechanism that generates negative capacitances at its input. Two 8-bit programmable capacitors between the input stage and the current feedback loop of the IA allow adaptive cancellation of the input capacitances from the electrode cables and printed circuit board. The proposed negative capacitance generation technique can improve the input impedance from a few megaohms to above 500 MΩ without significant impact on performance parameters such as the common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), total harmonic distortion (THD), and noise. Furthermore, a current injection circuit is introduced for on-chip input impedance estimation. An operational transconductance amplifier (OTA) and associated key design concepts are presented in this paper that achieve a transconductance of 25 pS and an output impedance above 4 GΩ. The IA and the test current generator were designed and simulated using 0.13µm CMOS technology.

Keywords: Instrumentation amplifier; negative impedance converter; input capacitance cancellation; biopotential measurement; bioimpedance measurement; negative capacitance generation feedback; test current generation; low-transconductance operational transconductance amplifier

1 Introduction

Battery-powered portable or implantable biopotential and bioimpedance measurement devices are becoming increasingly widespread in the medical diagnostics field. The signal acquisitions of the main biosignal-sensing applications such as electroencephalography (EEG) and electrocardiography (ECG) involve voltage measurements from a few microvolts to several millivolts [1-3]. Biopotentials are conventionally acquired using electrodes covered with electrolyte gels or solutions to decrease the contact impedance at the skin interface to values below 10 kΩ. However, wet-contact measurements cause discomfort and dry out in novel long-term monitoring applications such as in brain-computer interfaces where EEG signals are acquired and analyzed over hours or longer [4].

In general, dry electrodes such as inexpensive Ag/AgCl are better suited for long-term monitoring, but their use is associated with increased contact resistances that can be above 1 MΩ [1]. This characteristic complicates the measurement of small biopotentials in the range of a few microvolts for EEG applications by requiring very high input impedance at the analog front-end amplifier of at least 500 MΩ [5]. Nevertheless, a significant problem is that this impedance is affected by parasitic capacitances of the integrated circuit package as well as electrode cable and printed circuit board (PCB) capacitances that could be as high as 50-200 pF at the input of an instrumentation amplifier (IA), as shown in Fig. 1. For instance, when the goal is to record EEG signals with frequencies up to 100 Hz, an interface capacitance of 200 pF would limit the input impedance at 100 Hz to approximately 8 MΩ, which would cause excessive attenuation such that the EEG signal cannot be measured reliably.

A possible solution for boosting input impedance would be to add a classical negative impedance converter (NIC) at the input of the IA. Fig. 2 shows a simplified NIC circuit that could be used to generate a negative capacitance at the input node of the IA if the component Z is a capacitor [6]. However, this approach would require an additional amplifier, whose power and area consumption is undesirable. Furthermore, the additional noise from the operational amplifier at the input of the IA would have to be carefully assessed. The negative capacitance

generation scheme proposed in this paper is integrated into the IA and thereby avoids an extra amplifier.

The discussed IA is designed as part of a larger project in which the goal is to automate the input capacitance cancellation as visualized in Fig. 1 with on-chip monitoring using a digital signal processor (DSP) and with a programmable capacitor bank within the IA for tuning [7]. The calibration system will include an on-chip test current generator (i_{test}) with high output impedance and low output noise. As shown in Fig. 3, the test current generator consists of a relaxation oscillator, a limiter, a frequency divider, and an operational transconductance amplifier (OTA) [8-9]. In calibration mode, the test currents will be injected to generate a voltage swing at the instrumentation amplifier input, which will be amplified and lowpass-filtered in the analog EEG front-end blocks for input impedance evaluation based on amplitude estimation with voltage level detectors or an analog-to-digital converter (ADC).

This paper concentrates on design aspects of two critical circuits in Fig. 1: the IA with negative capacitance generation and the OTA that injects the test current (i_{test}) for input impedance evaluation. IA design with input capacitance cancellation for impedance boosting has general usefulness in emerging biopotential and bioimpedance measurement applications regardless of how the tuning method is implemented. The proposed IA design method is introduced in Section 2, which includes a comprehensive analysis of the IA's small-signal model and the negative capacitance generation method. The proposed low-transconductance OTA for test current generation is described and analyzed in Section 3. Simulation results of the IA with input capacitance cancellation are presented in Section 4 and compared to the results of an identical IA without input capacitance cancellation. The assessment of the IA's input impedance in Section 4 is conducted together with the test current generator. Conclusions are provided in Section 5.

2 Instrumentation Amplifier with Negative Capacitance Generation Feedback

Fig. 4(a) shows the schematic of the widely used IA topology with direct current feedback, where the DC gain of the IA is decided by the ratio R_2/R_1, and the dominant pole depends on R_2 and C_2 [7, 10-11]. In Fig. 4(a), V_{bias} is derived from a reference current and a diode-connected transistor to set the DC current of M_{tail}. In order to test the input impedance of the IA, resistor R_2 has been designed with digital programmability to implement four different gain modes as illustrated in Fig. 4(b), where the smallest gain setting is 20 dB. Amplifier B1 was realized as in [10]. Fig. 4(c) shows the input bias circuity of the IA using pseudo-resistors [12]. The pseudo-resistors ensure high impedances and a stable commode-mode DC voltage ($V_{cm\text{-}DC}$) at the input nodes (v_{i+}, v_{i-}) of the IA. The effective impedances from the inputs (v_{i+}, v_{i-}) of the IA to V_{bias} are 4.7 GΩ at DC and 3.36 GΩ at 100 Hz, respectively. The transfer functions from the inputs (v_{i+}, v_{i-}) to v_A, v_B, v_C, v_D, v_E, v_F, v_H, v_I, v_J, v_K, and v_o are provided in Section II-A to evaluate the possibilities for negative capacitance generation feedback (NCGFB). Since nodes v_C and v_D in Fig. 4(a) are the most appropriate locations to obtain suitable gains for generating negative capacitances at the inputs (v_{i+}, v_{i-}), the NCGFB realization at these two nodes is elaborated in Section II-B.

A. Instrumentation amplifier small-signal model analysis

Fig. 5(a) shows the small-signal model of the IA's input stage and the current feedback loop for solving the transfer functions from the inputs to internal nodes. All parasitic capacitances are omitted during the analysis because the typical applications of this IA are at frequencies below 1 kHz. It is also noteworthy that the small-signal inputs (v_A and v_B) of the differential pair (M_5 and M_6) in the feedback loop are not truly differential due to the asymmetric characteristic looking into v_A (M_3 is diode-connected) and v_B (M_4 is not diode-connected). Hence, the phase of v_B follows that of v_A, and v_G is not a virtual ground. For this reason, the small-signal drain-source resistance ($1/g_{ds,Mtail}$) of M_{tail} should be taken into account during the analysis.Note that the conditions $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$, $g_{m7} = g_{m8}$, $g_{m9} = g_{m10}$, and $g_{mb5} = g_{mb6}$ are valid for this analysis in the absence of device mismatches.

Furthermore, the same definitions as in [7] are used next: $v_{in} = v_{i+} - v_{i-} = v_E - v_F$, where $v_{i+} = v_{in}/2$ and $v_{i-} = -v_{in}/2$. With these definitions, the following voltage gains from v_{in} to v_{A-G} can be derived from equations (A-1) to (A-8) in the Appendix:

$$A_{V,A} = \frac{v_A}{v_{in}} = \frac{g_{m,M7} \cdot g_{ds,Mtail}}{D}, \tag{1}$$

$$A_{V,B} = \frac{v_B}{v_{in}} = \frac{2g_{m,M7}}{g_{m,M5} \cdot g_{m,M9} \cdot R_1} + \frac{g_{m,M7} \cdot g_{ds,Mtail}}{D}, \tag{2}$$

$$A_{V,C} = \frac{v_C}{v_{in}} = \frac{1}{g_{m,M9} \cdot R_1} - \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M9} \cdot D}, \tag{3}$$

$$A_{V,D} = \frac{v_D}{v_{in}} = -\frac{1}{g_{m,M9} \cdot R_1} - \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M9} \cdot D}, \tag{4}$$

$$A_{V,E} = \frac{v_E}{v_{in}} = \frac{1}{2} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M1} \cdot D}, \tag{5}$$

$$A_{V,F} = \frac{v_F}{v_{in}} = -\frac{1}{2} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M1} \cdot D}, \tag{6}$$

$$A_{V,G} = \frac{v_G}{v_{in}} = \frac{2 \cdot g_{m,M3} \cdot g_{m,M7}^{\ 2}}{g_{m,M9} \cdot D}; \tag{7}$$

where: $D=[(2 \cdot g_{m,M5}+2 \cdot g_{mb,M5}+g_{ds,Mtail}) \cdot g_{m,M3} \cdot g_{m,M7}-g_{m,M5} \cdot g_{m,M9} \cdot g_{ds,Mtail}] \cdot R_1$.

The voltage gains from v_{in} to v_{H-K} and to v_o in Fig. 5(b) can be found from (A-9) to (A-14) in the Appendix:

$$A_{V,H} = \frac{v_H}{v_{in}} = \frac{2}{g_{m,M13} \cdot R_1} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M13} \cdot D}, \tag{8}$$

$$A_{V,I} = \frac{v_I}{v_{in}} \approx \frac{Z_2}{R_1} + \frac{2}{g_{m,M13} \cdot R_1} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M13} \cdot D}, \tag{9}$$

$$A_{V,J} = \frac{v_J}{v_{in}} = \frac{g_{m,M13}}{g_{m,M15}} \cdot \left(\frac{2}{g_{m,M13} \cdot R_1} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M13} \cdot D} \right), \tag{10}$$

$$A_{V,K} = \frac{v_K}{v_{in}} \approx \frac{g_{m,M13}}{g_{m,M15}} \cdot \left(\frac{2}{g_{m,M13} \cdot R_1} + \frac{g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}}{g_{m,M13} \cdot D} \right), \tag{11}$$

$$A_{V,o} = \frac{v_o}{v_{in}} = \frac{g_{m,M11} \cdot Z_2}{g_{m,M9} \cdot R_1} = \frac{Z_2}{R_1}. \tag{12}$$

From (1) and (2) it can be observed that $A_{V,B}$ is always larger than $A_{V,A}$, and that $A_{V,A}$ and $A_{V,B}$ have the same phase. Equations (3) and (4) show that $A_{V,C}$ and $A_{V,D}$

are in anti-phase. Although these gain magnitudes are not equal, nodes v_C and v_D are well-suited as points at which the NCGFB can be added. From (5) and (6), the gains $A_{V,E}$ and $A_{V,F}$ have the same phase if $g_{m,M3} \cdot g_{m,M7} \cdot g_{ds,Mtail}/(g_{m,M1} \cdot D) > 0.5$, which would complicate the use of nodes v_E and v_F for NCGFB. The gains $A_{V,H}$, $A_{V,I}$, $A_{V,J}$ and $A_{V,K}$ in the output stage of the IA have the same phase. Thus, these nodes are not suitable for adding the proposed NCGFB.

B. Negative capacitance generation feedback analysis

Fig. 6 shows the proposed NCGFB implementation with an 8-bit digitally-controlled capacitor (C_p - $2^7 \cdot C_p$) and one fixed capacitor (C_{p0}) between nodes v_{i+} and v_C. The maximum and minimum capacitance values occur with $S_{p7,6,5,4,3,2,1,0}$ = [11111111] and [00000000] respectively, where '1' or '0' indicate that the switch is turned "on" or "off". The same programmable capacitor configuration was connected between nodes v_{i-} and v_D with control switches $S_{n7,6,5,4,3,2,1,0}$. Neglecting the very high resistance at the gates of the transistors, the input impedances (Z_{inp} and Z_{inn}) in Fig. 1 can be derived as

$$Z_{inp}(s) = \frac{1}{sC_{sp} + sC_{total,i+}}, \tag{13}$$

$$Z_{inn}(s) = \frac{1}{sC_{sn} + sC_{total,i-}}; \tag{14}$$

where C_{sp} and C_{sn} are the lumped cable and PCB capacitances at the positive and negative inputs of the IA, and $C_{total,i+}$ and $C_{total,i-}$ represent the IA's total equivalent capacitances at the inputs v_{i+} and v_{i-} respectively. The tuning range of the 8-bit capacitors can be designed to compensate for the 50-200 pF capacitances from the cables and PCB by generating negative $C_{total,i+}$ and $C_{total,i-}$ values through the presented NCGFB configuration. This property becomes evident after using Miller approximations to express $C_{total,i+}$ and $C_{total,i-}$ in terms of the previously derived gains:

$$\begin{aligned} C_{total,i+} = {} & C_{gs,M1}(1 - 2A_{V,E}) + C_{gd,M1}(1 - 2A_{V,A}) \\ & + [C_{p0} + C_p \cdot \sum_{i=0}^{7}(2^i \cdot S_{pi})] \cdot (1 - 2A_{V,C}) \end{aligned}, \tag{15}$$

$$\begin{aligned} C_{total,i-} = {} & C_{gs,M2}(1 + 2A_{V,F}) + C_{gd,M2}(1 + 2A_{V,B}) \\ & + [C_{n0} + C_n \cdot \sum_{i=0}^{7}(2^i \cdot S_{ni})] \cdot (1 + 2A_{V,D}) \end{aligned}, \tag{16}$$

where $C_{gs,X}$ and $C_{gd,X}$ are the parasitic gate-source and gate-drain capacitances of transistor M_X. Note that $A_{V,D}$ is negative based on (4), and that this negative gain dominates in (16). Therefore, the total equivalent capacitance in (16) is negative.

3 Test Current Generator Design

The test current generator in Fig. 1 injects AC current i_{test} into the IA input such that a corresponding voltage swing appears, which depends on the magnitude of the input impedance. The on-chip oscillator in Fig. 3 generates a 20 kHz rail-to-rail square wave, which is divided down to 19.5 Hz. A voltage limiter converts the rail-to-rail signal to an 80 mV differential peak-to-peak level that is compatible with the OTA input requirement. The OTA's transconductance is designed to be 25 pS, which makes the i_{test} magnitude equal to 1 pA. If the input impedance of the IA is boosted to above 2.5 GΩ at 19.5 Hz, the voltage swing at the IA's inputs would be more than 5 mV peak-to-peak because of the harmonics. This voltage swing is amplified and filtered by the following stages in the analog front-end. The requirements of the OTA for test current generation are stringent because of its interface with the IA:

1.) The output impedance of the OTA should be high enough to avoid excessive loading effects even when the input impedance of the IA reaches more than 500 MΩ at frequencies up to 100 Hz.
2.) The output voltage amplitude is limited by the IA's input range that is designed for EEG signals, requiring an OTA transconductance in the sub-nano-Siemens range.
3.) The output noise of the OTA should be small enough compared to the small voltage swing at the IA input during the current injection test mode. Here, we assume an output noise target of less than 100 μV_{rms} integrated from 0.01 Hz to 100 Hz.
4.) The power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) of the OTA should be similarly high as in typical analog front-ends for biosignal processing applications.
5.) As part of the test current generator, it is preferred that the OTA has small layout dimensions and low power consumption.

A. Sub-nano-Siemens transconductance design

The target value of the IA input impedance is 500 MΩ up to 100 Hz. A differential test current magnitude of 1 pA was chosen to keep the input voltage swing at the injection node limited to a few millivolts, which maintains linear operation of the IA and lowpass filter. Hence, the OTA's transconductance was designed to be approximately 25 pS. Its differential inputs are limited to 40 mV_{peak}. There are several methods to design sub-nano-Siemens OTAs [12]. In the proposed architecture shown in Fig. 7, transistors M_2-M_6 in Fig. 7(a) implement a series-parallel current division with an 8:1 ratio, which was adapted from the OTA design with 33 pS transconductance in [13]. To generate precise picoampere-range bias currents such as I_{b2}, the current splitting technique from [14] was applied as shown in Fig. 7(b) with N = 10 and I_{REF} = 150 nA, which is a layout efficient configuration to obtain such small currents. With these two structures, a transconductance of 25 pS is obtained at the cost of the input stage's linearity performance which is not critical in this amplitude detection application.

B. Design of an OTA output stage with high output impedance, low noise, and high PSRR

As depicted in Fig. 7(a), the output stage of the OTA is composed of transistors M_3-M_{10}, which includes a PMOS common-gate structure (M_8-M_{10}). Biased with a DC current less than 1 nA, the output impedance could reach tens of gigaohms without M_8-M_{10}. Such high output impedance is desirable for current injection at the instrumentation amplifier input. However, without M_8-M_{10}, the output noise of the OTA would be several millivolts because of the low transconductance of the transistors in the output stage and the high output impedance. In order to alleviate the trade-off between low output noise and high output impedance in the conventional output stage (M_3-M_7), a common-gate structure whose input transistor is M_8 was added to lower the output impedance to approximately $1/g_{m8}$. Hence, the OTA's low-frequency output impedance can be estimated with equation (17), where g_{m8} is the transconductance of M_8. This modification significantly reduces the output noise.

$$r_{out,OTA} \approx \frac{1}{g_{m8}} \quad . \tag{17}$$

In our previous work [9], M_8 was biased with a diode-connected NMOS driven by a reference current. This creates sensitivity to temperature and process variations. For example, when the temperature changes, the DC bias voltage provided by the diode-connected NMOS transistor changes due to the temperature's effect on the threshold voltage. Since the gate of M_8 is a sensitive node in the output stage, especially in a scenario where the bias current is only a few picoamperes, the output impedance (approximately $1/g_{m8}$) would change significantly in response to a temperature change. Even though the simple biasing structure consisting of a diode-connected NMOS and current mirrored from I_{REF} has the advantage of high PSRR, it is not a good choice when it is required to ensure a high output impedance that is insensitive to temperature and process variations.

Fig. 7(c) presents the topology for the generation of most of the OTA's bias voltages, and Fig. 8 displays the proposed biasing circuit for the PMOS transistor in the common-gate structure of the OTA output stage in Fig. 7(a). The asterisks of M_{25}^* and M_{26}^* indicate that these composite transistors consist of multiple unit transistors in series with shared gate connections, which are implemented in the same way as M_3-M_6 in Fig. 7(a). Currents I_{b1}-I_{b4} are generated from the current splitting structure in Fig. 7(b), and I_{b2}'-I_{b4}' are bias currents produced from I_{b2}-I_{b4} using simple current mirrors, respectively. There are two benefits of the structure in Fig. 8: one is a high OTA PSRR, and the other is that the voltage V_{pb2} adapts to compensate for temperature and process variations.

Assuming that I_{REF} in Fig. 7(b) is obtained from a current reference circuit with very high PSRR, then I_{b1} is also robust to supply voltage ripples because it is mirrored from I_{REF} using transistors that experience the same gate-source voltage fluctuations. Thus, if there is a ripple on V_{DD}, the fluctuation at node A in Fig. 8 can be ignored because I_{b1} remains almost constant despite of the ripple from V_{DD}. Hence, the mirrored current flowing into M_{15} also maintains its value, which causes the gate voltage of M_{15} (node B) to follow the ripple at V_{DD} because the source-gate voltage (V_{SG}) of M_{15} is constant as a result of its constant current. As a consequence, M_{16} also has an almost constant source-gate voltage in the presence of a supply voltage ripple, and therefore the drain current flowing into the diode-connected load is quite insensitive to ripple on V_{DD}. Note that the

voltage at node C is produced with the same configuration as the bias voltage V_{pb2} in our previous work [9], which exhibits a decent PSRR. With a robust voltage at node C and current mirrored from I_{b1}, the voltage V_{pb2} can be expressed as:

$$V_{pb2} = V_C - V_{SG24} - V_{GS25}, \tag{18}$$

where V_{SG24} is the source-gate voltage of M_{24} and V_{GS25} is the gate-source voltage of M_{25}^*. Both voltages are insensitive to power supply ripple because M_{24} and M_{25}^* are biased with the current that is mirrored from I_{b1}. Hence, V_{pb2} exhibits an equally good PSRR as the voltage V_C at node C. In the OTA output stage in Fig. 7(a), M_7 is biased with a diode-connected PMOS transistor (M_{27} in Fig. 7(c)). Therefore, the ripple effect from V_{DD} through M_7 to V_{out} is negligible. As revealed by simulation results and comparison in Section 4, the PSRR of the OTA with the proposed biasing structure is higher than that of our previous design [9].

If we lump the gate-source voltage changes due to temperature and process variations as threshold voltage changes, the deviation of V_{pb2} can be expressed as:

$$\begin{aligned} \Delta V_{pb2} &= \Delta V_C - \Delta V_{SG24} - \Delta V_{GS25} \\ &= \Delta V_{THN} - \Delta V_{THP24} - \Delta V_{THN} = -\Delta V_{THP24} \end{aligned}. \tag{19}$$

The underlying assumption in the above equation is that the threshold voltage changes of the composite transistor $M_{17\text{-}23}$ (formed by M_{17} - M_{23}) are the same as the changes of the composite transistor M_{25}^*. Hence, in the presence of temperature or process variations, the change $\Delta V_{pb2} = -\Delta V_{THP24}$ can compensate for the change of the threshold variation of M_8 as long as the bias current or copies of the bias currents (I_{b2}', I_{b3}', and I_{b4}') are generated as robustly as previously described:

$$\Delta(V_{SG8} - V_{THP8}) = \Delta V_{THP24} - \Delta V_{THP8} \approx 0. \tag{20}$$

Partial cancellation necessitates that the PMOS transistors are laid out carefully (i.e., in proximity to each other with a matching technique) such that their threshold variations are highly correlated. With the proposed structure, the variation-induced $\Delta(V_{SG8} - V_{THP8})$ is compensated by $\Delta V_{pb2,}$ making the output impedance of the OTA ($\approx 1/g_{m8}$) more robust.

4 Simulation Results

The IA in Fig. 4(a) was designed in 0.13µm CMOS technology for EEG signal measurement applications. A commensurate IA without NCGFB was designed as reference for comparison. Table 1 contains the key design parameters of both IAs. Identical supply voltages of 1.2 V and total currents of 78 µA were used for both designs. C_{p0}, C_p, C_{n0} and C_n were selected to cover cable/PCB capacitances from 50 pF to 200 pF for the IA across all device corner model cases. Notice that C_{p0} is not equal to C_{n0}, and that C_p is not equal to C_n due to the different gains and phases, as discussed in Section 2-A. Implementing large capacitors as off-chip capacitors is frequently done in analog front-ends for biosignal acquisitions as in [2-3, 15]. Therefore, it is assumed here that C_2 would not be laid out on chip.

Table 2 summarizes the simulated specification parameters of both IAs. The two designs have the same gain, bandwidth, root-mean-square input offset voltage and noise in the typical corner case with C_{sp} = C_{sn}= 200 pF (Fig. 1). The common-mode rejection ratio (CMRR) was designed to be comparable to a commercial IA [16]. The Monte Carlo results in Fig. 9 were obtained with foundry-supplied statistical device models using activated process and mismatch variations. They show that there are no significant differences in the anticipated CMRR, PSRR, or THD of both IAs. Fig. 10 displays the simulated noise density versus frequency for both IAs, which is also not impacted by the addition of NCGFB circuits.

Fig. 11 shows the input impedances of Z_{inp} and Z_{inn} for both amplifiers in the typical corner case for different C_{sp} and C_{sn} values. The impedances at Z_{inp} and Z_{inn} for the IA with NCGFB reach 500 MΩ or more at 100 Hz. As described in Section 1, a tuning scheme, such as in Fig. 1, is required to adjust the programmable capacitors in Fig. 6 to a value that cancels most of the capacitance at each input. For example, the case with C_{sp} = C_{sn} = 100 pF in Fig. 11(a) requires that $S_{p7,6,5,4,3,2,1,0}$ = [01010110] and $S_{n7,6,5,4,3,2,1,0}$ = [01010001]. On the other hand, without the NCGFB method, the impedances at Z_{inp} and Z_{inn} are below 20 MΩ at 100 Hz, which fall short of the 500 MΩ requirement for measurements with dry electrodes [5]. Simulation results in Fig. 11(b) indicate that the IA with NCGFB has the capability to compensate for different cable capacitances at each input (C_{sp} = 200 pF and C_{sn} = 50 pF).

Fig. 12 shows the impedances at Z_{inp} for the IAs with and without NCGFB in different process corner cases with C_{sp}= 200 pF. The impedances at 100 Hz for the IA with NCGFB are over 500 MΩ in all corner cases after adjusting the switch settings ($S_{p7,6,5,4,3,2,1,0}$) of the capacitor array. In contrast, the impedances at 100 Hz for the IA without NCGFB are less than 20 MΩ in all process corner cases. The proposed technique boosts the input impedance significantly more than the method in [17], where the impedance increases from 6 MΩ to 30 MΩ. However, the trade-off is that the presented IA has higher power consumption compared to the 2 µW IA in [17].

Fig. 13 shows the simulated output impedance of the OTA in the test current generator for different temperature and process variation cases, which demonstrates that the output impedance is reliably high enough for current injection with the proposed biasing structure for the output stage. Table 3 summarizes the simulation results of the OTA's most important parameters for the target application. As discussed at the beginning of the Section 3, the design approach with the proposed OTA focuses on the realization of sub-nS transconductance with substantial output impedance, adequate output noise, as well as good CMRR and PSRR. These application-specific characteristics are needed for reliable pico-ampere current injection at the high-impedance input nodes of the instrumentation amplifier with a limited voltage swing to avoid saturation. As a consequence, this OTA is different from conventional low-transconductance OTA designs for filters with low cut-off frequency, which are typically optimized for low input-referred noise, low distortion, and high dynamic range [18]. Nevertheless, for comparison, Table 3 lists the reported parameters of some similar OTAs found in the literature. Fig. 14 displays the voltage swings (with and without NCGFB) at the IA's input using the described OTA for current injection. In an automated calibration such as in Fig. 1, this input signal would be amplified and filtered for impedance estimation through amplitude detection. The simulation result in Fig. 14 reveals that the input impedance is greatly boosted by the NCGFB activation, and that the voltage swing at the IA input is far above the noise level during the test current injection with the OTA.

5. Conclusion

This paper described an input impedance boosting technique for integrated instrumentation amplifiers and a test current generation circuit for the approach. Designed in 0.13μm CMOS technology, the operational transconductance amplifier for test current injection has a low transconductance of 25 pS. It also has high output impedance above 4 GΩ in the presence of variations to enable current injection testing for estimation of the instrumentation amplifier's input impedance.

The negative capacitance generation feedback of the instrumentation amplifier can boost its impedance from below 20 MΩ to above 500 MΩ at 100 Hz after the proper adjustment of digitally programmable capacitors. Based on Monte Carlo simulations, important performance parameters such as CMRR, PSRR and THD are not significantly affected by the proposed input capacitance cancellation technique.

Appendix

Without the effect of the NCGFB, the current summation equations at nodes 1 through 4 in Fig. 5(a) are:

$$\frac{v_E - v_F}{R_1} + g_{m,M1}(v_E - v_{i+}) + g_{m,M9}v_D = 0, \quad \text{(A-1)}$$

$$\frac{v_E - v_F}{R_1} - g_{m,M2}(v_F - v_{i-}) - g_{m,M10}v_C = 0, \quad \text{(A-2)}$$

$$g_{m,M2}(v_F - v_{i-}) - g_{m,M4}v_A = 0, \quad \text{(A-3)}$$

$$(g_{m,M5} + g_{mb,M5} + g_{m,M6} + g_{mb,M6} + g_{ds,Mtail})v_G - g_{m,M5}v_A - g_{m,M6}v_B = 0; \quad \text{(A-4)}$$

where $g_{m,M1}$-$g_{m,M10}$ are the transconductances of M_1-M_{10}, $g_{mb,M5}$ and $g_{mb,M6}$ are the body effect transconductances of M_5 and M_6, and $g_{ds,Mtail}$ is the small-signal drain-source admittance of M_{tail}. From Fig. 5(a), the voltages v_A, v_C, ,v_D, v_G can be expressed as

$$v_A = \frac{g_{m,M1}(v_E - v_{i+})}{g_{m,M3}}, \quad \text{(A-5)}$$

$$v_C = \frac{(g_{m,M5} + g_{mb,M5})v_G - g_{m,M5}v_A}{g_{m,M7}}, \quad \text{(A-6)}$$

$$v_D = \frac{(g_{m,M6} + g_{mb,M6})v_G - g_{m,M6}v_B}{g_{m,M8}}, \quad \text{(A-7)}$$

$$v_G = \frac{g_{m,M5}v_C + g_{m,M3}v_A}{(g_{m,M3} + g_{mb,M3})}. \quad \text{(A-8)}$$

For the output stage of the IA, the current summation equations at nodes 5 and 6 in Fig. 5(b) are:

$$\frac{(v_I - v_H)}{Z_2} + g_{m,M13}(v_I - v_o) + g_{m,M11}v_C = 0, \quad \text{(A-9)}$$

$$\frac{(v_I - v_H)}{Z_2} - g_{m,M14}v_H - g_{m,M12}v_D = 0; \quad \text{(A-10)}$$

where $Z_2 = R_2||(1/sC_2)$. Note that the design conditions $g_{m11} = g_{m12}$, $g_{m13} = g_{m14}$, and $g_{m15} = g_{m16}$ are assumed for this analysis in the absence of device mismatches. From Fig. 5(b), the voltages v_K, v_J, and v_o can be expressed as

$$v_K = \frac{g_{m,M13}(v_I - v_o)}{g_{m,M15}}, \quad \text{(A-11)}$$

$$v_J = \frac{g_{m,M14}v_H}{g_{m,M16}}, \quad \text{(A-12)}$$

$$v_o = A_{V,B1}(v_J - v_K). \quad \text{(A-13)}$$

Based on (A-11), (A-12) and (A-13), if the voltage gain ($A_{V,B1}$) of B1 is approximated to be infinite for simplicity, then v_o can be rewritten as

$$v_o \approx v_I - v_H \quad . \quad \text{(A-14)}$$

Note that $g_{m9} = g_{m11}$ is another condition used in this design.

Acknowledgement

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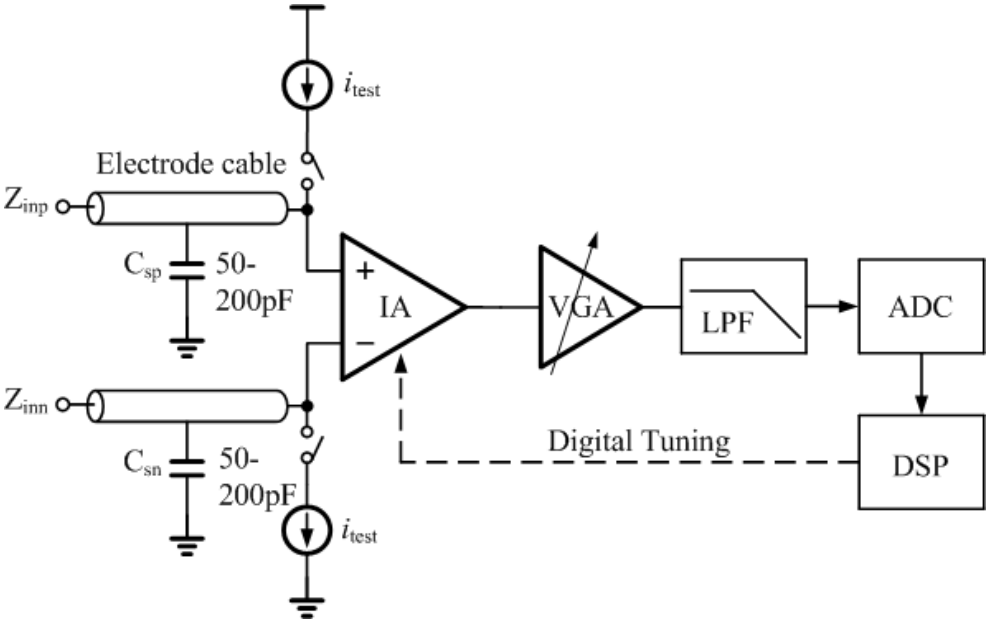


Fig. 1. Analog front-end for EEG signal measurements with electrode cable capacitances and calibration blocks for input impedance boosting.

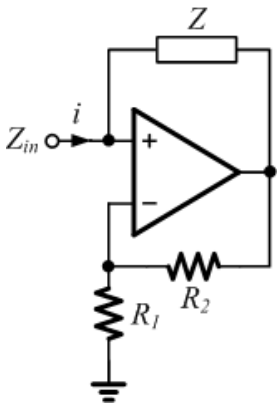


Fig. 2. Basic negative impedance converter (NIC), where $Z_{in} = -Z$ when $R_1 = R_2$.

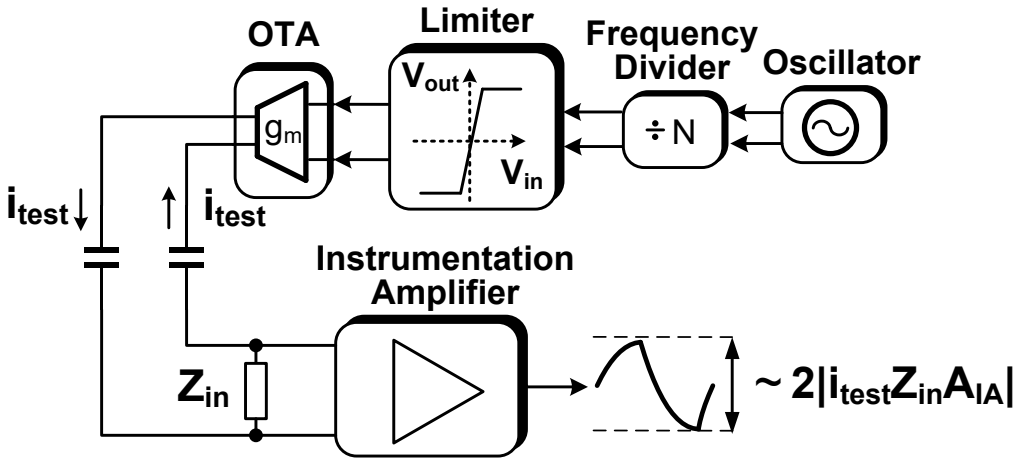
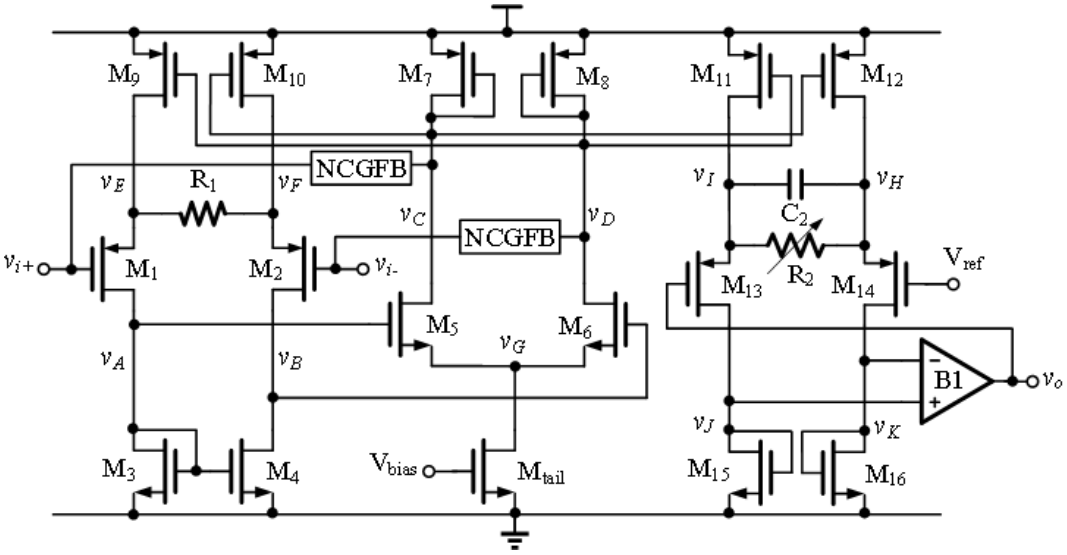
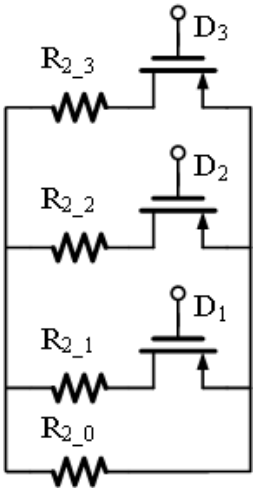


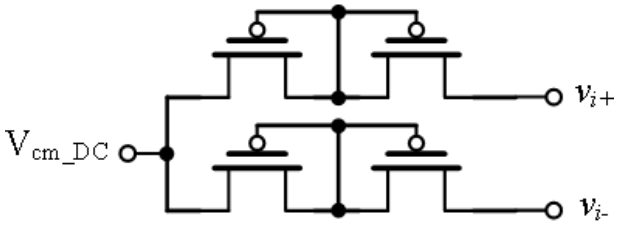
Fig. 3. Current injection with the test current generator.



(a)

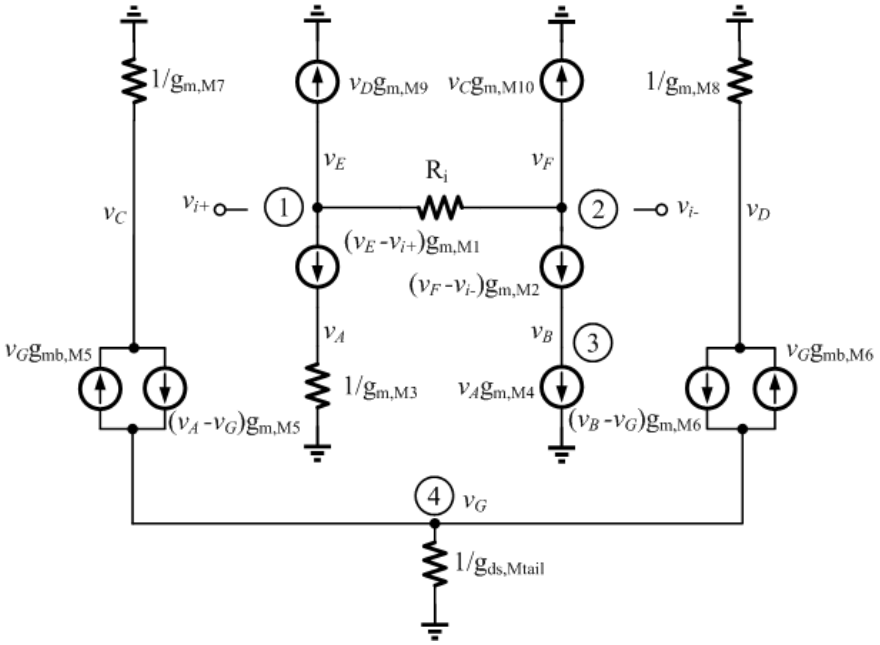


(b)

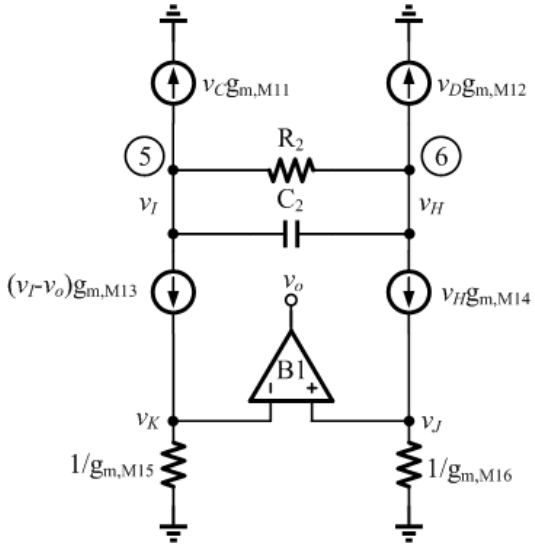


(c)

Fig. 4. (a) Instrumentation amplifier (IA) with direct current feedback and negative capacitance generation feedback (NCGFB); (b) variable R_2 implementation; (c) input bias circuitry.



(a)



(b)

Fig. 5. (a) Small-signal model of the IA's input and feedback stages; (b) small-signal model of the IA's output stage.

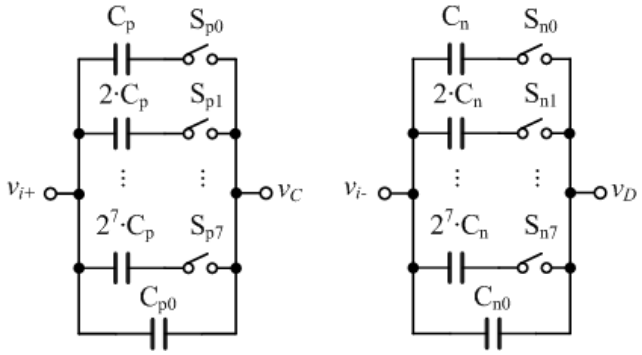


Fig. 6. Negative capacitance generation feedback (NCGFB) with programmable capacitors between nodes v_{i+} and v_C (and nodes v_{i-} and v_D).

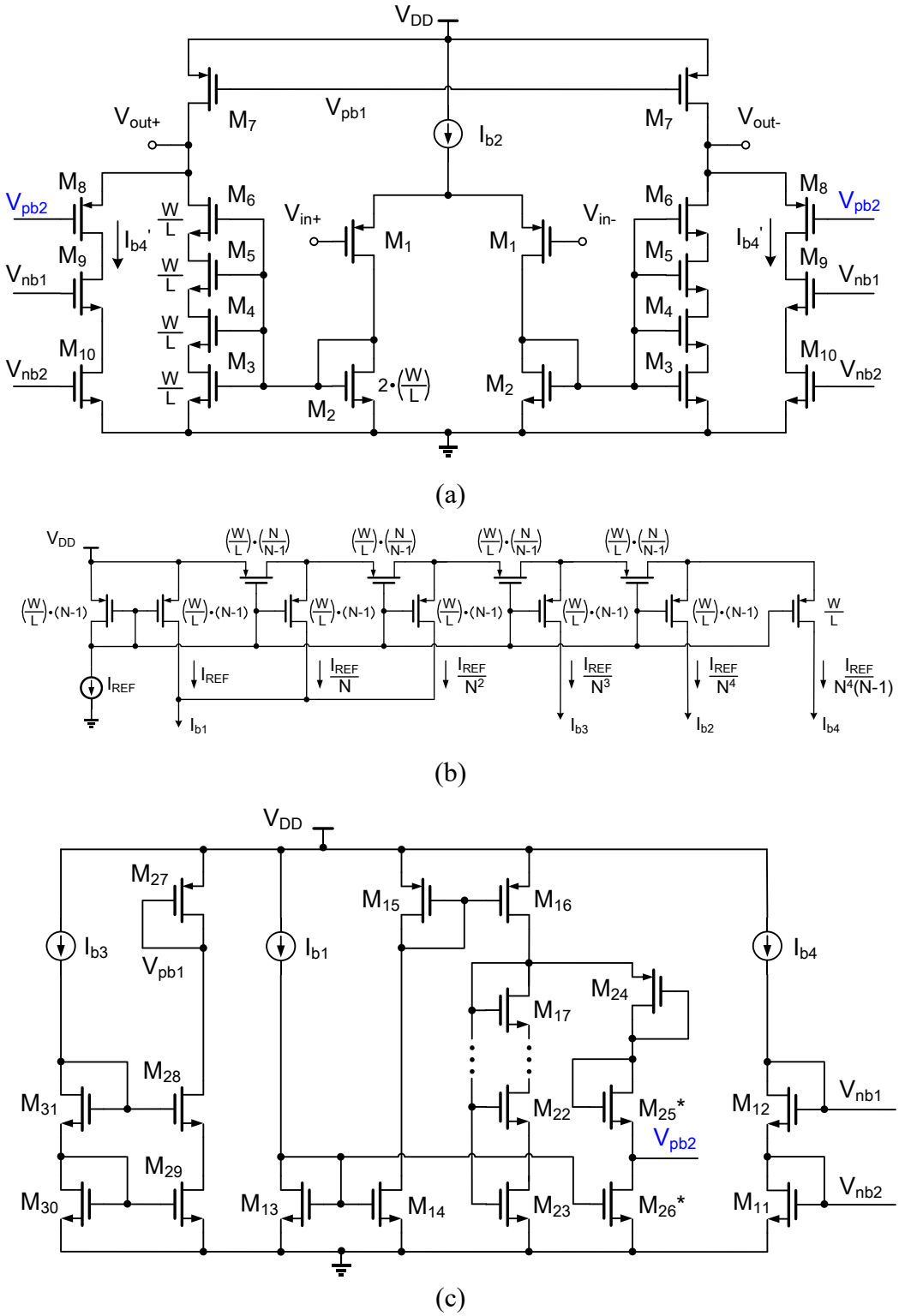


Fig. 7. Schematic of (a) the OTA core, (b) the bias current generation structure of the OTA (N = 10), and (c) the structure to generate the bias voltages of the OTA.

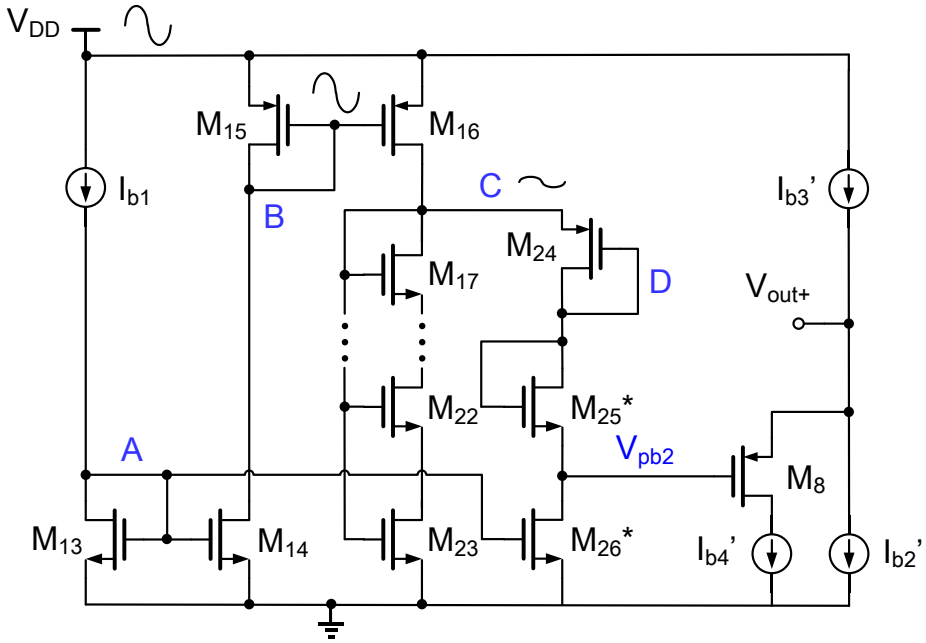


Fig. 8. Proposed biasing circuit for the OTA's output stage.

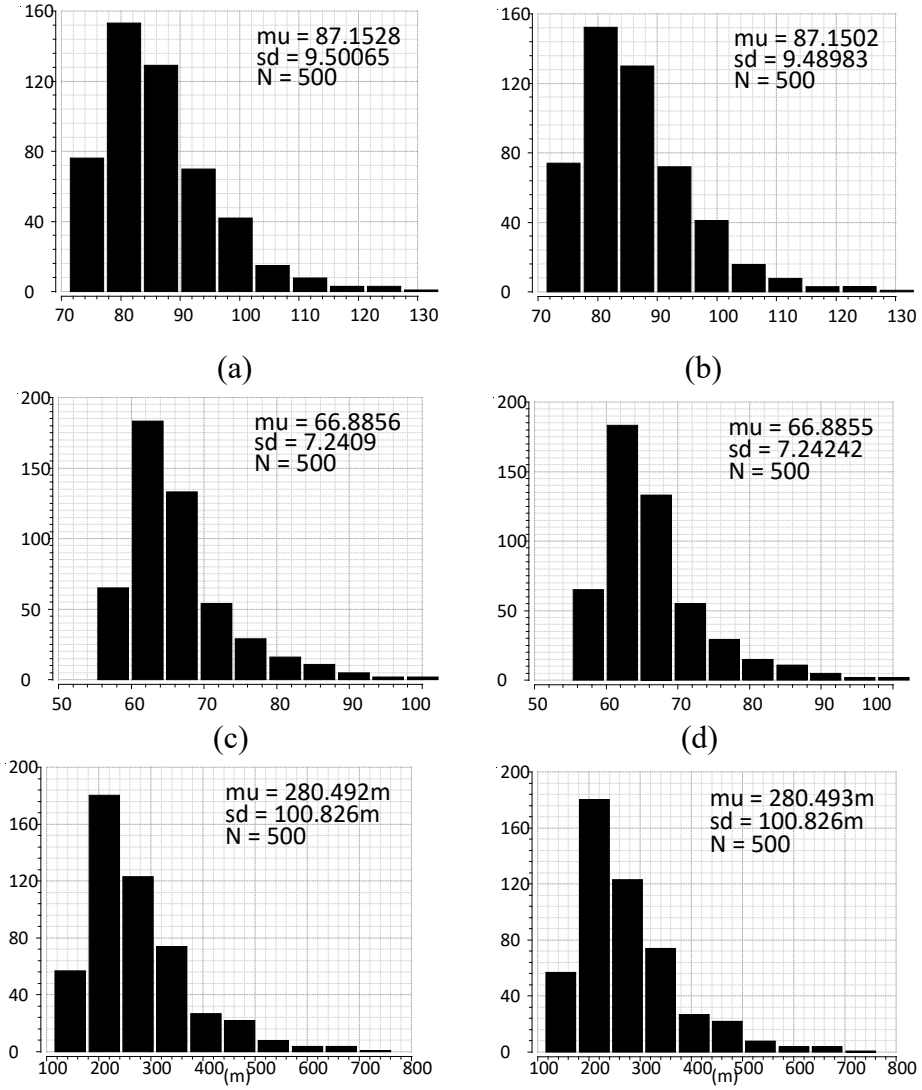


Fig. 9. Monte Carlo simulation results of both IAs.
CMRR: (a) IA without NCGFB and (b) IA with NCGFB,
PSRR: (c) IA without NCGFB and (d) IA with NCGFB,
THD: (e) IA without NCGFB and (f) IA with NCGFB

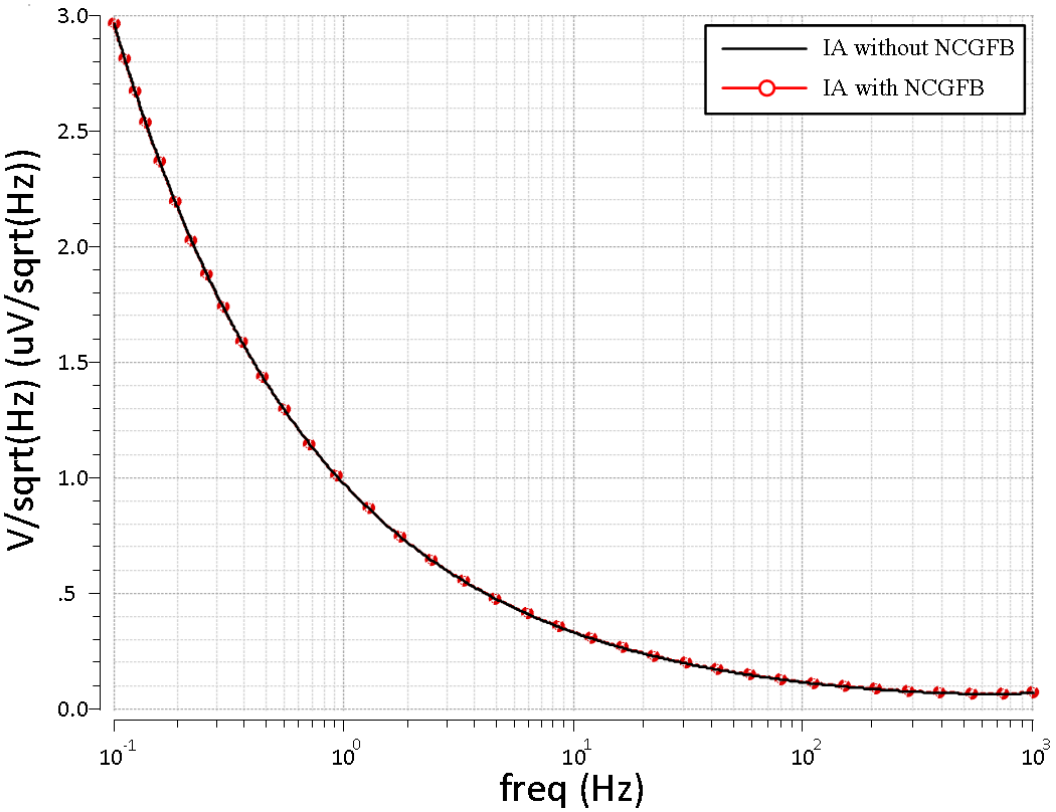
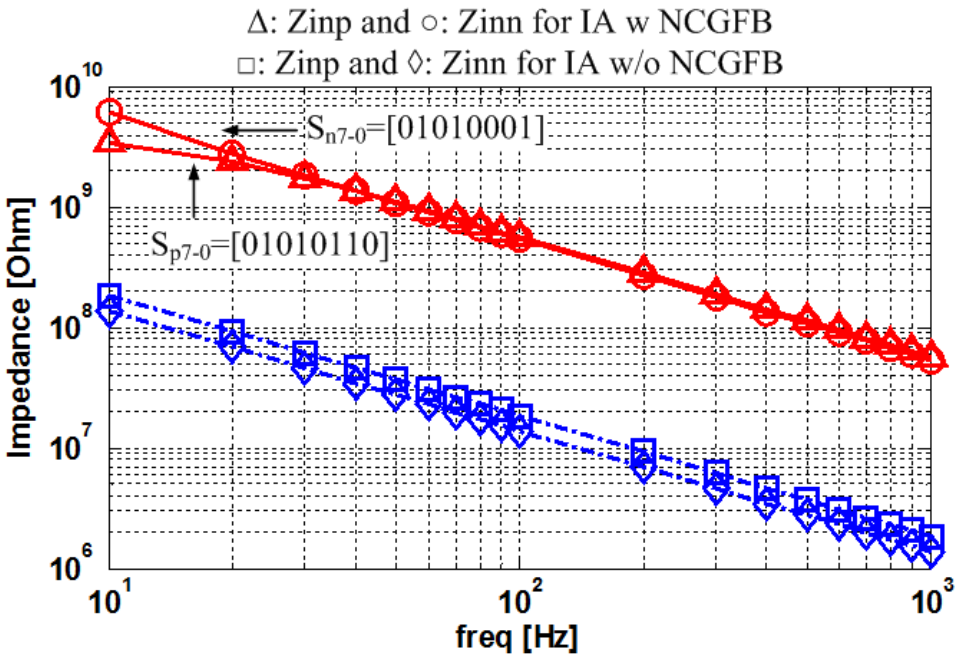
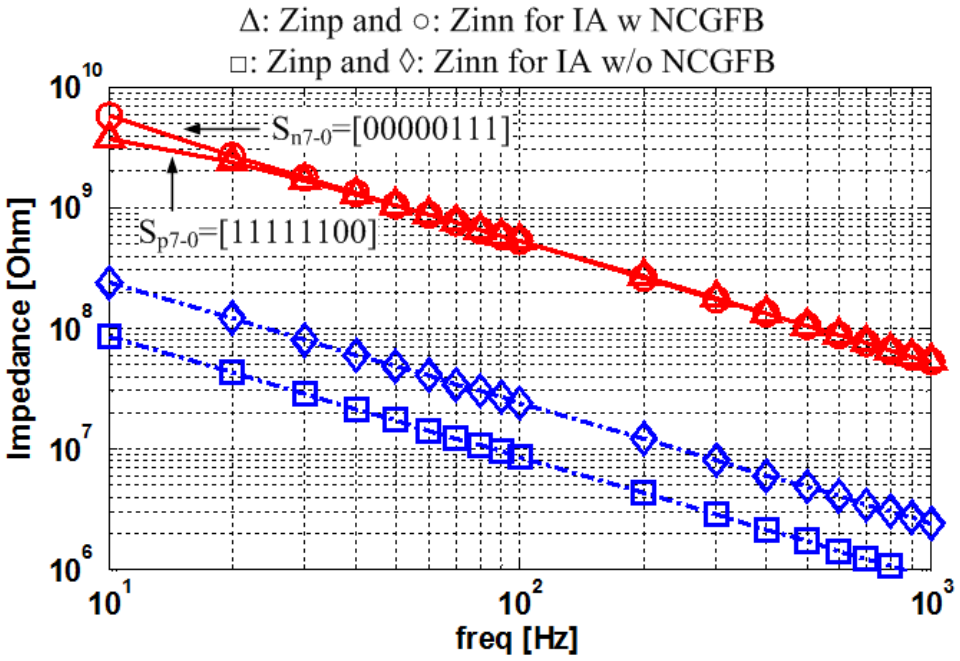


Fig. 10. Noise distributions of the IA without NCGFB and of the IA with NCGFB.



(a)



(b)

Fig. 11. Impedances at the IA inputs with and without NCGFB for different C_{sp} and C_{sn} values: (a) $C_{sp} = C_{sn} = 100$ pF, (b) $C_{sp} = 200$ pF and $C_{sn} = 50$ pF.

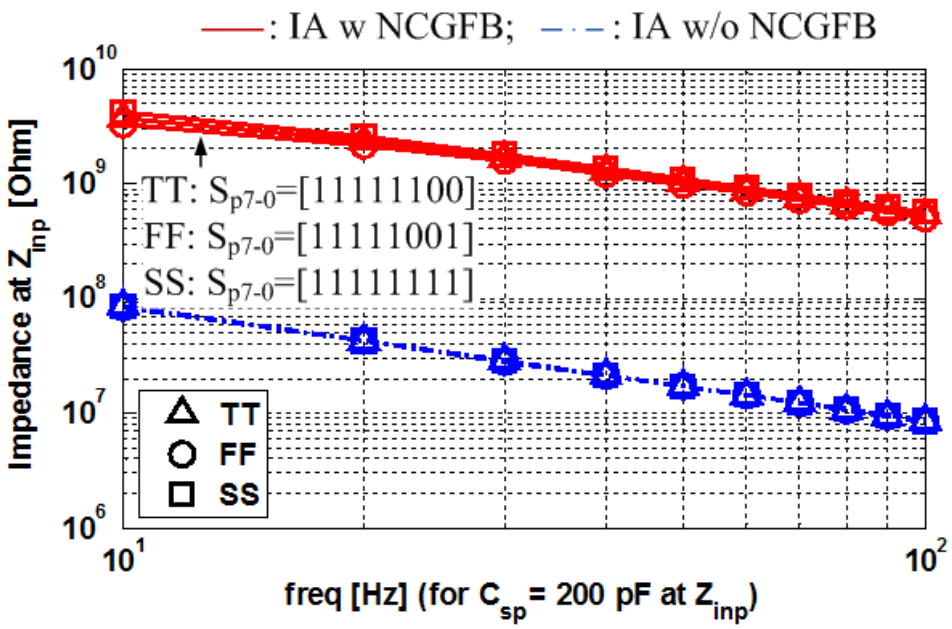


Fig. 12. Input impedance comparison (at Z_{inp}) for the IAs with and without NCGFB in different process corner cases.

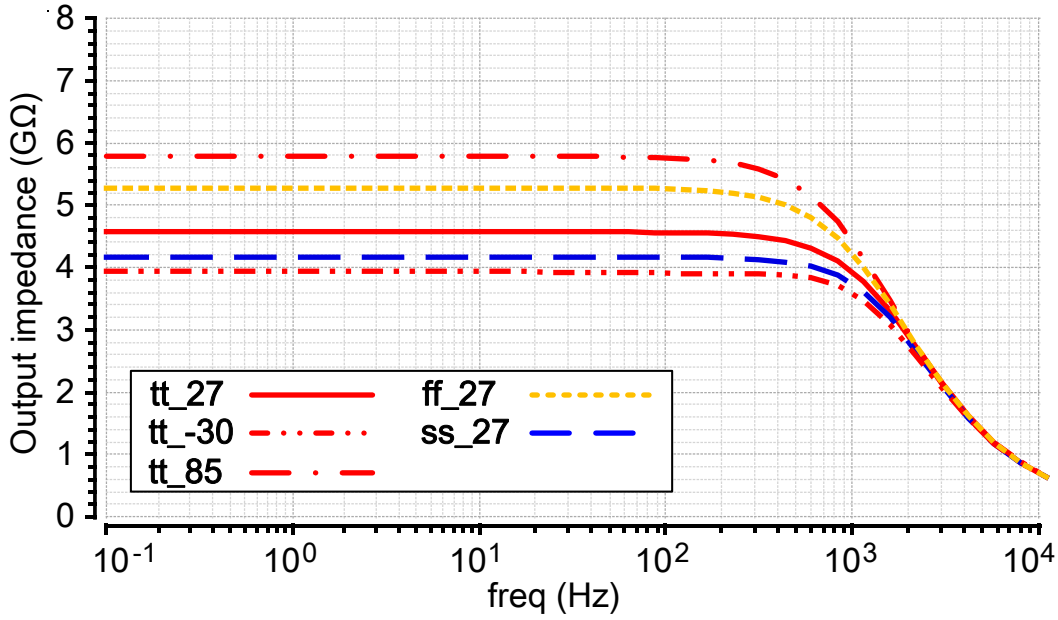


Fig. 13. Output impedance vs. frequency of the OTA with process and temperature variations.

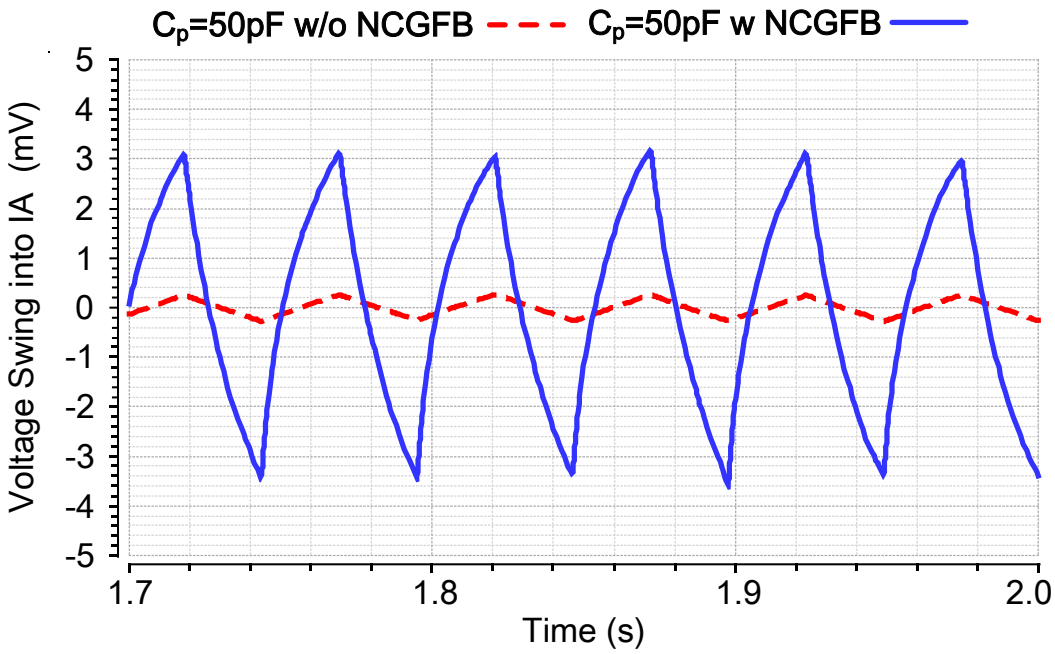


Fig. 14. Voltage swings at the IA input with current injection from the OTA for two cases: i.) with NCGFB, ii.) without NCGFB. (Noise was activated during the transient simulations based on the integrated noise density from 0.01 Hz to 100 Hz.)

Table 1. Parameters of the IA designs without and with NCGFB

Component/Parameter	**Without NCGFB**	**With NCGFB**
V_{DD}	1.2 V	1.2 V
Power supply current	78 µA	78 µA
R_1	0.7 kΩ	0.7 kΩ
R_2	40 kΩ	40 kΩ
C_2*	41,200 pF	41,200 pF
C_{p0}	-	4.3 pF
C_p	-	0.082 pF
C_{n0}	-	2.32 pF
C_n	-	0.028 pF

* Typically implemented off-chip for high capacitance values, such as in [2] and [3].

Table 2. Comparison of simulation results

Performance	Without NCGFB	With NCGFB
Gain	32.2 dB	32.2 dB
Bandwidth	100 Hz	100 Hz
CMRR* @10 Hz	87.2 dB	87.2 dB
PSRR* @10 Hz	66.9 dB	66.9 dB
THD* @10 Hz for 1 mV_{pk-pk} input	-51.1 dB	-51.1 dB
Input-referred offset voltage* (root-mean-square)	0.945mV	0.945mV
Total input-referred voltage noise (noise bandwidth: 0.1 - 100 Hz)	2.72 μV	2.72 μV

* Results were obtained with 500 Monte Carlo simulation runs with process and mismatch variations using foundry-supplied device models.

Table 3. OTA simulation results

Performance	[13]	[19]	[9]	This Work
Output impedance at 100 Hz	-	-	2.9 GΩ	4.6 GΩ
Transconductance	33 pS	15-150 pS	25.9 pS	29.2 pS
Output-referred noise / integration range	160 μV_{rms} / 0.3-10 Hz	-	78 μV_{rms} / 0.01-100 Hz	74 μV_{rms} / 0.01-100 Hz
HD3 (of i_{out}, sinusoidal V_{in} = 80 mV_{p-p} at 19.5 Hz)	-	< 1% (THD)	-30.1 dB	-29.5 dB
CMRR mean / standard deviation (with mismatch*)	-	-	69 dB / 7.2 dB	85 dB / 6.6 dB
PSRR mean / standard deviation (with mismatch*)	-	-	56 dB / 6.5 dB	72 dB / 7.3 dB
Supply current	~100 nA	< 1 μA	168 nA[$]	686 nA[$]

* 100 Monte Carlo simulations with a load capacitance of 3 pF at 60 Hz.
[$] Includes supply currents for bias circuits.