Sinusoidal Signal Generation through Successive Integration

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***Abstract* — This paper introduces a sinusoidal signal generation technique using successive integration of a digital square wave. It utilizes operational transconductance amplifiers (OTAs) and capacitors to realize the required integrators. To provide an example, the technique has been implemented in 130 nm CMOS technology with a supply voltage of 1 V and a power consumption of 325 µW. In this design, the input square wave and the sinusoidal output signals are both at 10 MHz. The output signal THD is -51 dBc, and the SFDR is 51 dB at 200 mV_{P-P}.**

***Keywords* — Wave generators, sinusoidal generators, OTA-C, built-in testing.**

I. Introduction

The popularity of integrated systems-on-chips (SoCs) has increased the need for low-power integrated versions of several circuits that used to be on the board, or even existed within lab testbench equipment. Hence, sinusoidal signal generators are becoming more frequently used within diverse SoCs. Examples include built-in self-test and calibration of analog and mixed-signal circuits [1]-[7], RF front-end calibration and third-order intercept point (IIP3) enhancement [8]-[11], and biomedical diagnosis and prognosis devices [12]-[16]. These SoCs require sinusoidal signals that have low total harmonic distortion (THD), high spurious-free dynamic range (SFDR), and are generated with low power.

Previous works can be divided into digital and analog approaches. Digital approaches depend on the existence of a digital-to-analog converter (DAC) that repeats digital words producing the sinusoidal-like signal [17]-[23]. This approach requires the presence of a high-frequency digital clock, often incurs power consumption in the hundreds of milliwatts range, and typically generates spurs that are difficult to suppress. Analog approaches, on the other hand, have significantly lower power consumption and are more suitable for integration into SoCs as low-cost blocks [7], [14], [24]-[33]. However, current analog approaches rely on wide bandwidth of the active components and high values for passive components, leading to non-optimal power dissipations and large layout areas, respectively.

This paper presents a reliable and efficient method for generating sinusoidal signals. The technique, illustrated in Fig. 1, depends on the successive integration of a digital square wave using multiple transconductor-capacitor (G_m-C) integrators. The simplicity of the technique, along with the absence of feedback paths and the ease of implementation to suite various THD and SFDR requirements, make it a very good candidate for contemporary sinusoidal signal generation needs.

The paper is structured as follows: Section II introduces the proposed technique, and Section III describes its circuit design and implementation. Section IV discusses simulation results of the designed sinusoidal signal generator example, and compares these results with prior works. Section V contains a summary and conclusions.

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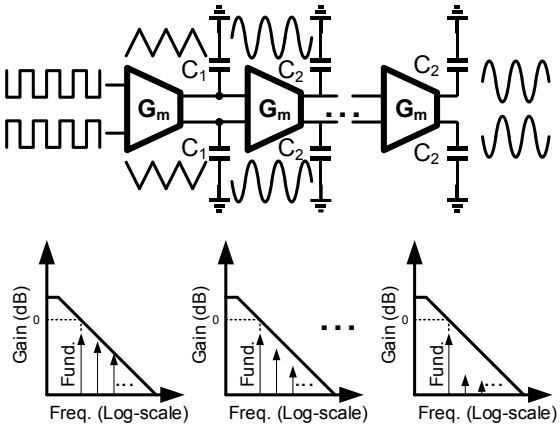


Fig. 1. Successive integration and attenuation of harmonics.

II. Proposed Sinusoidal Signal Generation Method

A. Mathematical foundation

The technique is based on Fourier Series of a differential square wave in eq. (1). According to [34]-[36], this signal can be efficiently generated with power consumption ranging from 5.8 µW to 20 µW, and area ranging from 16 μm^2 to 36 μm^2.

$$f(t) = \frac{4}{\pi} \cdot \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \cdot sin\left(\frac{n \cdot 2\pi \cdot t}{T}\right), \quad (1)$$

where $f(t)$ is the square wave as a function of time, and T is the square wave period. Using successive integration of $f(t)$, the high-order harmonics are reduced by a factor of $2n\pi/T$ every time the input signal is integrated, where n is the order of the harmonic. The third harmonic is $(4/\pi)\cdot(1/3)\cdot sin((3\cdot 2\cdot \pi \cdot t)/T)$, which is the harmonic experiencing the least suppression, and therefore can be taken as a baseline for the worst-case performance with the technique.

The first integration of equation (1) produces the following:

$$f(t) = \frac{-4 \cdot T}{2 \cdot \pi^2} \cdot \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n^2} \cdot cos\left(\frac{n \cdot 2\pi \cdot t}{T}\right), \quad (2)$$

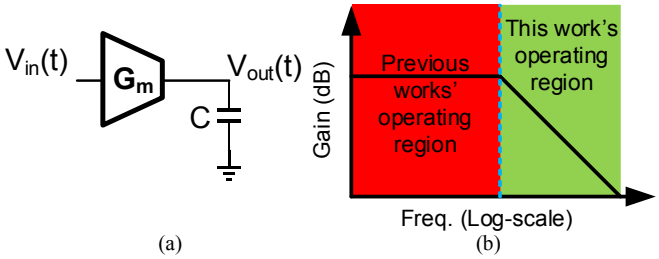


Fig. 2. Simple G_m-C integrator.

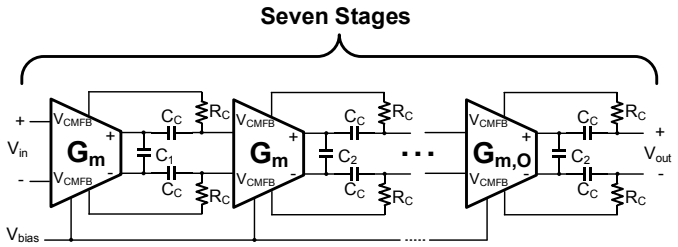


Fig. 3. Sinusoidal signal generator circuit.

The previous equation shows that after normalizing the $4 \cdot T/2 \cdot \pi^2$ factor, the fundamental tone maintains the same amplitude after the integration, while the third harmonic becomes $-(1/3)^2 \cdot \cos((3 \cdot 2 \cdot \pi \cdot t)/T)$, which has a three times lower amplitude (i.e., 9.5 dB reduction) compared to the input of the integrator. The fifth, seventh, and higher order components are attenuated five, seven, and n times every integration; or 14 dB, 17 dB, and $20 \cdot \log n$ dB. This process reduces the THD after every integration stage.

B. Implementation

The integration and associated suppression of harmonics can be realized by cascading multiple G_m-C stages, such as the one depicted in Fig. 2 (a). The transfer function of a simple G_m-C circuit is $G_m/(s \cdot C)$, which is an integrator with a gain of $G_m/(2 \cdot \pi \cdot f \cdot C)$. By designing the gain to be equal to one at the fundamental frequency, the approach described in Section II-A can be realized to reduce the THD level in each G_m-C integrator stage. As illustrated in Fig. 2 (b), one advantage of this implementation is that the OTA in each G_m-C stage operates beyond its 3-dB frequency. This enables low-power design by lowering the bandwidth requirement. In comparison, other G_m-C based implementations require wide bandwidths that are at least equal to the frequency of interest, which leads to higher power consumption.

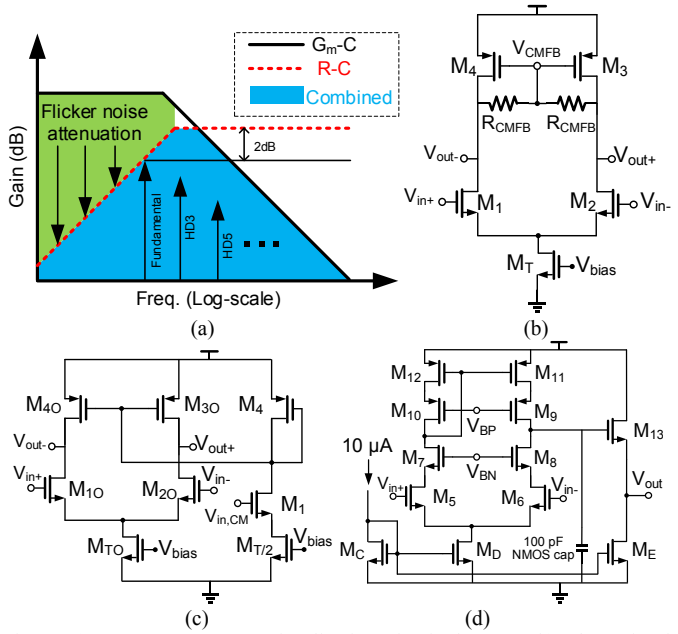


Fig. 4. (a) Frequency response visualization of a single stage, (b) schematic of the OTA in stages 1-6, (c) schematic of the OTA in stage 7, (d) schematic of the amplitude control loop OpAmp.

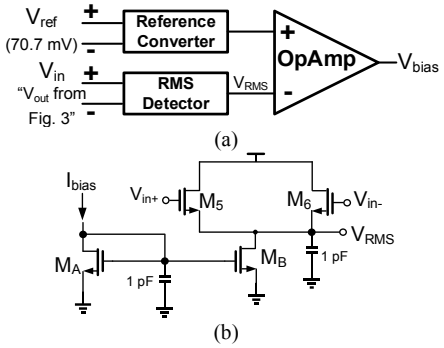


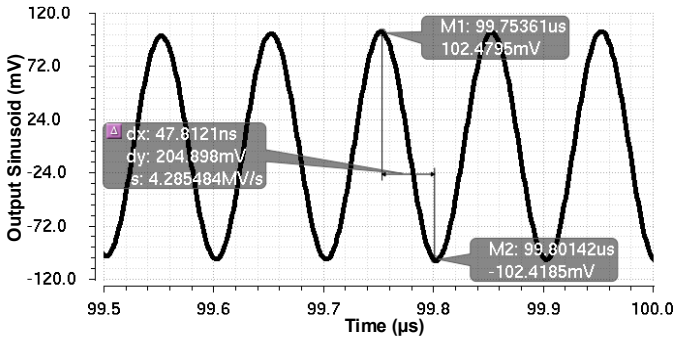
Fig. 5. (a) Amplitude control circuit, (b) RMS detector.

III. Circuit Design

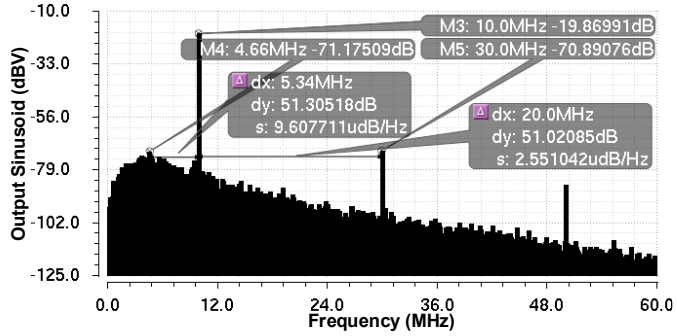
The example design in Fig. 3 is a 7-stage generator, where every stage is an integrator. The number of stages can be varied according to the required THD and power consumption. OTA non-linearities become the major contributor to THD with higher amplitude and an increasing number of stages. The output of every stage is AC-coupled to the following stage using an R-C network with a cutoff frequency three times lower than the frequency of interest. This prevents unwanted DC offsets and flicker noise from propagating to the following stages. As shown in Fig. 4 (a), the cutoff frequency is chosen high enough to suppress unwanted flicker noise, but low enough to avoid attenuating the fundamental tone. This reduces the rejection of third-order harmonic distortion (HD3) to about 7 dB per stage. The DC bias for the AC coupling comes from the common-mode feedback (CMFB) circuit of the previous stage to ensure linear operation of the devices across different corners. The gain of the first stage is designed to be less than unity by operating it beyond its slew rate to convert the fundamental tone amplitude from large rail-to-rail (i.e., from a reliable supply to ground) input clock signal to a 30 mV amplitude triangular wave for more linear operation in the subsequent stages.

Fig. 3 displays the circuit of the sinusoidal signal generator. The first G_m-C stage capacitor (C_1) value was selected to provide an attenuation of 20 dB to limit the first stage's output (a triangular-shaped wave) to 60 $mV_{P\text{-}P}$. The capacitors of the following G_m-C stages (C_2) were selected to obtain a gain of one at the fundamental tone frequency. It is important to take the attenuation of the fundamental tone due to AC-coupling into account when selecting the coupling capacitors (C_C). The values of C_1, C_2, C_C, and R_C, are 7 pF, 500 fF, 1 pF, and 50 kΩ respectively. The capacitors are metal-insulator-metal (MIM) capacitors consuming a total area of 0.018 mm^2, and the resistors are polysilicon resistors consuming less than 0.02 mm^2 total.

Fig. 4 (b) shows the OTA architecture for stages 1-6. It is a simple differential pair with resistive CMFB. It has a linear differential input range of 200 $mV_{P\text{-}P}$. This input range ensures linear operation for stages 2-6, thus limiting the impact of OTA non-linearities on the output SFDR. The tail transistor, M_T, passes a current of 27 µA. M_1 and M_2 have transconductances of 100 µA/V. R_{CMFB} is a polysilicon resistor of 25 kΩ. Fig. 4 (c) displays the output OTA architecture in the last stage. Its devices (M_{1O}-M_{4O}, M_{TO}), are five times larger than in the previous OTAs. It uses M_1,



(a)



(b)

Fig. 6. Simulated output signal with transient noise enabled: (a) vs. time, (b) spectrum.

M_4, and $M_{T/2}$ to bias its PMOS load; creating high output impedance while enabling high output swing. The tail transistor (M_{TO}) in the last stage passes 135 µA, such that M_{1O} and M_{2O} have a transconductance of 500 µA/V.

Fig. 5 (a) shows the amplitude control loop to adaptively generate the bias voltage (V_{bias}) for the OTAs [Fig. 4 (b), (c)]. It has an input differential reference voltage of 70.7 mV, which corresponds to the RMS value of the desired amplitude (100 mV). The reference voltage is generated by a polysilicon resistor ladder with total resistance of 100 KΩ, consuming 10 µA from 1 V supply voltage. Both, the sinusoidal output and the reference voltage, are applied to the root-mean-square (RMS) detector (reference converter) depicted in Fig. 5 (b). The RMS detector consumes 2.5 µA through its tail M_B. Its inputs and output are at the M_5-M_6 transistors' gates and common source respectively. The operational amplifier (OpAmp), shown in Fig. 4 (d), is a differential-input single-output telescopic cascode with NMOS inputs and PMOS load. It has a source-follower output stage that acts as a voltage level shifter.

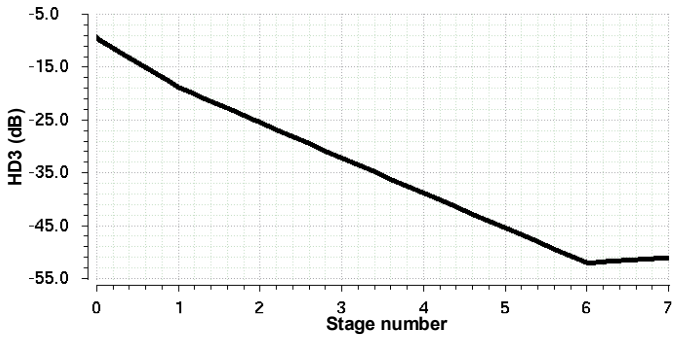


Fig. 7. Simulated HD3 at every stage.

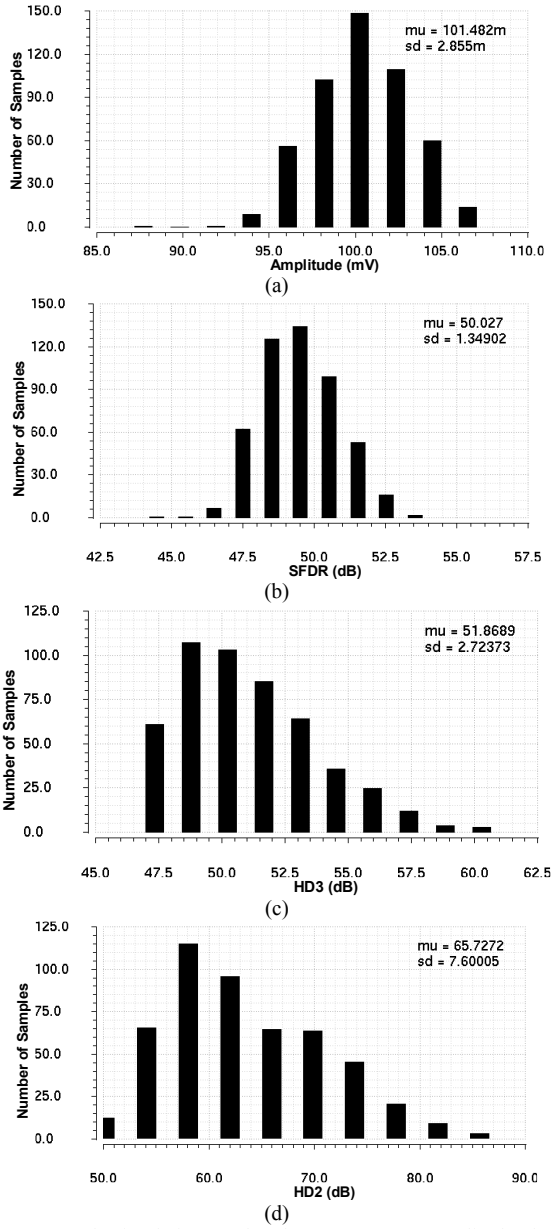


Fig. 8. Monte Carlo simulation results after 500 runs: (a) amplitude, (b) SFDR, (c) HD3, (d) HD2.

A 100 pF NMOS capacitor at the output of the OpAmp creates a dominant pole to stabilize the amplitude control loop.

IV. Simulation Results

Circuit-level schematic simulations were carried out with foundry-supplied device models from 130 nm CMOS technology using Cadence Spectre. An ideal square wave (without jitter) having rise and fall times of 10 ns was applied as an input, emulating a rail-to-rail digital signal swinging between ground and supply levels. The results from schematic simulations show close consistency with theoretical calculations.

Fig. 6 (a) displays transient simulation results of the output sinusoidal signal vs. time. Transient noise was enabled to examine its effect on the output. The simulated amplitude is 100

Table I. Performance comparison

	This Work	[24]	[26]	[22]	[25]	[23]	[14]	[7]	[27]	[28]	[29]	[30]	[31]	[32]	[37]	[12]	[13]	[38]	[39]
f_{out} (MHz)	10	10	10	18.7	25	1.56	2.048	1	41.4	1.12	2.5	2.048	1.11	10.7	0.02	0.09	0.1	0.02	5
Power (mW)	0.345*	4.04	20.1	174	1.58	8	15.3	23	N/A	0.355	N/A	5.1	3.24	132	0.06	2	N/A	0.05	2.79
V_{P-P}/V_{DD}	0.2	0.19	0.02	0.07	0.01	0.03	0.22	0.17	0.08	0.18	N/A	0.4	0.56	0.15	N/A	N/A	N/A	N/A	N/A
Area (mm^2)	0.1**	0.1	0.2	1.47	0.63	1.4	N/A	0.08	0.1	0.28	N/A	0.72	0.04	3.15	0.05	0.75	0.91	0.76	0.49
Technology (nm)	130	130	350	350	800	500	250	350	350	800	180	180	180	350	180	180	180	180	65
Supply (V)	1	1.2	3.3	3.3	2	2.7	2.5	3	3.3	1.8	3.3	1.8	1.8	3.3	1.2	1.2	1.8	2.2	1.2
FoM^1 (dB)	50.2	47.4	31.5	16.2	38.5	21	N/A	25.9	N/A	31.1	N/A	21	N/A	10.7	38.1	8.77	N/A	13.3	28.7
FoM^2 (dB)	40.2	40.1	24.5	17.9	36.5	22.5	24.2	15	N/A	25.6	N/A	19.6	N/A	15.7	25.2	7.52	N/A	12.1	25.6
THD (dBc)	-51	-72	-54.8	-55	-43.6	-42.1	-66	-72	-67	-41	-38.5	-43	-77	-53	-55.4	-41.8	-54	-32.8	-46
SFDR (dB)	51	72	54.8	55	48.8	59	65.7	57	67	41	50	47	N/A	53	59.1	41.8	54	32.8	46

* Power consumption after adding 20 µW of estimated power for the VCO based on [34], [35], and [36].
** Estimated area after adding 36 μm^2 of estimated area for the VCO based on [34], [35], and [36].

mV at 10 MHz. Fig. 6 (b) shows the spectrum of the output signal shown in Fig. 6 (a). A SFDR of 51.3 dB and HD3 of -51 dBc can be observed. The spectrum reveals that flicker noise is the main limiting factor of the SFDR.

Fig. 7 shows the simulated HD3 after each stage. It can be seen that the HD3 decreases by 7 dB per stage. After the sixth stage, the HD3 becomes limited by the non-linearities of the devices in the seventh stage due to its large output voltage swing.

Monte Carlo simulations were performed using statistical devices models supplied by the foundry. Fig. 8 displays Monte Carlo simulation results of the sinusoidal signal generator for 500 samples. These results were obtained from transient simulations with noise enabled, and with a correlation coefficient of 0.97 between matched devices; which implies the use of multiple fingers/subdevices with common-centroid matching for identical pairs of transistors and passive components in the layout [2]. Fig. 8 (a) illustrates that the output amplitude has a mean of 101.5 mV with a standard deviation of 2.9 mV. Without the amplitude control loop, the standard deviation is 30 mV. Fig. 8 (b) and Fig. 8 (c) indicate an expected mean SFDR and HD3 of 50 dB and 52 dBc respectively with standard deviations of 1.3 dB and 2.7 dB respectively. Fig. 8 (d) reveals an HD2 with a mean of 66 dBc and a variance of 7.6 dB. The HD2 variations result from mismatches of transistors, resistors and capacitors simulated with foundry-supplied statistical device models for the technology.

Table II summarizes simulation results for different corners with the amplitude control loop enabled. Transient simulations with noise enabled were used to obtain these results. HD3, HD2, amplitude, and SFDR exhibited acceptable variations. The amplitude, on the other hand, has significant variations across corners without the presented amplitude control loop. This emphasizes the importance of the amplitude control loop for the given circuit implementation. Furthermore, it was observed that the amplitude control loop reduces the unity-gain frequency changes across process-voltage-temperature variations (device model corner cases, -50 °C to 80°C, +/-5% supply voltage) from a range of 9-27 MHz down to a range of 10-15 MHz.

Fig. 9 shows the simulated amplitude control loop OpAmp output vs. time at start-up across corners. The loop settles without overshooting for slow-fast and slow-slow corners. There is minimal overshooting in the remaining corners, which ensures loop stability.

Table I presents a performance comparison with other works. The figures of merit are:

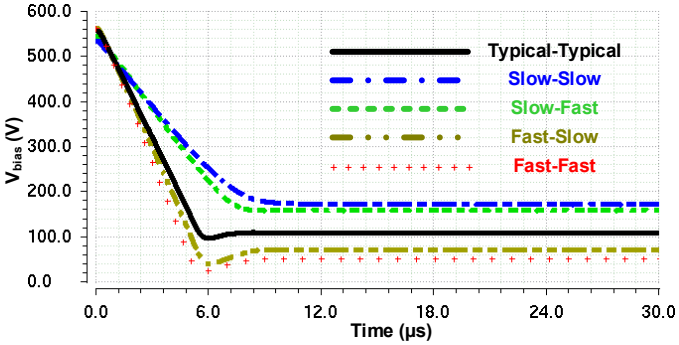


Fig. 9. Amplitude control start-up across corners.

$$FoM^1 = 10 \times \log\left(\frac{f_o(MHz) \cdot 2^{SFDR\,(dB)\,/\,6}}{Area\,(mm^2) \cdot power\,(mW)}\right)$$

$$FoM^2 = 10 \times \log\left(\frac{f_o(MHz) \cdot 2^{SFDR\,(dB)\,/\,6}}{power\,(mW)}\right)$$

FoM^1 is from [40] and reported in decibels. FoM^2 is FoM^1 without area, which was used for supplemental comparison because the presented design was not laid out. This work achieves FoMs that are significantly higher than most previous works. Note that the area was estimated by placing components in the layout editor, measuring the total occupied area, and multiplying it by 1.5 for possible routing overhead. Even after the oscillator overhead, the presented technique would still have a best-in-class FoM^1 of 50.2 dB and FoM^2 of 40.2 dB.

V. Conclusion

This paper described a sinusoidal signal generation technique using successive integration of a digital square wave. It utilizes basic OTAs and capacitors to realize the integrators. The technique was demonstrated with a design in standard 130 nm CMOS technology with a reduced supply voltage of 1 V and power consumption of 325 µW. The input square wave and the output sinusoidal signals are both at 10 MHz, resulting in a 200 mV_{P-P} sinusoidal output signal with a THD of -51 dBc and an SFDR of 51 dB.

Table II. Corners simulation results

	HD3	HD2	SFDR	Amplitude
Typical	-51.02 dBc	-76.55 dBc	51.02 dB	101.5 mV
Fast-Fast	-50.24 dBc	-81.61 dBc	50.24 dB	104.6 mV
Slow-Slow	-55.62 dBc	-75.1 dBc	52.85 dB	100.4 mV
Slow-Fast	-48.09 dBc	-77.22 dBc	48.09 dB	101.1 mV
Fast-Slow	-53.96 dBc	-76.11 dBc	50.08 dB	102.7 mV

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