Comparator Design and Calibration for Flash ADCs within Two-Step ADC Architectures

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***Abstract* — This paper describes a foreground offset calibration scheme for a 3-bit flash analog-to-digital converter (ADC), which is integrated as a coarse ADC within an 8-bit two-step time-interleaved (TI) hybrid ADC architecture. The calibration path emulates the ADC's normal operation to establish realistic loading and transient effects. Analog circuitry for input generation in the calibration path was designed to pass a specific reference for each comparator. A digital-to-analog converter (DAC) generates the calibration voltages. The presented design approach also addresses integration challenges within the hybrid ADC, such as kickback noise and common-mode variations. Simulation techniques were developed to assess the calibration effectiveness in the hybrid ADC system and to determine the standard deviations of the offsets. A prototype chip was fabricated in 130nm CMOS technology for experimental verification of the calibration method. Evaluations of operation with 6-bit resolution at 500MS/s and 10.28MHz input frequency demonstrate a measured ENOB of 5.24 bits after automatic calibration with 500MS/s and an ENOB of 4.93 bits using a 1GS/s clock.**

***Keywords* — Analog-to-digital converter (ADC), calibration, offset reduction, digitally assisted design, wide-swing amplifier.**

I. Introduction

Digitally-assisted integrated circuit design has gained popularity in recent years due to challenges associated with analog components in mixed-signal systems-on-a-chip (SOC) and miniaturization of transistors. These challenges include process variations, mismatches, and increased demand for circuit complexity for designs in sub-micron fabrication process technologies [1]. In flash ADCs, the offsets are typically random variables with normal distributions and have a direct impact on an ADC's performance, worsening its integral and differential nonlinearities (INL and DNL, respectively). On-chip calibration techniques aid to address these issues by reducing the sensitivity of analog circuit designs to variations.

Fig. 1 depicts the hybrid ADC diagram with the calibration circuitry. As in [2], a 3-bit high-speed (1GS/s) flash ADC is utilized as a coarse ADC to resolve 3 MSBs, while 4 time-interleaved channels of the comparator-based asynchronous binary search (CABS) ADC resolve the 5 LSBs. In this way the number of cycles of the CABS ADC is reduced, resulting in a faster overall conversion rate. For the calibration, an additional (fifth) channel emulates the hybrid ADC's normal operation; which includes input generation circuitry, a matching network at the ADC input, and a sample-and-hold and capacitive digital-to-analog converter (SHDAC). The latter samples the input voltage, delivers it to the flash, and shifts it to the optimal voltage range of the second stage based on flash decision. If allowing offset of ½ LSB for the flash ADC, which corresponds to 62.5mV for a $1V_{peak\text{-}to\text{-}peak}$ differential full scale input of a conventional 3-bit ADC, a shifting offset would result in serious performance degradation. Thus, the flash ADC should comply with the system's 8-bit offset requirement of 2mV instead of the conventional 3-bit requirement.

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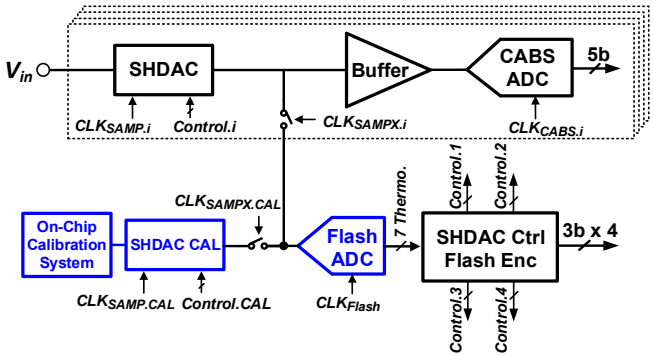


Fig. 1. Hybrid ADC architecture with embedded flash ADC and calibration.

II. Design Considerations for the Flash ADC and the Automatic Calibration Scheme

A. 3-bit flash ADC integration challenges

The flash ADC was designed as in [2], and includes seven strongARM comparators, which is depicted in Fig. 2. In the hybrid ADC system, kickback noise is caused by a large variation of internal voltages within the comparator, which are coupled by the gate-drain capacitance (C_{gd}) of the input transistors back to the input nodes (also called "differential kickback" [3]). In addition, a "common-mode kickback" is caused by the clocked gates of the tail transistors (M_{tail1} and M_{tail2} in Fig. 2) at the sources of the input pairs. The severity of the kickback depends on the impedance of the preceding circuit, which is finite and asymmetric. For example, the reference voltages of the comparators come from resistor reference ladder, while the

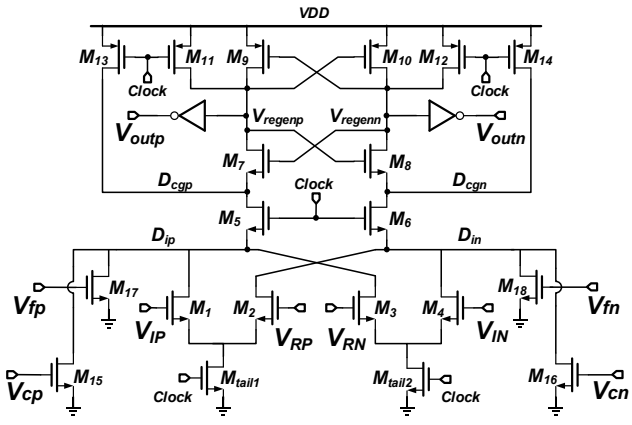
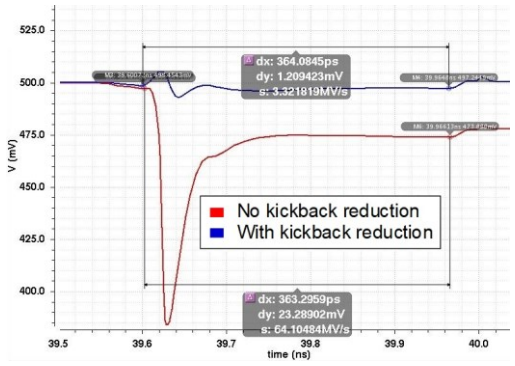
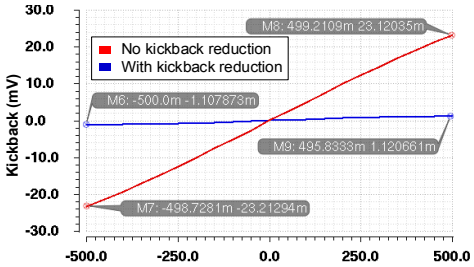


Fig. 2. Dynamic latched comparator with kickback reduction and offset compensation.



(a)



(b)

Fig. 3. Simulated (a) flash ADC input with and without kickback reduction (500mV input), (b) input voltage amplitude versus kickback.

inputs come from the switches connecting the flash ADC to the sample-and-hold circuit.

Fig. 3(a) shows the differential input waveform of the flash ADC inputs with and without kickback reduction nMOS switches M_5-M_6 (as in [4] and [5]) in the worst-case where the input voltage is equal to the peak value of 500mV. Fig. 3(b) displays the kickback errors at the input of the flash ADC versus input voltage amplitude from simulations with and without kickback reduction transistors. The worst-case voltage error from kickback is reduced from 23.2mV to 1.21mV.

Asymmetry in the hybrid ADC differential operation results in common-mode variations at flash input. Fig. 4 shows the simulated offset as a function of the common-mode voltage difference between the input and the reference of each comparator, which is added to the offsets caused by device mismatches. The range of the offset calibration system (Fig. 5) for the flash ADC is designed to be able to reduce this systematic offset in addition to the random (mismatch) offset.

B. Analog circuitry for input generation in the calibration path and wide-swing buffer

To automatically calibrate the seven comparators of the 3-bit flash ADC, an input that equals the specific reference of each comparator must pass through the same path as the regular signal, which ensures similar transient effects such as kickback and

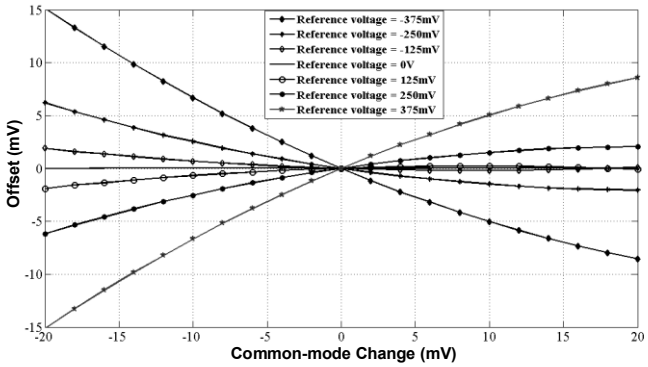


Fig. 4. Systematic offset versus input common-mode voltage variations.

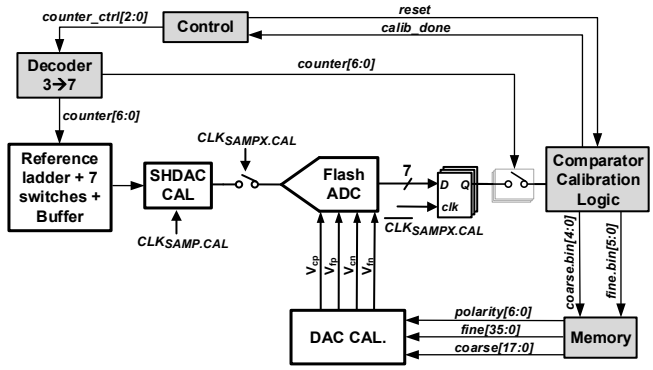


Fig. 5. Digital calibration scheme.

feedthrough. The detailed input generation circuitry from Fig. 5 is depicted in Fig. 6. The input is derived from a conventional ladder with polysilicon resistors. Two sets of seven transmission gate switches are controlled by the calibration logic for a proper input voltage connection. Each set passes the input signal to the two wide-swing operational amplifiers [6] with unity-gain configuration, which act as buffers. The rail-to-rail operational amplifier with single-ended output shown in Fig. 7 was designed. This topology enables a wide input common-mode range (from 225mV to 925mV in this case). This is achieved by two complementary differential pairs (nMOS and pMOS) connected in parallel. The nMOS pair (M_1-M_2) is mostly active for high input common-mode voltages, while the pMOS pair (M_3-M_4) is active for low input common-mode voltages. A folded cascode structure is formed by transistors M_{13}-M_{14} and M_{19}-M_{20}. Transistors M_{17}-M_{18} and M_{23}-M_{24} form a class-AB output stage to provide rail-to-rail swing. This is achievable with the complementary common-source connections in the output stage. Transistors M_{15}-M_{18} form floating current sources, whose purpose is to maintain a relatively constant voltage difference between the gates of M_{23} and M_{24}. The effective transconductance (g_m) depends on the instantaneous input common-mode level and is doubled around the middle of the range when both pairs are active. In [6], the current of the active pair is directed to a current mirror, then it is tripled and added to the current of that pair, yielding $4 \cdot I_D$, which provides $2 \cdot g_m$ when only one pair is active. For this work, the modified amplifier in Fig. 7 does not have g_m control because constant g_m is not required for the unity-gain configuration in the calibration path where it is used to pass DC voltages. From post-layout simulations, the amplifier gain is 49.9dB with phase margin of 46° at the 600mV common-mode level.

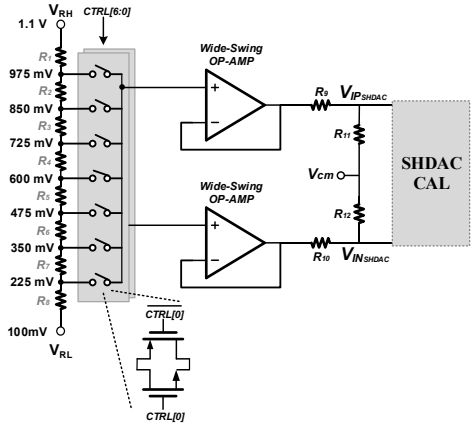


Fig. 6. Circuits at the input of the calibration path.

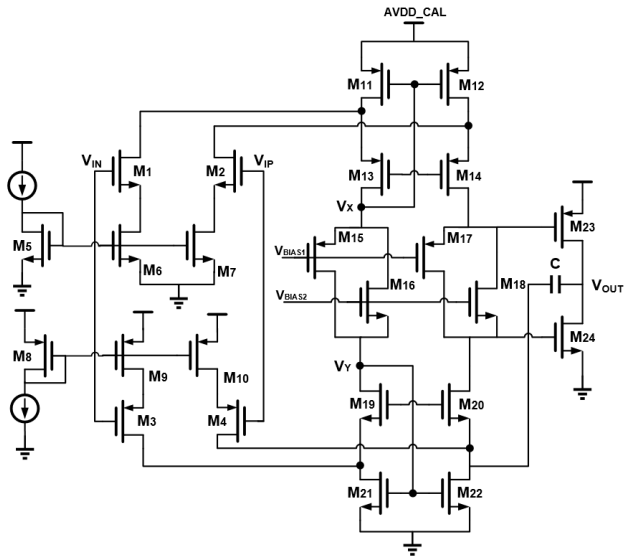


Fig. 7. Wide-swing operational amplifier schematic.

C. Calibration DAC

The calibration digital-to-analog converter (DAC) in Fig. 5 converts the digital code to gate control voltages. This DAC is depicted in Fig. 8. The shared resistor ladder consists of 35 p-type doped polysilicon resistors of 1.055kΩ with width of 4µm and length of 12µm each. Its ladder generates 36 reference levels between 500mV and 1.2V with steps of 20mV. A polarity bit determines which branch receives the voltage level, and which branch remains at 500mV. The DAC layout occupies approximately 500µm × 500µm.

D. Memory block

The memory block (Fig. 9) stores all codes of the calibration logic for the seven comparators, and directly controls the switches. The memory supports external writing of manual codes, as well as reading of either manual or automatic calibrated codes. To reduce the number of the chip package pins, the external decoder and encoder were designed to convert data of 6 bits for fine adjustments and 6 bits for coarse adjustments (5 bits) plus polarity (1 bit). A 3-bit pin address_ext[2:0] represents the comparator number, such that 001 corresponds to the comparator with the lowest differential reference. The 1-bit pin address_ext[3] determines if the written or read code is a coarse (with polarity) or a fine code. The bi-directional analog multiplexer (MUX) either writes to memory (when RW_mux = '1') or reads from memory (RW_mux = '0'). Hence, the reading and writing operations are performed from the same pin, which avoids six additional external pins.

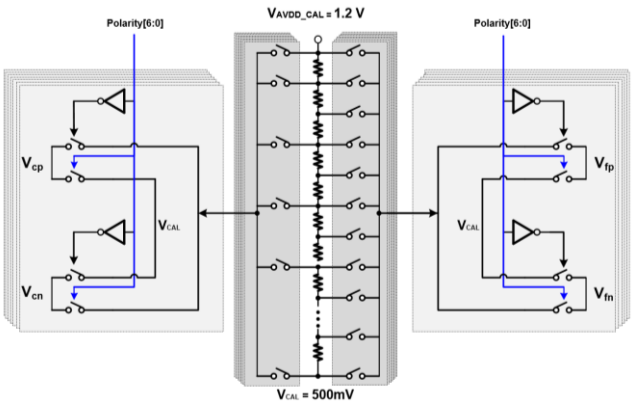


Fig. 8. Calibration DAC diagram.

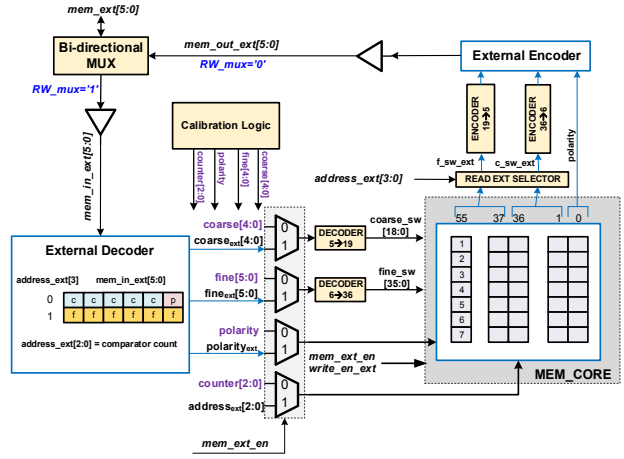


Fig. 9. Memory block and digital components of the on-chip calibration system.

III. Offset Determination within the Hybrid ADC

Simulating the calibration within the complete hybrid ADC system level has two main advantages. First, the loading effects of the other six comparators on the single calibrated comparator are taken into consideration together with the preceding switches and SHDAC, as well as with the realistic input generation path that changes the common-mode level. Second, the offset standard deviations within the system are expected to be different than that of a single comparator. Therefore, to obtain a more realistic evaluation of the comparator's standard deviations, Monte Carlo (MC) simulations should be run on the system level. To avoid excessively slow simulations, the DAC and calibration logic were implemented with Verilog-A modules, while the other circuits and components were simulated on the transistor level. The simulation setup is visualized in Fig. 10, and its timing diagram is displayed in Fig. 11. Each comparator is connected to the Verilog-A module for the calibration. To further reduce the simulation time, a binary search was used for offset determination. This allows to determine the offset within 11 clock cycles. The testbench determines the offsets of all seven comparators numerically before calibration, then performs the calibration procedure serially, and determines the offsets again after calibration. Since the calibration code modifies the comparator operation, which is coupled to the flash input as kickback, the calibration codes of other comparators can be modified or affected. For this reason, the calibration procedure is executed for three cycles, where the most significant expected change is from cycle 1 to cycle 2. Considering that the simulation with transient noise impacts the offset determination, the offset was evaluated five times to obtain an average. From 100 MC simulations within the system, the offset standard deviations before calibration were 18.01mV, 10.98mV, 8.61mV, 8.11mV, 9.29mV, 11.09mV,

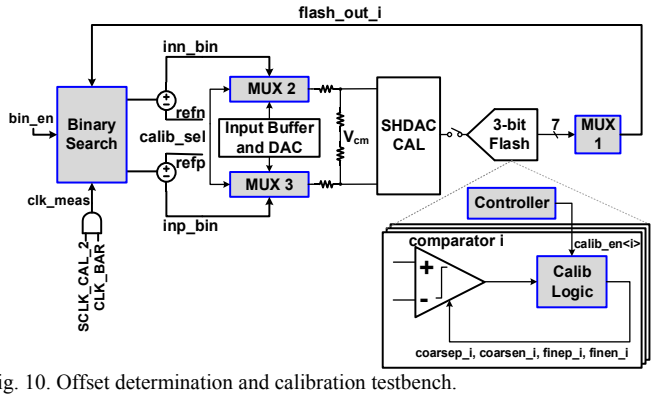


Fig. 10. Offset determination and calibration testbench.

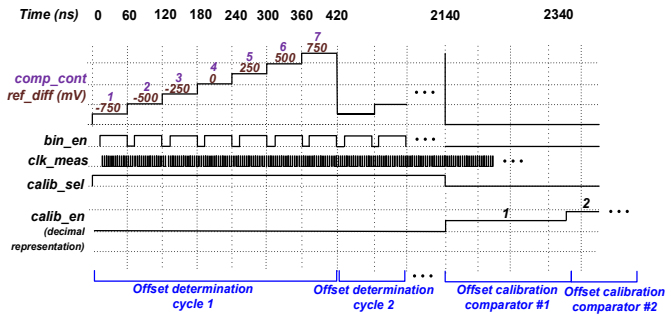


Fig.11. Timing diagram for the offset determination simulation.

and 19.19mV. After calibration, these offsets reduced to 1.05mV, 741µV, 527µV, 447µV, 363µV, 593µV, and 582µV, respectively.

IV. Measurement Results

A prototype chip with a 3-bit flash ADC and calibration circuitry within an 8-bit hybrid two-step ADC was designed and fabricated in a 130nm CMOS technology. Measurement results of the hybrid ADC are compared with the state-of-the-art in [7]. The flash ADC and calibration system performance were evaluated by recording the digital data of the four channels via low-voltage differential signaling (LVDS) outputs and a logic analyzer before and after calibration. The data was afterwards processed in MATLAB to obtain spectra or INL/DNL. Fig. 12 displays the micrograph of the chip. For automatic calibration, a clock signal of 500MHz was applied with a calibration clock of 1MHz. A clock frequency reduction was used because of a loss of calibration effectiveness with a 1GS/s clock, where the comparators connected to the largest differential reference voltages experienced discrepancies. Both the fine and coarse codes reached their maximum values, which resulted in clipping of the reconstructed output due to insufficient comparator offset tuning range. The fast clock is routed 577µm further down to the clock generation of the four normal operation channels than to the clock generation of the calibration channel. Since the clock generation delay blocks were optimized for the hybrid ADC core, the timing difference between the flash clock, which is the same for both cases, and the generated sampling clock for the calibration SHDAC causes a problem. As a consequence, the SHDAC for calibration path is sampled too early, which was alleviated by reducing the clock frequency.

Fig. 13 displays the output spectra of the 500MS/s 6-bit hybrid ADC testing (taking the 6 MSB of the 8-bit output) from captured data with f_{in} = 10.28MHz before and after calibration. Full scale sinusoidal input signals were used. The calibration improved the ENOB from 3.64 bits to 5.24 bits. With a higher sampling rate of 1GS/s using the same codes (calibration performed with 500MS/s), the ENOB is 4.93 bits. The result with 1GS/s is worse because the automatic calibration was performed for 500MS/s, which is associated with different transient and memory effects affected by clock frequency. The result with 500MS/s after automatic calibration is 0.33 bits lower than that with manual calibration [7]. This is because the quality of the automatic calibration has dependence on the input provided to the flash ADC during calibration. If the references of the resistor ladder for input generation are not optimized correctly, an error that translates to offset in the system causes the logic to yield a non-optimal code. Fig. 14 displays the measured INL and DNL before and after automatic calibration. Prior to calibration, the DNL and INL values were within -1/+3.175 LSB and -2.65/+2.374 LSB, respectively. After automatic calibration, the DNL and INL values are within -0.653/+1.175 LSB and -0.854/+1.141 LSB. In comparison, note that manual flash ADC offset calibration resulted in DNL and INL errors within -0.41/+0.50 LSB and -0.77/+0.52 LSB [7], leading to

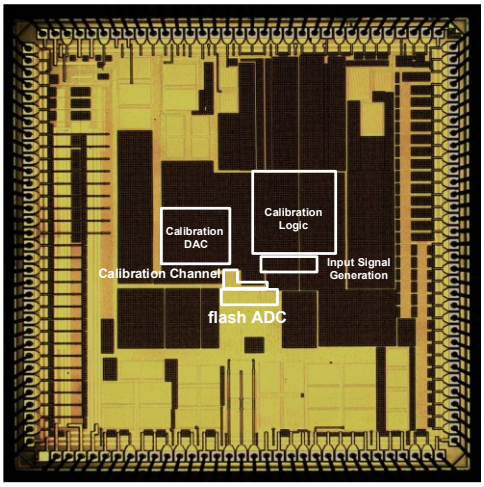


Fig. 12. Micrograph of the hybrid ADC chip with flash ADC and calibration logic.

slightly higher ENOB and SFDR values. The results suggest that it would be advisable to include one additional bit of resolution for the calibration DAC when implementing this scheme in practice.

V. Conclusion

Design and simulation details for an offset calibration scheme within a hybrid ADC architecture were presented. This automatic calibration was verified for the first time with a fabricated 130nm CMOS prototype chip. Measurements of a 6-bit equivalent 500MS/s ADC resulted in an ENOB of 5.24 bits after automatic calibration. Although manual calibration achieves slightly better performance, the automatic calibration is more practical and can be improved by increasing the number of tuning bits for enhanced resolution. For future implementations, it is advisable to use equal distance for the layout of the clock generation paths of the ADC core and for the calibration circuitry, or to insert a capacitance in the faster path to achieve equal delays.

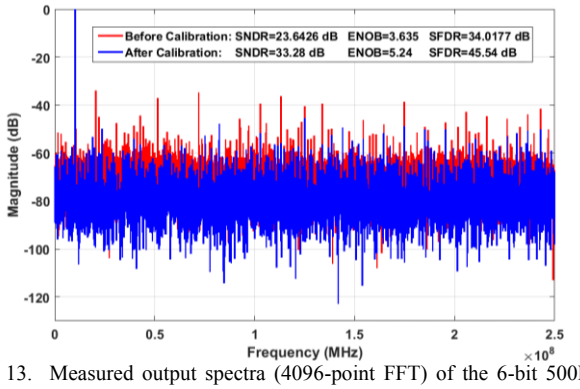


Fig. 13. Measured output spectra (4096-point FFT) of the 6-bit 500MS/s hybrid ADC output for f_{in} = 10.28MHz before and after automatic calibration.

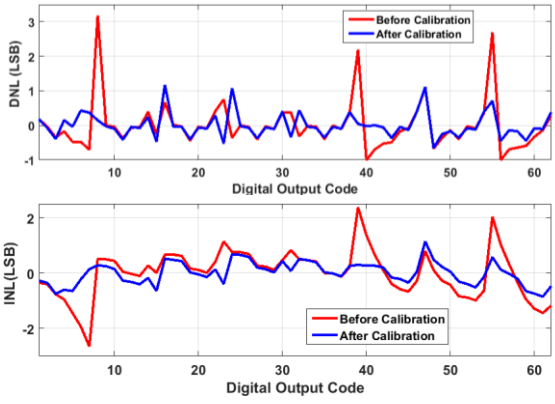


Fig. 14. Measured DNL and INL of the hybrid ADC (6-bit evaluation) before and after calibration.

REFERENCES

[1] M. Onabajo and J. Silva-Martinez, *Analog Circuit Design for Process VariationResilient Systems-on-a-Chip*. New York, NY: Springer, 2012.

[2] S. A. Zahrai, M. Zlochisti, N. Le Dortz, and M. Onabajo, "A low-power high-speed hybrid ADC with merged sample-and-hold and DAC functions for efficient subranging time-interleaved operation," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3193-3206, Nov. 2017.

[3] Y. Huang, H. Schleifer, and D. Killat, "Design and analysis of novel dynamic latched comparator with reduced kickback noise for high-speed ADCs," in *Proc. European Conference on Circuit Theory and Design (ECCTD)*, 2013.

[4] T. Sundstrom and A. Alvandpour, "A kick-back reduced comparator for a 4-6-bit 3-GS/s flash ADC in a 90 nm CMOS process," in *Proc. Intl. Conf. Mixed Design Integr. Circuits Syst.*, Aug. 2007, pp. 195–198.

[5] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.

[6] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505-1513, Dec 1994

[7] S. A. Zahrai, M. Zlochisti, N. Le Dortz, and M. Onabajo, "Design considerations and experimental verification of a 10.5mW 1GS/s hybrid ADC for portable wireless devices," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2018.