A Transmitter Architecture for Wireless Medical Devices in the MICS Band

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***Abstract* — This paper introduces a 401-457 MHz BFSK transmitter (TX) architecture that utilizes mixing and image rejection techniques to generate the two carrier frequencies for BFSK transmission. The proposed architecture enables low power consumption for a wide range of data rates by avoiding fast settling time requirements for the frequency-locked loop. Simulations indicate that the TX designed in 130nm CMOS technology can achieve data rates up to 10 Mbps with a power consumption of 140 µW or lower from a 0.6 V supply. Its estimated energy efficiency is 14 pJ/b while delivering -19.7 dBm of output power.**

Keywords —Transmitter, low-power radio frequency circuit design, MICS, wireless medical devices.

I. Introduction

Portable wireless medical devices are instrumental for monitoring of vital signs and the treatment of chronic diseases. There are two approaches to power such devices: they can use a battery that requires replacement, or they can be powered by energy harvesting from an external source. A problem arises when the device must operate continuously to send data for alerts about abnormal conditions. This creates the need for low-power transmitters that are able to send data at any time.

Over the years, the Federal Communications Commission (FCC) has facilitated the deployment of wireless medical devices by providing frequency bands through the medical implant communication service (MICS) and the medical device radiocommunications service (MedRadio) [1]. MedRadio includes a range of frequencies from 401 MHz to 457 MHz, as listed in TABLE I. This range has the benefit of low power consumption due to relatively low transmission frequencies, which has been exploited in several published works. Literature review shows that there are two main approaches to generate the output frequencies for ultra-low power transmitters [2]-[7]: injection-locked oscillators [2], [4], [5], [7]; and all-digital frequency-locked loops (ADFLL) [3], [6]. The modulations used in these transceivers are simple such as binary frequency shift keying (BFSK) [5]-[7], binary phase shift keying (BPSK) [2], on/off keying (OOK) [4], minimum shift keying (MSK) [3], and quadrature phase shift keying (QPSK) [7]. Data rates have a wide range starting from 120 Kbps [3] up to 20 Mbps [2].

TABLE I. MICS Bands

Start (MHz)	End (MHz)	Channel Width (MHz)
401	401.85	0.1
401.85	402	0.15
402	405	0.3
405	406	0.1
413	419	6
426	432	6
438	444	6
451	457	6

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Recent efforts in our group focused on low-power receiver circuit design [8]-[9]. On the other hand, this paper introduces the low-power BFSK MICS transmitter architecture shown in Fig. 1. One of the most power-hungry blocks in a frequency shift keying (FSK) transmitter is the frequency-locked loop (FLL), whose power is inversely proportional to its settling time [6], [10]-[12]. Reduced settling time is required to achieve higher data rates, which implies higher power consumption. The presented architecture alleviates the need for fast FLL settling time by realizing mixing and image rejection techniques to quickly switch between two frequencies without changing the frequencies of the frequency generators in Fig. 1. Thus, a low-power FLL can be used in this transmitter architecture. Since the maximum data rate of BFSK is directly proportional to the switching speed between the two frequencies, the data rate of this architecture is theoretically limited by the channel bandwidth and does not depend on the setting time of the FLL. This allows to achieve low overall transmitter power consumption.

This paper is structured as follows: Section II describes the proposed transmitter architecture using frequency mixing to generate the required transmission signals. Section III contains circuit design descriptions for each block. Simulation results are provided in Section IV, and Section V contains concluding remarks regarding the design method and results.

II. Proposed Transmitter Architecture

A. System architecture and analysis

The proposed system architecture is displayed in Fig. 1. This transmitter utilizes BFSK modulation for its simplicity, which allows reducing power consumption by using mixing for the generation of the two output frequencies instead of using a high-speed FLL to switch between two frequencies. As visualized in Fig. 2, the transmission involves the processing of signals with two fundamental frequencies that remain constant throughout the operation: The high frequency (ω_H) for signal transmission can

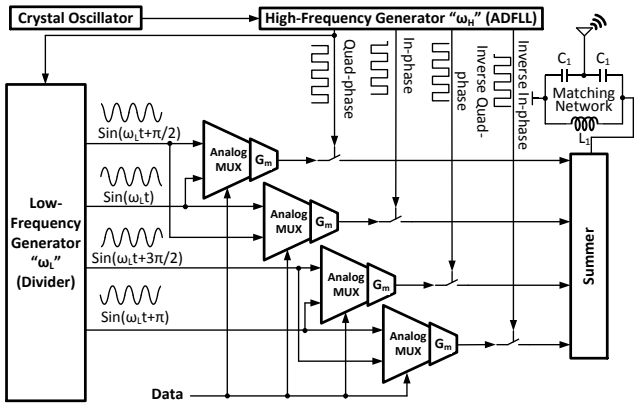

Fig. 1. System-level transmitter diagram.

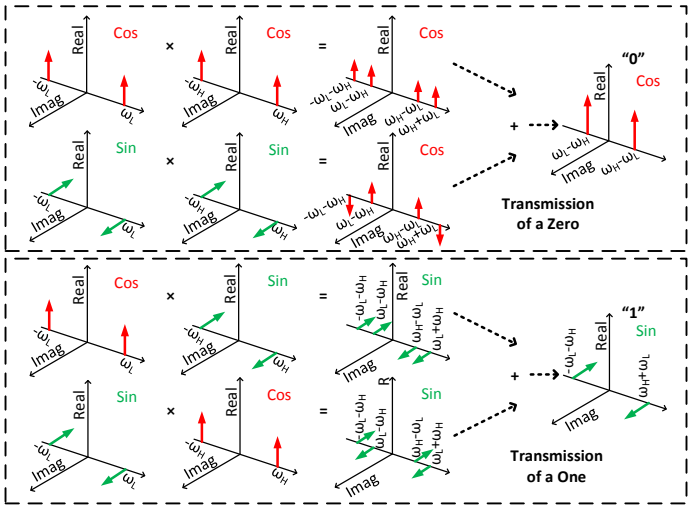

Fig. 2. Transmission frequency generation scheme.

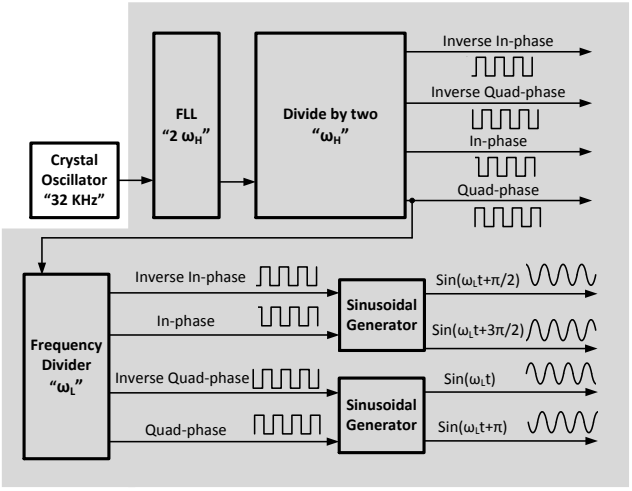

Fig. 3. Signal generation approach.

vary according to the utilized channel from 401 MHz to 457 MHz; and the baseband frequency (ω_L), which equals the bandwidth of the channel divided by two, can vary from 50 KHz to 3 MHz according to TABLE I. Fig. 2 graphically illustrates the mixing process within the architecture in Fig. 1, which is captured by the following equations with ideal sinusoids (i.e., representing the fundamental tones of the mixed signals) for simplicity:

- To generate the first frequency (corresponding to "0" data):

$$V_{out} = \sin(\omega_L \cdot t) \times \sin(\omega_H \cdot t) + \cos(\omega_L \cdot t) \times \cos(\omega_H \cdot t)$$

$$\therefore V_{out} = K \cdot \cos((\omega_H - \omega_L) \cdot t) + \cdots$$

$$\therefore F_{out} = \frac{\omega_H - \omega_L}{2 \cdot \pi} = F_1$$

- To generate the second frequency (corresponding to "1" data):

$$V_{out} = \sin(\omega_L \cdot t) \times \cos(\omega_H \cdot t) + \cos(\omega_L \cdot t) \times \sin(\omega_H \cdot t)$$

$$\therefore V_{out} = K \cdot \sin((\omega_H + \omega_L) \cdot t) + \cdots$$

$$\therefore F_{out} = \frac{\omega_H + \omega_L}{2 \cdot \pi} = F_2$$

Note that all frequency mixing products outside the band of interest were dropped from the above equations since the components are suppressed by the band-pass matching network, as can be observed from the simulation results in Section IV. Furthermore, the constant K in the above equations is the combination of the mathematical expressions as well as the gains in the transconductance stage (G_m), summing stage, and matching network in Fig. 1. Each analog multiplexer (MUX) is comprised of PMOS switches that have negligible impact on the gain during the selection of the low-frequency signals.

Since ω_H is a rail-to-rail digital signal (i.e., a square wave) generated by an ADFLL, which is applied to switches for up-conversion of the sinusoid having a frequency of ω_L, the output of the summer in Fig. 1 contains harmonics at multiples of ω_H. These harmonics are suppressed by the filtering in the matching network. However, our preliminary assessments revealed that the low-frequency signal at ω_L should be a sinusoidal-like signal to avoid harmonics located at frequencies that are separated from ω_H by multiples of ω_L, which could fall into the passband of the matching network.

B. Signal generation and system operation aspects

Fig. 3 illustrates the signal generation components. It is assumed that the FLL has an off-chip crystal oscillator with a frequency of 32 KHz as reference. Since the proposed architecture does not necessitate variable frequencies during data transmissions, the FLL can have relaxed locking time. Frequency changes are only required when the channel is changed. The FLL frequency is divided by two to generate the in-phase and quad-phase square waves at ω_H. The signal at ω_L is produced by a frequency divider ($\omega_H \div 400$ in this example) to obtain the in-phase and quad-phase square wave signals, from which the sinusoidal waveforms with an amplitude of 50 mV are generated.

As shown in Fig. 1, the low-frequency generator output voltages are fed to transconductors (G_m) to convert them to currents that are easier to sum at high frequency compared to voltages. These currents are up-converted to the transmission band by the switches serving as mixers. All currents are then summed and converted to a voltage that is applied to the antenna (50 Ω load) by the power amplifier within the summer block. The digital data fed to the analog MUXs decides how the tones are mixed to produce ($\omega_H + \omega_L$) as logic "1" or ($\omega_H - \omega_L$) as logic "0".

C. System-level simulation

System level simulations with ideal behavioral blocks were first carried out to evaluate the proposed transmitter architecture. Fig. 4 shows the output spectrum of the system in Fig. 1 for repetitive transmission of a logic "1" with a 405 MHz ADFLL output and a 1 MHz sinusoid. It can be observed that the output tone is shifted by 1 MHz relative to the frequency of the high-frequency generator output, as expected. It can also be

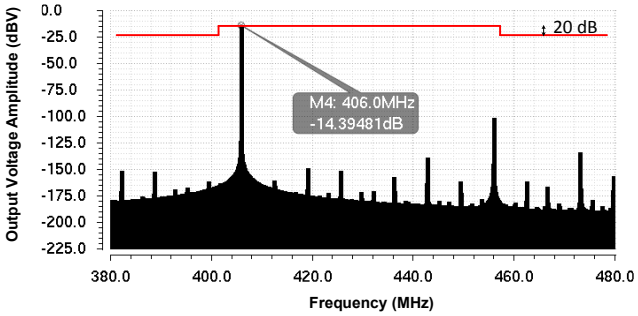

Fig. 4. System-level mask compliance from a behavioral simulation.

seen in Fig. 4 that all resulting undesired harmonics are at least 85 dB below carrier. This is well in compliance with the FCC regulation, which requires the out-of-band harmonics to be at least -20 dB with respect to the transmitted signal at 406 MHz.

III. Design of the Transmitter Circuits

All circuits of the blocks in Fig. 1 except for the ADFLL and the digital divider (Fig. 3) were designed using GlobalFoundries 130nm CMOS technology. Ideal square wave generators (pulse sources) were used for simulations instead of the ADFLL and divider. A well-designed low-power ADFLL can consume 100 µW for an output frequency around 2.4 GHz [10]-[12]. Hence, for power estimation, we assume a maximum ADFLL and divider power of 30 µW for a design with a lower output frequency in the 802-914 MHz range (= $2\cdot\omega_H$ for in-phase/quad-phase output generation at ω_H).

A. Sinusoidal signal generator

The sinusoidal signal generator provides the 50 mV $\sin(\omega_L\cdot t)$ signal with four equally-spaced phases. This block is composed of in-phase and quad-phase paths, each containing two low-power operational transconductance amplifiers (OTAs) with capacitors at the outputs as depicted in Fig. 5. The OTA configurations act as cascaded integrators. The integration of the first stage results in triangular signals and that of the second stage results in a second-order polynomial. This polynomial can be approximated as a sinusoidal signal with harmonics. Potential OTAs have been reported with power consumptions in the 7-9.4 µW range [9], [13]. The folded cascode OTA design used in this prototype transmitter has a simulated power consumption of 4.9 µW from a 0.6 V supply, such that the sinusoidal signal generator's power is 19.6 µW. The OTA has a low-frequency gain of 49 dB, a unity-gain frequency of 1.8 MHz, and a third-order harmonic distortion (HD3) of -40.9 dB with a 250 mV_{P-P} sinusoidal input. With digital rail-to-rail inputs to the first stage of the signal generator in Fig. 5, the simulated 50 mV sinusoidal outputs of the second stage have a second-order harmonic distortion (HD2) of -49.4 dB and an HD3 of -52.7 dB.

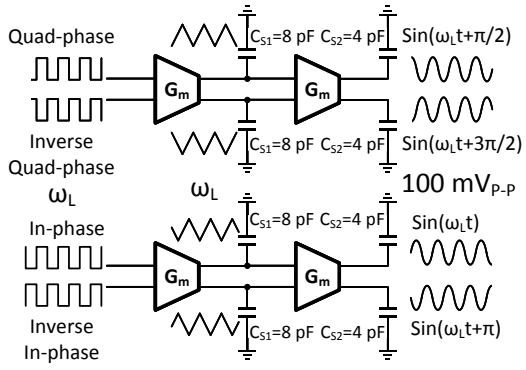

Fig. 5. Sinusoidal signal generator with OTAs (G_m blocks).

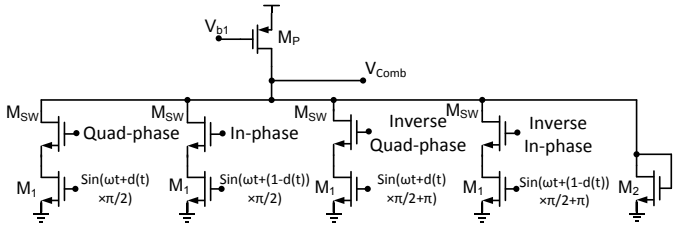

Fig. 6. Combined analog MUX, G_m-stage, and summer; where d(t) in the sinusoids depends on the digital data applied to the MUXs in Fig. 1.

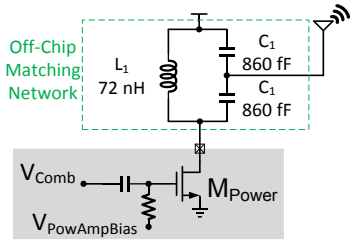

Fig. 7. Power amplifier.

B. Combined analog MUX, G_m-stage, and summer

Fig. 6 shows the schematic of the stage that converts the sinusoidal signals to currents (G_m-stage in Fig. 1), up-converts them to the transmission band via switching, sums the resulting currents, and then converts these current into a voltage using a diode-connected transistor (M_2). The transistors labeled as M_1 act as the G_m-stage. Their gates are AC-coupled to the sinusoidal signal generator with 1 pF capacitors, and the DC gate bias voltage is provided through 500 KΩ PMOS pseudo-resistors consisting of PMOS transistors (as used for the instrumentation amplifier in [14]) to save area. Transistor M_P serves as a bias current source. The switches (M_{SW}) are directly controlled by the digital signal (levels with reduced supply: 0 V and 0.6 V) with a fundamental frequency of ω_H for the up-conversion process described in Section II. Transistor M_2 is biased in the subthreshold region to increase its effective resistance ($\approx 1/g_{m2}$) for enhanced voltage swing at the output (V_{comb}). The simulated power consumption of the block in Fig. 6 is 54 µW from a 0.6 V supply.

C. Power amplifier

The power amplifier (PA) in Fig. 7 receives the summed input (V_{comb}), and drives the antenna (modeled with a 50 Ω resistance) using class AB biasing and AC-coupling at its input. The off-chip matching network component values were selected to maximize the power transfer to the antenna. This network also acts as filter for the attenuation of higher-order mixing byproducts at multiples of ω_H by 29 dB at $2\cdot\omega_H$, 35 dB at $3\cdot\omega_H$, and 39 dB at $4\cdot\omega_H$. The PA consumes 36 µW according to simulations.

IV. Simulation Results

Simulations of the circuits described in Section III were carried out using ideal ω_H and ω_L square waveforms (after the dividers in Fig. 3) in Cadence with foundry-supplied device models for GlobalFoundries 130nm CMOS technology. The effects of package, bonding wires and pad parasitics were taken into consideration by including the model in Fig. 8 for a typical QFN package at the output. Fig. 9 shows the output voltage spectrum at the antenna for the cases of transmitting a "1" (a) and a "0" (b). The spectra are compliant with the MICS mask specified by FCC. The total power consumption of the simulated analog circuits is 110 µWatt from a 0.6 Volt supply. As elaborated in the first paragraph of Section III, an estimated digital power of 30 µW is assumed for the FLL and divider. TABLE II shows a comparison of the presented architecture with the state of the art. The simulation results are an indicator for the potential of the design approach, but some performance degradation can be expected after a complete implementation, particularly in comparison to other works with test chip

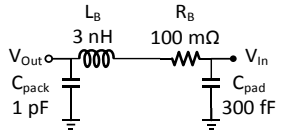

Fig. 8. Package and pad parasitics.

TABLE II. Transmitter performance comparison

Parameter	This Work	[2]	[3]	[4]	[5]	[6]	[7]
Power (µWatt)	<140 ***	330	350	160	90	332.6	4060/4080
Data Rate (Mbps)	1 (max.: 10)	20	0.12	1	0.2	2	0.55/11
Transmit Power (dBm)	-19.7	-15	N/A	-17	-17	N/A	-13
Supply Voltage (V)	0.6 (analog) 1.2 (digital)	0.8, and 0.2*	N/A	0.6, and 1	1	1, and 0.6**	1
Process	0.13 µm CMOS	0.18 µm CMOS	90 nm CMOS	90 nm CMOS	0.13 µm CMOS	90 nm CMOS	0.13 µm CMOS
Modulation	BFSK	BPSK	MSK	OOK	BFSK	BFSK	BFSK/QPSK
Carrier Generator	ADFLL	injection-locked	DCO	injection-locked	injection-locked	ADFLL	injection-locked
FoM (nJ/bit)	< 0.14 (min.: 0.014)	0.0149	2.9	0.16	0.45	0.1663	7.42/0.37

* PA supply. **DCO supply. *** Simulated: sinusoidal signal generator (19.6 µW); combined analog MUX, G_m-stage, and summer (54 µW); and power amplifier (36 µW). Estimated: 30µW for FLL and divider.

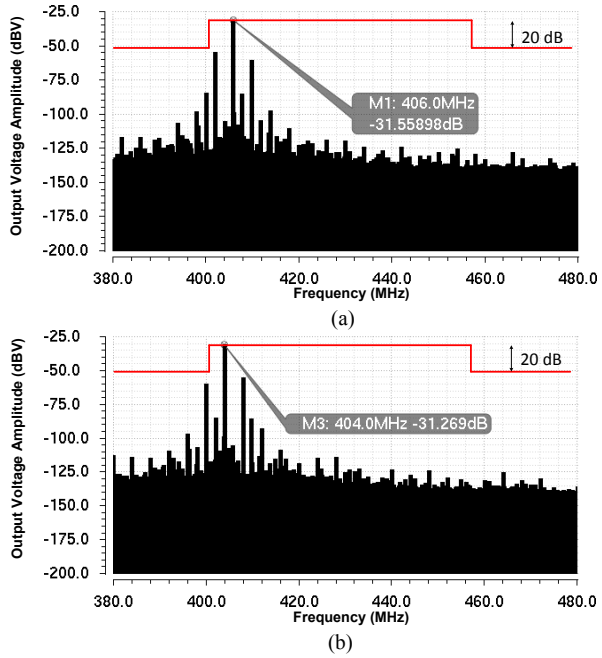

Fig. 9. Output spectra with 1 Mbps: (a) logic "1" symbol, (b) logic "0" symbol.

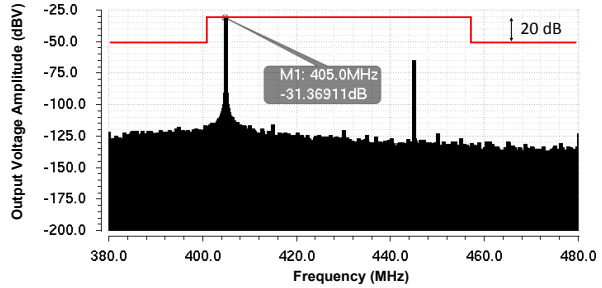

Fig. 10. Output spectrum with 10 Mbps: logic "0" symbol.

measurements. This transmitter has a promising Figure of Merit (FoM) of 0.14 nJ/bit with 1 Mbps data rate. Even though 10 Mbps is not a typical data rate, it was also simulated with 10 MHz low-frequency input and 415 MHz high-frequency signal for up-conversion to assess its high-speed capability. Fig. 10 shows the output spectrum from a simulation with consecutive logic "0" transmissions. The corresponding FoM is 0.014 nJ/bit.

V. Conclusion

This paper described a 401-457 MHz BFSK MICS transmitter (TX) architecture with built-in frequency translation and image rejection for the generation of the two data-dependent output frequencies. The architecture does not rely on a fast frequency-locked loop for the switching of the output frequency during data transmissions, which leads to low power consumption even with relatively high data rate. Simulations have shown that the TX achieves BFSK data rates up to 10 Mbps with an estimated power consumption up to 140 µW. Designed in 130nm CMOS technology, the prototype TX achieves an energy efficiency of 14 pJ/bit (with a maximum data rate of 10 Mbps) while delivering -19.7 dBm of output power with a 50 Ω load and modeled package parasitics.

VI. References

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