A Low-Power RF Receiver Front-End Chip Designed with Methods to Reduce Third-Order Intermodulation Distortion

Chun-hsiang Chang, Li Xu, Marvin Onabajo
Dept. of Electrical and Computer Engineering
Northeastern University, Boston, MA, USA
monabajo@ece.neu.edu

***Abstract* — This paper describes a linearized RF front-end design consisting of a subthreshold pseudo-differential common-source cascode low-noise amplifier (LNA) and a subthreshold active mixer. The applied linearization mechanisms can improve the third-order intermodulation intercept point (IIP3) without additional power consumption by using only passive components, which implies that the techniques do not require auxiliary amplifiers to suppress third-order distortion components. A 1.95 GHz RF receiver front-end was designed and fabricated in 110nm CMOS technology. Measurement results show that the linearized low-power front-end has a 20.6 dB voltage gain, a 9.5 dB double-sideband noise figure, and a -10.8 dBm IIP3 with a power consumption of 0.9 mW.**

***Index Terms* — Subthreshold LNA, subthreshold mixer, linearization, low-power RF design, RF front-end.**

I. Introduction

Diverse low-power wireless standards and circuit design approaches have been developed for low-rate wireless personal area network (WPAN) and wireless body area network (WBAN) communication [1]-[5]. Their range of applications spans health and fitness monitoring, wireless sensor nodes, automated payments, and smart home applications. The associated standards include IEEE 802.15.4, IEEE 802.15.6, Bluetooth low energy (BLE), Near Field Communication (NFC), and Global Positioning System (GPS).

Transistors operated in the subthreshold (or weak inversion) region offer opportunities to minimize power consumption in low-power CMOS RF front-end circuits. Over the past years, some of such LNAs and mixers were reported with very low power consumptions [5]-[8], which were made possible by high transconductance-to-drain current ratios (g_m/I_D) and low power supply voltages (V_{DD}). However, the prevalent design challenge associated with subthreshold RF front-end circuits has been linearity degradation. For example, in earlier published subthreshold LNAs and mixers [5]-[8], the third-order intermodulation intercept point (IIP3) is typically below -10 dBm. The key distinguishing characteristics of subthreshold biasing compared to strong inversion biasing are stated below to summarize our prior simulation-based works [9]-[11].

1) Higher power efficiency: transistors biased in subthreshold can provide a higher g_m/I_D ratio than those biased in strong inversion. Furthermore, the drain-to-source voltage (V_{DS}) can be lower, which permits the use of lower power supply voltages at the expense of slightly higher noise figure.

2) The change of the contribution and increase of parasitic capacitances: In subthreshold mode of operation, the gate-to-source capacitance (C_{gs}) no longer dominates, implying that the gate-to-drain capacitance (C_{gd}) and the gate-to-bulk capacitance (C_{gb}) have to be taken into account for more sophisticated design. Moreover, to achieve similar transconductance gains as in strong inversion it is required to increase the transistor widths, which results in higher parasitic capacitances and lower transition frequency (f_T).

3) Linearity degradation due to highly positive g_3/g_1, where $g_1 = g_m$ and g_3 is the third-order nonlinearity coefficient: The sign of g_3 transitions from negative to positive when the transistor biasing changes from strong inversion to subthreshold. In addition, the value of g_3/g_1 strongly depends on the g_m/I_D ratio in the subthreshold region.

In this paper, measurement results are presented for the combination of the subthreshold LNA simulated in [9] and the mixer simulated in [10], demonstrating the feasibility of the proposed design approach. The organization of this paper is as follows: The linearity improvement methods for the subthreshold LNA and mixer are briefly introduced in Section II. Prototype chip measurement results are summarized in Section III, and conclusions are provided in Section IV.

II. Linearity Enhancement Techniques

Fig. 1 displays the schematic of the RF front-end with LNA (consisting of transistors M_1-M_4) and mixer (consisting of transistors M_5-M_{10}). The extra passive components (inductors L_{g2}, L_1, L_2 and capacitor C_{gd2_ext}, C_c) improve the

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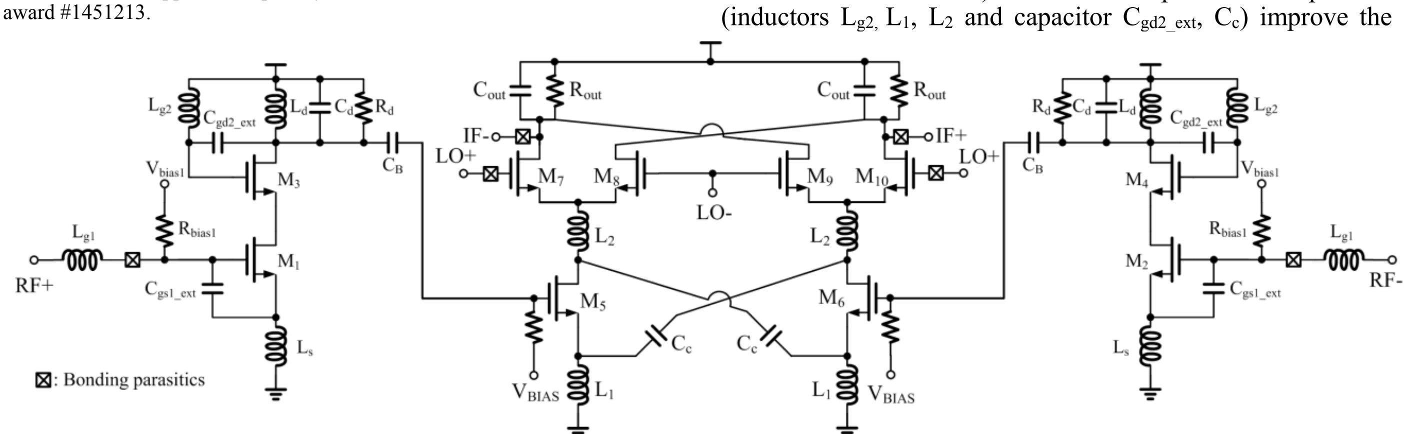

Fig. 1. Schematic of the linearized subthreshold RF front-end circuit with pseudo-differential LNA and mixer.

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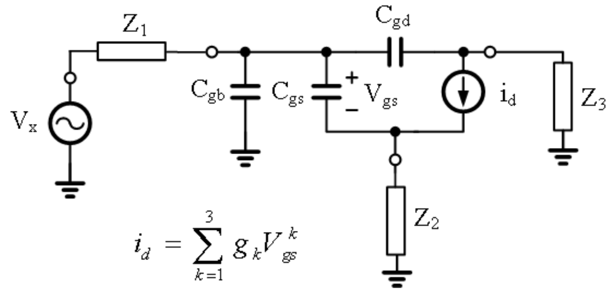


Fig. 2. Nonlinear small-signal model of a common-source amplifier.

IIP3 as explained next. Fig. 2 depicts the nonlinear small-signal model of the LNA input stage with three terminal impedances: Z_1, Z_2, and Z_3 signify the impedances when looking out from the gate, source and drain of the transistor, respectively. The IIP3 of the input stage can be derived with Volterra series analysis [12], [13] as

$$IIP3 = \frac{1}{6R_s \cdot |H(\omega)| \cdot |A(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|}\ , \tag{1}$$

where ω is the center frequency of the two intermodulation tones at ω_{RF1} and ω_{RF2}, $\Delta\omega$ is defined as $|\omega_{RF1} - \omega_{RF2}|$, and R_s is the antenna impedance of 50Ω. H(ω) is the third-order nonlinearity transfer function from V_{in} to the drain-source current (i_d) of the transistor (M_1), A(ω) is the linear transfer function from the input voltage (V_x) to the gate-to-source voltage (V_{gs}), and ε(Δω,2ω) represents the nonlinear contribution from the second-order and third-order terms of the transistor in the input stage. Minimization of ε(Δω,2ω)| in (1) leads to improved IIP3. Note that this approach cancels third-order intermodulation distortion under the impact of the second-order contribution, which does not necessarily imply that second-order intermodulation distortion is simultaneously canceled. The ε(Δω,2ω) term of M_1 can be expressed as

$$\varepsilon(\Delta\omega, 2\omega) = g_3 - g_{oB}\ , \tag{2}$$

where:

$$g_{oB} = \frac{2}{3} g_2^2 \left[\frac{2}{g_1 + g(\Delta\omega)} + \frac{1}{g_1 + g(2\omega)} \right], \tag{3}$$

$$g(\omega) = \frac{\begin{array}{l} 1 + j\omega C_{gd} \cdot [Z_1(\omega) + Z_3(\omega)] \\ + j\omega C_{gs} \cdot [Z_1(\omega) + Z_2(\omega)] \\ + j\omega C_{gb} \cdot [1 + j\omega C_{gd} Z_3(\omega)] \cdot Z_1(\omega) \end{array}}{Z(\omega)}, \tag{4}$$

$$\begin{array}{l} Z(\omega) = Z_2(\omega) + j\omega C_{gb}[1 + j\omega C_{gd} Z_3(\omega)] Z_1(\omega) Z_2(\omega) \\ + j\omega C_{gd}[Z_1(\omega)Z_2(\omega) + Z_1(\omega)Z_3(\omega) + Z_2(\omega)Z_3(\omega)] \end{array}. \tag{5}$$

For the input stage of the LNA, Z_1-Z_3 can be expressed as

$$Z_{1,LNA}(\omega) = R_s + j\omega L_{g1}, \tag{6}$$

$$Z_{2,LNA}(\omega) = j\omega L_s, \tag{7}$$

$$Z_{3,LNA}(\omega) = \frac{\begin{array}{l} 1 + j\omega C_{gd3} Z_3(\omega) \\ + [j\omega C_{gs3} + j\omega C_{gd3} - \omega^2 C_{gs3} C_{gd3} Z_d(\omega)] \cdot Z_{22}(\omega) \end{array}}{\begin{array}{l} g_{1,M2} + j\omega C_{gs2} \\ + [j\omega C_{gd3} g_{1,M3} - \omega^2 C_{gd3} C_{gs3}] \cdot [Z_{22}(\omega) + Z_d(\omega)] \end{array}}\ , \tag{8}$$

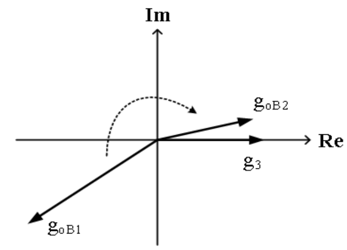


Fig. 3. Vector diagram of the third-order intermodulation cancellation, where g_{oB1} and g_{oB2} are g_{oB} realizations in (2) with different design parameters.

where the combined impedances are $Z_{22}(\omega) = (j\omega L_{g2}) // (j\omega C_{gb3})^{-1}$ and $Z_d(\omega) = R_d // (j\omega L_d) // (j\omega C_d)^{-1}$.

For the input stage of the mixer, Z_1-Z_3 can be expressed as

$$Z_{1,mixer}(\omega) = (1/(R_s/2) + j\omega C_{gb5})^{-1}, \tag{11}$$

$$Z_{2,mixer}(\omega) = (1/(j\omega L_1) + j\omega C_c(1 + K(j\omega)))^{-1}, \tag{12}$$

$$Z_{3,mixer}(\omega) = (1/(Z_{M3}) + j\omega C_c(1 + 1/K(j\omega)))^{-1}. \tag{13}$$

where: $Z_{M3}(\omega) = j\omega L_2 + \dfrac{1}{g_{m7} + j\omega_{RF}(C_{gs7} + C_{gs8})}$.

As described in in [9] and [10], the impedances Z_1, Z_2 and Z_3 of the LNA and mixer input stages can be designed to minimize |ε(Δω,2ω)|. Fig. 3 visualizes that the mechanism of the partial third-order intermodulation cancellation in (2) entails changing the magnitude and phase of g_{oB} in (3) such that they are almost identical to those of g_3, where g_{oB2} represents a better design point (with more cancellation of g_3) than g_{oB1} as result of different parameters. We have proposed this design approach in our previous works together with theoretical analyses and simulation results. The next section introduces first proof-of-concept measurement results from an RF front-end that combines the LNA and mixer architectures from [9] and [10].

III. Measurement Results

A low-power linearized RF receiver front-end (Fig. 1) was designed using subthreshold biasing, and fabricated in Dongbu 0.11μm CMOS technology with an RF frequency of 1.95 GHz (second tone in the two-tone tests at 1.948 GHz) and an LO frequency of 1.96 GHz. Table I lists the important parameters of the LNA and mixer designs. Fig. 4 visualizes the test setup for the RF front-end, which consumes 1.5 mA of current from a 0.6 V power supply instead of the nominal 1.2 V supply voltage in 0.11μm CMOS technology. Fig. 5 displays the chip micrograph of the pseudo-differential LNA and mixer with a total area of 1.5 mm × 1.1 mm. The die was bonded to a conventional QFN24 package.

Fig. 6 shows the measured IIP3 performance of the front-end, and the output spectrum from a test with a two-tone input signal having a power of -36.5 dBm. Fig. 7 shows the plot of output power measurements from a power level sweep of a single 10 MHz tone to determine the 1-dB compression point (P_{1dB}) of the front-end. The IIP3 and P_{1dB} of the subthreshold RF front-end are -10.8 dBm and -22.7 dBm, respectively. After de-embedding the effects of the losses (9.5dB) due to the loading at the output, the overall voltage gain of the front-end

$$K(\omega) = \frac{v_d(\omega)}{v_s(\omega)} = \frac{g_{m5}(j\omega C_{gd5} - 2j\omega C_c - \frac{1}{j\omega L_1}) + \frac{C_{gd5}}{L_1} - \omega^2 (C_{gs5}C_{gd5} + C_{gd5}C_c - C_{gs5}C_c)}{g_{m5}(j\omega C_{gd5} + 2j\omega C_c + \frac{1}{Z_{M3}}) + \frac{j\omega C_{gs5}}{Z_{M3}} - \omega^2 (C_{gs5}C_{gd5} + C_{gs5}C_c - C_{gd5}C_c)}\ , \tag{14}$$

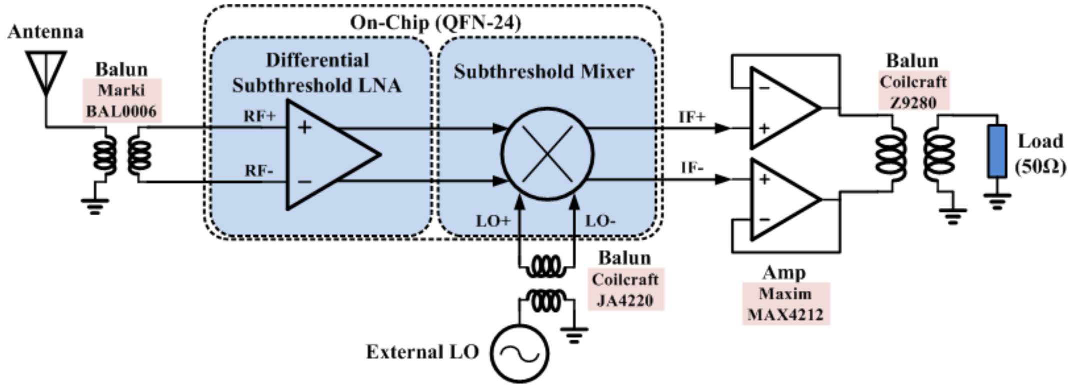


Fig. 4. Diagram of the RF front-end measurement setup.

TABLE I. DESIGN PARAMETERS OF THE RF FRONT-END CIRCUITS

LNA	
V_{DD}	0.6 V
I_D	875 µA
L_{g1}	6.2 nH
L_{g2}	3.5 nH
L_s	2.4 nH
C_{gs1_ext}	130 fF
C_{gd2_ext}	150 fF
L_d	6.4 nH
C_d	88 fF
R_d	720 Ω
W/L per finger ($M_{1,2,3,4}$)	6µm / 0.13µm
Number of fingers ($M_{1,2,3,4}$)	64
Mixer	
V_{DD}	0.6 V
I_D	625 µA
L_1	2.7 nH
L_2	5.8 nH
C_c	337 fF
C_{out}	1178 fF
R_d	1 KΩ
W/L per finger ($M_{5,6}$)	6µm / 0.13µm
Number of fingers ($M_{5,6}$)	64
W/L per finger ($M_{7,8,9,10}$)	5.8µm / 0.13µm
Number of fingers ($M_{7,8,9,10}$)	64

based on the measured transient output voltage in Fig. 8 is 20.6 dB. Fig. 9 displays the plot of the measured double-side band noise figure (NF_{DSB}) that is 14 dB at 10 MHz with the input balun. After de-embedding the effect of the input balun loss (5.5 dB), the double side band noise figure of the RF front-end is 9.5 dB at 10 MHz.

Table II summarizes the performance of low-power narrowband RF front-ends with operating frequencies ranging from 1.95 GHz to 5.1 GHz. The presented design exhibits a combination of high linearity with low power consumption and adequate noise figure. However, the relatively high number of inductors in the presented design creates a layout area trade-off. The pseudo-differential LNA stage in this work has the benefit of creating robustness to phase shift imbalances. On the other hand, the designs in [14]-[16] include single-ended LNAs, which saves power.

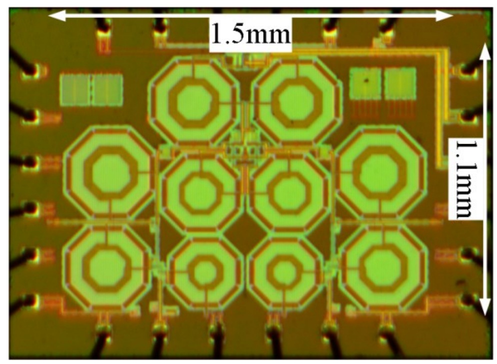
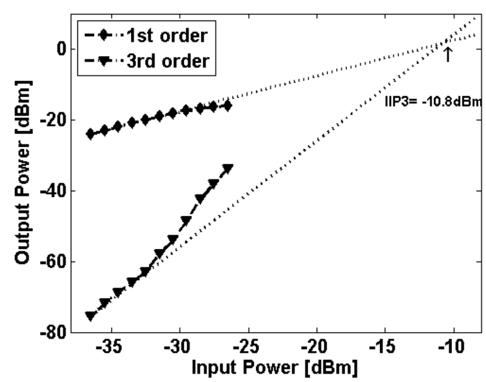
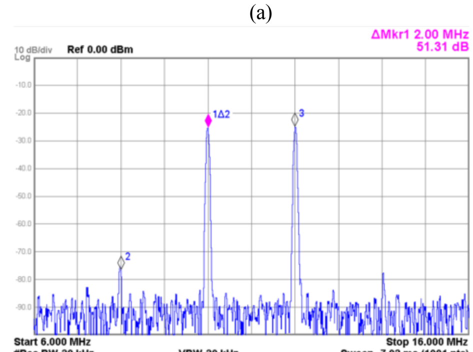


Fig. 5. Chip micrograph of the fabricated linearized subthreshold RF front-end in 0.11µm COMS technology.



(a)



(b)

Fig. 6. (a) Measured IIP3 of the RF front-end with output balun and amplifier (9.5 dB loss), (b) output spectrum from a test with two tones at 10 MHz and 12 MHz and an input power of -36.5 dBm.

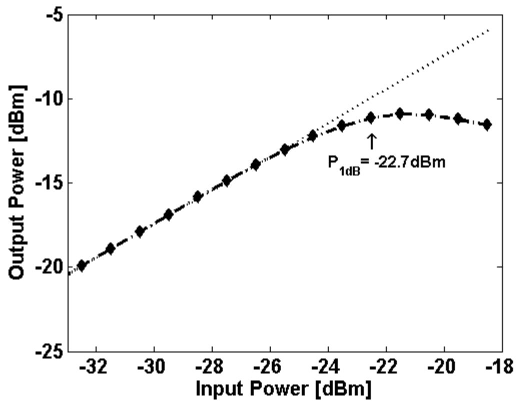


Fig. 7. Measured 1-dB compression point of the RF front-end with input and output baluns (at IF = 10 MHz).

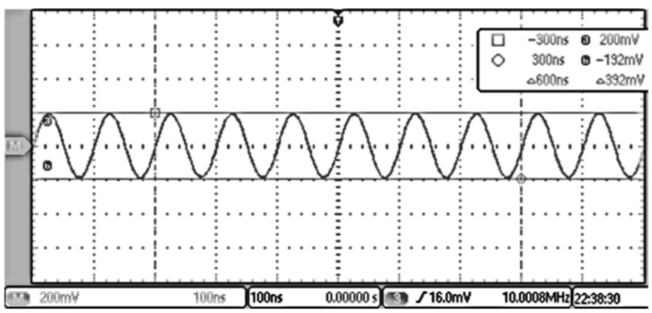


Fig. 8. Measured output waveform before the output balun.

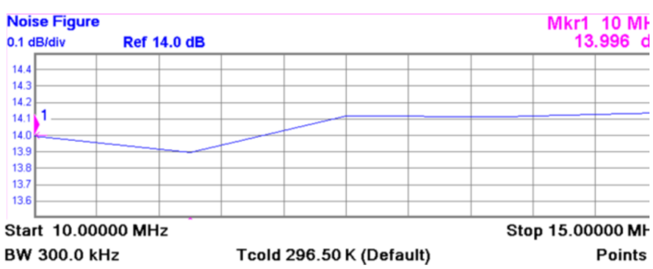


Fig. 9. Double-sideband noise figure (at IF = 10 MHz) measured with the input balun (5.5 dB loss).

TABLE II. COMPARISON OF LOW-POWER RF FRONT-ENDS

	THIS WORK	[14]*#	[15]#	[16]#	[17]	[18]
f_{RF} [GHz]	1.95	5.1	2.4	2.445	2.4	2.4
f_{IF} [MHz]	10	10	2	10	2	2
P_{LO} [dBm]	-9	-5	n/a	n/a	n/a	n/a
S11 [dB]	-20	n/a	-17	n/a	<-16	-9
Gain [dB]	20.6	27	20.5	30	55.5	32
NF_{DSB} [dB]	9.5	16	10.2	7.5	15.1	8.8
IIP3 [dBm]	-10.8 (IB)	-3 (IB)	-7.8 (IB)	-16.2 (IB)	-15.8 (OOB)	-7 (OOB)
P_{1dB} [dBm]	-22.7	n/a	-20	-26	n/a	n/a
P_{DC} [mW]	0.9	1	1.08	4.68	0.6	1.4
Tech. [nm]	110	180	180	90	130	65
Area [mm^2]	1.65$	0.856‡	1.69‡	0.74$	0.25$	0.14$

* passive mixer # single-ended LNA $ without pads ‡ with pads
IB = in-band OOB = out-of-band

IV. CONCLUSION

A 1.95 GHz subthreshold RF receiver front-end with an LNA and an active mixer was designed, fabricated and tested in 0.11μm CMOS technology to demonstrate recently proposed linearization methods with chip measurements. The applied linearization techniques involve extra passive components to accomplish partial cancellation of third-order nonlinearity products. Measurements of the RF front-end resulted in an IIP3 of -10.8 dBm, a voltage gain of 20.6 dB, and a double-sideband noise figure of 9.5 dB with a power consumption of 0.9 mW.

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