Design Considerations and Experimental Verification of a 10.5mW 1GS/s Hybrid ADC for Portable Wireless Devices

Seyed Alireza Zahrai*, Marina Zlochisti*, Nicolas Le Dortz+, Marvin Onabajo*
*Department of Electrical and Computer Engineering, Northeastern University, Boston, USA
+Analog Devices, Cambridge, USA
szahrai@ece.neu.edu, zlochisti.m@husky.neu.edu, nicolas.ledortz@analog.com, monabajo@ece.neu.edu

***Abstract* — A low-power 1GS/s hybrid analog-to-digital converter (ADC) for portable wireless applications is described. The first stage of the subranging architecture contains a 3-bit flash ADC with offset calibration. Its second stage employs a 5-bit 4-channel time-interleaved (TI) comparator-based asynchronous binary search (CABS) ADC. A merged sample-and-hold and capacitive digital-to-analog converter (SHDAC) samples the input, and generates the residue voltage for the subranging operation in each channel. The error on the residue voltage from the parasitic capacitances is cancelled through a linearity correction method. Design considerations of the amplifier in the unity-gain buffer and bandwidth mismatches between TI channels are studied and exemplified with simulation results. A prototype ADC chip was fabricated in 130nm CMOS technology for experimental verification of the concepts. Evaluations of operation with 6-bit resolution at 1GS/s demonstrate a measured ENOB above 5.26 up to the Nyquist frequency with a power consumption of 10.5mW from a 1.2V supply.**

***Keywords* — Analog-to-digital converter (ADC), time-interleaved, subranging, sample-and-hold, amplifier.**

I. INTRODUCTION

High sampling-rate (1-3 GS/s) ADCs with medium resolutions (6-10 bits) are utilized in various applications, such as wireless communication systems [1]-[2]. Lowering the power consumption of such wideband ADCs will make it feasible to employ them in a broader range of demanding portable applications. This work advances the concept of subranging and time-interleaved (TI) operation by realizing a hybrid flash-TI-CABS ADC architecture. Fig. 1 displays the proposed hybrid ADC architecture and its timing diagram. A 3-bit 1GS/s flash ADC is employed as the coarse ADC to resolve the most significant bits (MSBs), whereas four time-interleaved 5-bit 250MS/s CABS ADCs in the second stage resolve the least significant bits (LSBs). The fast MSB conversion by the flash ADC, together with the use of high-speed CABS ADCs in a TI structure, help to reduce the number of interleaved channels, which results in higher input bandwidth.

A merged sample-and-hold and capacitive digital-to-analog converter (SHDAC) was designed to perform the sampling and residue generation for the subranging operation [3]. The ideal SHDAC transfer function is shown in Fig. 2 ($V_{FS} = 1V_{p\text{-}p}$), where the green area indicates the operating region of the CABS ADC. The CABS ADC is power efficient at high speed due to the asynchronous operation [4], [5]. However, it has a relatively high input capacitance because of the large number of comparators. In each channel, a unity-gain voltage buffer is used between the SHDAC and the CABS ADC to isolate the SHDAC output from the load of the CABS ADC. Digitally-assisted analog design is becoming more popular these days, as it simplifies the stringent analog design considerations [6]. Hence, an on-chip digital calibration scheme using coarse and fine calibration codes was implemented to reduce the flash ADC comparators offsets [3]. A

This work was in part supported by the National Science Foundation under Award #1451213.

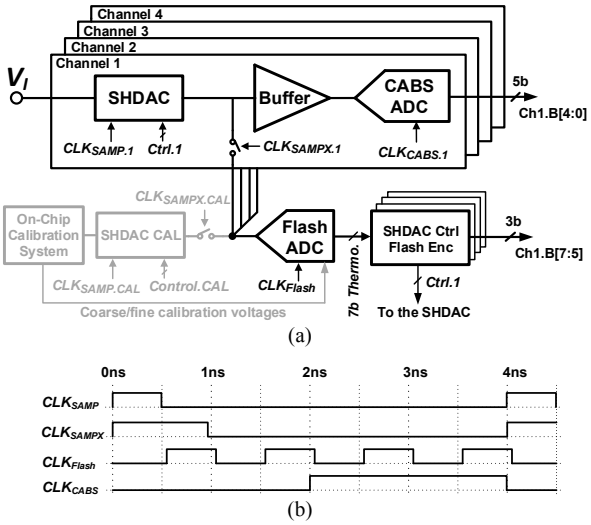


Fig. 1. (a) Single-ended representation of the hybrid ADC architecture, (b) timing diagram for one channel of the hybrid ADC.

clock generation system has been implemented to satisfy the jitter and timing-skew requirements for 1GS/s operation with 8-bit resolution [7]. At the beginning of each conversion, the SHDAC of channel *i* samples the input signal, and the switch between the SHDAC and flash ADC is closed while the ones in the other channels are opened. Then, the flash ADC resolves the first three MSBs. The SHDAC generates the residue voltage (based on the flash thermometer outputs) that passes through the unity-gain buffer. Finally, the CABS ADC performs the 5-bit conversion.

In Section II of this paper, the sensitivity of the SHDAC linearity correction method is reviewed. To supplement the analysis in [3], additional design considerations are provided for the amplifier in the unity-gain buffer, and for bandwidth mismatches in the TI channels. The measurement results of the fabricated prototype ADC chip are presented in Section III as another contribution in extension of the previous post-layout simulations in [3]. They provide first-time experimental proof-of-concept for the proposed low-power hybrid ADC architecture. Section IV contains concluding remarks.

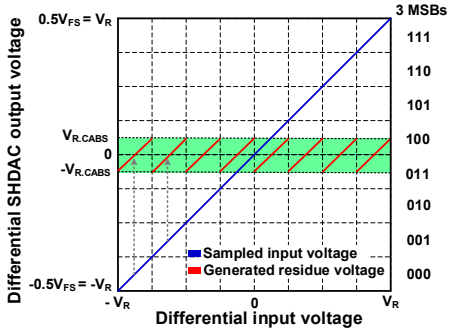


Fig. 2. Ideal transfer function of the SHDAC during sampling and residue generation (differential representation).

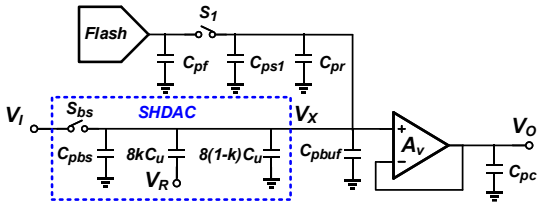


Fig. 3. Model with parasitic capacitances at the output of the SHDAC in one channel (single-ended equivalent).

TABLE I
SIMULATED ADC ENOB WITH SCALING FACTOR ("g") VARIATION

g	ENOB @ f_{in} = 2.93MHz	ENOB @ f_{in} = 491.2MHz
1.415	7.48	7.56
1.425	7.83	7.71
1.435	7.79	7.67

II. DESIGN CONSIDERATIONS FOR THE HYBRID ADC

A. SHDAC sensitivity to parasitic capacitances

To simplify the analysis, we use the single-ended model shown in Fig. 3; where C_{pbs}, C_{ps1}, C_{pf}, C_{pc}, C_{pbuf}, and C_{pr} respectively represent the parasitic capacitances at node V_X from the sampling bootstrap switch (S_{bs}), the switch between the flash and the SHDAC (S_1), the input of the flash ADC, the input of the CABS ADC, the input of the voltage buffer, and routing at the output of the SHDAC. The residue voltage can be estimated as in equation (1), where $C_{px} = C_{pbs} + C_{ps1} + C_{pbuf} + C_{pr}$, and C_{px1} and C_{px2} correspond to the total parasitic capacitance at the SHDAC output before and after residue generation, respectively.

$$V_{X2} = V_{X1} + \alpha \cdot k \cdot V_R + \beta \cdot V_{X1}, \quad (1)$$

where: $\alpha = \dfrac{8C_u}{8C_u + C_{pX2}}$ and $\beta = \dfrac{C_{pX1} - C_{pX2}}{8C_u + C_{pX2}}$.

The error due to β is negligible since the amounts of C_{pX1} and C_{pX2} are kept sufficiently close by design optimizations. The attenuation caused by α has been compensated by applying a constant scaling factor of $g = \alpha^{-1}$ to the SHDAC reference voltages as explained in [3]. Here, we evaluate the ADC performance sensitivity to the variation of the scaling factor (g), which originates from SHDAC reference voltage (V_R) variations. To consider a pessimistic case, we have simulated the transistor-level schematic of the ADC with about ±1% mismatch from the optimized value of g = 1.425. This mismatch corresponds to 5mV error on V_R, which is an extreme difference (1 LSB ≈ 4mV) when the SHDAC capacitors are matched in the layout. As seen from the simulation results in Table I, the ENOB of the hybrid ADC for a severe mismatch of "g" stays above 7.48.

B. DC gain requirement for the amplifier in the buffer

The voltage buffer plays a critical role because it can cause conversion errors in the CABS ADC. The voltage error ($V_{E.Gain}$) due to the limited DC gain (A_v) of the opamp is estimated as:

$$V_{E.Gain} = V_X - V_O = V_X - \left(\frac{A_v}{1+A_v}\right) \cdot V_X, \quad (2)$$

$$V_{E.Gain} = V_X \cdot \left(\frac{1}{1+A_v}\right), \quad (3)$$

where V_X is the ideal residue voltage and V_O is the buffer output. As indicated in Fig. 2, the maximum amplitude of the differential residue voltage (V_X in the center region) is $V_{FS}/2^4 = 2^4 \times LSB$. Therefore, to assure an error voltage below LSB/2, it is required that:

$$(2^4 \cdot LSB) \cdot \left(\frac{1}{1+A_v}\right) \le \frac{LSB}{2}, \text{ leading to } A_{vdB} \ge 29.8\text{dB}.$$

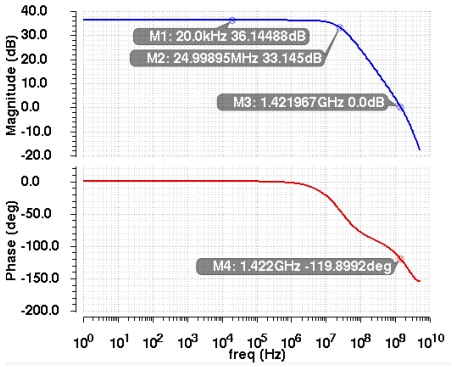


Fig. 4. Simulated gain and phase plots of the OTA in the unity-gain buffer.

The DC gain requirement for the residue voltage is only 30dB, which is low in comparison to the case of using a unity-gain buffer for a full $V_{FS}/2$ voltage swing that would require 48dB gain. Such relaxed gain requirement results in significant power reduction during the design of the amplifier for the hybrid ADC.

C. Amplifier bandwdith requirement

For a simple first-order approximation, let us consider a single-pole amplifier, i.e., with one dominant pole far below the unity-gain bandwidth (f_u) and the other pole(s) located far beyond f_u. For an amplifier in unity-gain configuration such as in this work, the voltage settling error ($V_{E.BW}$) due to limited bandwidth of the opamp can be expressed as:

$$V_{E.BW} = V_X - V_O = V_X - (1 - e^{-t/\tau}) \cdot V_X \quad (4)$$

$$V_{E.BW} = V_X \cdot e^{-t/\tau} = V_X \cdot e^{-2\pi \cdot f_u \cdot t} \quad (5)$$

where τ is the time constant of the amplifier. The total timing budget for the residue generation is 1ns (Fig. 1(a)), and the operational transconductance amplifier (OTA) has 0.8ns to settle to its final value since 0.2ns is needed for the SHDAC decoder and switched-capacitor operation. Therefore, the following requirement can be identified:

$$(2^4 \cdot LSB) \cdot e^{-2\pi \cdot f_u \cdot 0.8ns} \le \frac{LSB}{2}, \text{ resulting in } f_u \ge 670MHz$$

A telescopic cascode OTA was designed for the unity-gain buffer [5]. Fig. 4 shows its simulated magnitude and phase responses, where a capacitor of 250fF was used as the OTA load to model the input capacitance of the CABS ADC (C_{pc} in Fig. 3). The OTA for this hybrid ADC has a gain, unity-gain bandwidth and phase margin of 36.1dB, 1.42GHz and 60.1°, respectively. It consumes 0.6mW power from a 1.2V supply.

D. Time-interleaved bandwidth mismatches

Mismatches between the sampling bandwidths of the TI channels cause SNR degradation [8]. Each sampling circuitry can be approximately modeled with an RC circuit, behaving like a low-pass filter with a certain bandwidth. Bandwidth mismatch originates from two sources: First, the mismatches of the MOS transistor switch resistances and the sampling capacitances between each sample-and-hold. Second, the systematic RC mismatches between the input signal routing among the channels on the chip. Moreover, if a buffer amplifier is used in each S/H, the amplifier bandwidth mismatch will also contribute to the TI bandwidth mismatch. According to the analysis for a 4-channel TI ADC in [8], an overdesign of the sample-and-hold bandwidth (BW) suppresses the impact of bandwidth mismatches, as it is conceptually plotted in Fig. 5 based on the results in [8]. Therefore,

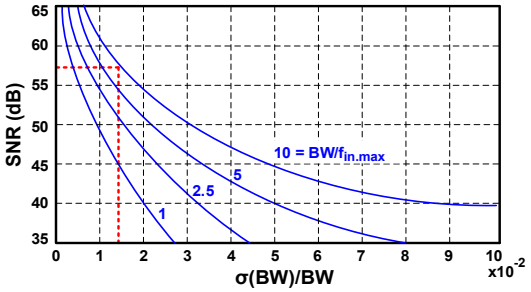


Fig. 5. Conceptual plots for a 4-channel TI ADC: SNR (dB) vs. σ(BW)/BW.

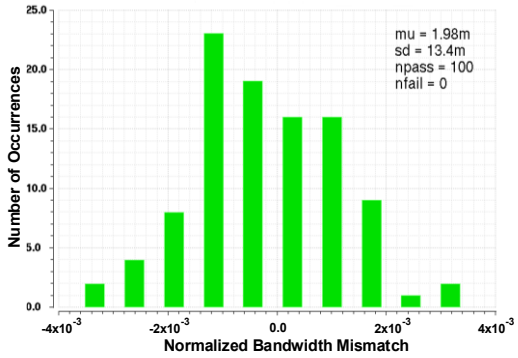


Fig. 6. Histogram of the SHDAC mormalized bandwidth mismatch from Monte Carlo simulations.

the SHDAC was overdesigned with 6.92GHz bandwidth and 60dB SNDR. Based on post-layout Monte Carlo simulations of the hybrid ADC, the total normalized bandwidth mismatch of the TI channels was obtained to be σ(BW)/BW = 0.013, as displayed in Fig. 6. According to Fig. 5, this value corresponds to a maximum achievable SNR of 57dB when the channel bandwidth is overdesigned by a factor of ten compared to the input bandwidth, implying sufficient margin for 8-bit resolution.

III. Measurement Results

A prototype ADC chip was fabricated in 130nm CMOS technology. Fig. 7 displays the micrograph of the ADC. Low voltage differential signaling (LVDS) outputs are used to read the four channels. The ADC core occupies 0.69mm^2, including all SHDACs, CABS ADCs, flash ADC, switches, thermometer-to-binary encoders, and clock generation circuits. The digital calibration occupies 0.71mm^2, which includes the calibration logic and its digital-to-analog converter, test signal generation, and extra calibration channel (SHDAC, unity-gain buffer).

A custom printed circuit board (PCB) was designed for the measurements of the ADC chip. The digital outputs from the four channels of the ADC were recorded with a logic analyzer and evaluated in MATLAB. For the tested ADC chip on the PCB, the optimum coarse and fine calibration codes plus the offset polarity bit for each comparator in the flash ADC are listed in Table II. A histogram testing method was employed to evaluate DNL and INL errors of the hybrid ADC while applying a 3.235MHz sinusoidal input signal. The measured DNL and INL for the 8-bit outputs of the hybrid ADC revealed large nonlinearity errors even after flash ADC offset calibration. The main cause for the high 8-bit DNL/INL is the large offset in the comparators of the fabricated CABS ADCs due to random device mismatches. Therefore, the hybrid ADC was also evaluated for 6-bit operation by neglecting the last 2 LSBs to achieve acceptable nonlinearity errors. Fig. 8 displays measured

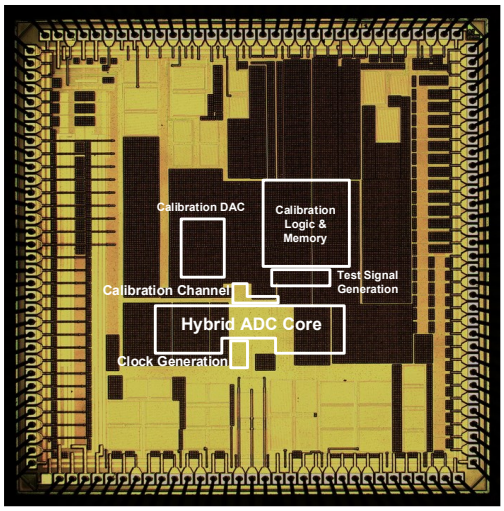


Fig.7. Micrograph of the hybrid ADC chip.

DNL and INL errors of the hybrid ADC with 6-bit equivalence before and after flash ADC calibration, respectively. As seen from Figure 8, the nonlinearity errors of the hybrid ADC have been significantly reduced by the calibration of the flash ADC. The 6-bit DNL and INL errors after flash ADC offset calibration are within -0.41/+0.50 LSB and -0.77/+0.52 LSB, respectively.

Fig. 9 shows the measured output spectra of the hybrid ADC with 6-bit evaluation at a sampling rate of 1GS/s with low-frequency and high-frequency (near Nyquist rate) sinusoidal full-scale input signals. The 6-bit 1GS/s hybrid ADC achieves 33.42dB SNDR and 45.71dB SFDR with a near Nyquist rate input frequency. The 6-bit evaluation of the 1GS/s hybrid ADC revealed an ENOB of 5.26 with a near Nyquist rate input frequency. In comparison to the 8-bit performance, the ENOB at Nyquist rate only degraded by 0.22 bit (Table III). Note that for the evaluations of this work, the post-processing did not involve

TABLE II
Offset Calibration Codes for the Comparators in the Flash ADC

	Polarity	Coarse Code	Fine Code
Comparator 1	1	00011 (3)	000100 (4)
Comparator 2	1	00000 (0)	000010 (2)
Comparator 3	0	00010 (2)	001011 (11)
Comparator 4	0	00010 (2)	010000 (16)
Comparator 5	0	00110 (6)	100000 (32)
Comparator 6	0	00011 (3)	010100 (20)
Comparator 7	0	00101 (5)	011000 (24)

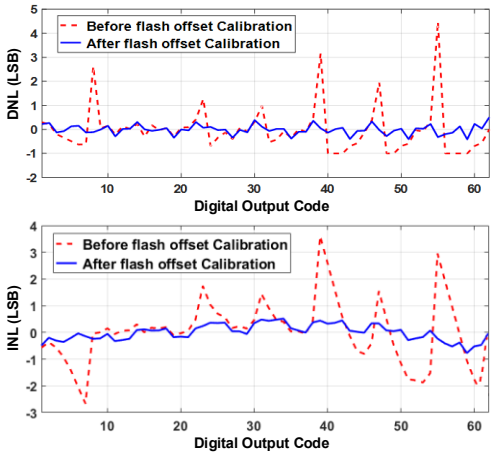


Fig.8. Measured DNL and INL of the hybrid ADC before and after flash ADC offset calibration (6-bit evaluation).

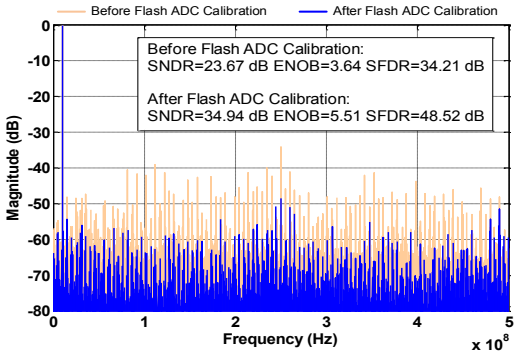
TABLE III
SUMMARY OF THE HYBRID ADC MEASUREMENT RESULTS AND COMPARISON TO OTHER WORKS

Specification	This work		[1] TVLSI,15	[2] JSSC,09	[9] JSSC,13	[10] TCASII,11	[11] JSSC,06	[12] JSSC,14	[13] JSSC,17	[14] TCASI,17
Sampling Rate (GS/s)	1	1	1	1.25	1.6	1.5	0.6	1	1.2	0.8
Resolution (bit)	6	8	8	6	6	7	6	6	8	6
CMOS Technology (nm)	130	130	55	130	90	90	130	65	65	65
ENOB @ NQ	5.26	5.48	6.19	5.0	4.44	6.05	5.02	5.16	6.97	4.8
SNDR @ NQ (dB)	33.42	34.74	39	32	28.5	38.2	32	32.8	43.7	30.6
SFDR @ NQ (dB)	45.71	46.03	53	35	35.5	46.6	46	44	58.1	36.2
Supply Voltage (V)	1.2	1.2	1.2	1.2	1.3	1.2	1.2	1.1	1.3	1
Power (mW)	10.5	11	16	32	20.1	204	5.3	9.9	5	3.62
Area (mm^2)	$< 0.72^2$, $< 1.4^3$	0.72^2, 1.4^3	0.2	0.09	0.24	1.2	0.12	0.044	0.013	0.012
FoM[1] @ NQ (fJ/conv. step)	274	246	219	800	579	2053	272	278	35	162

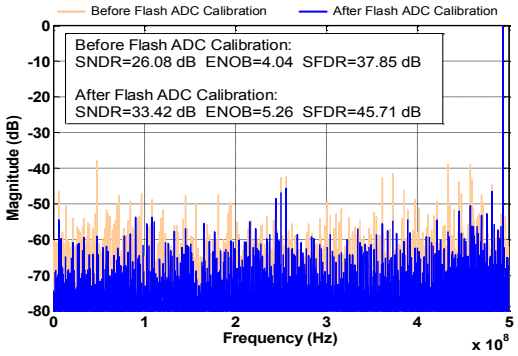
1: FoM = Power / ($2^{ENOB\ @\ NQ} \times f_s$), 2: ADC core area only, 3: total area with calibration circuitry

the calibration of the impacts from time-interleaved channel mismatches (offset, gain and timing). The dynamic performance of the hybrid ADC was also assessed with measurements at various input frequencies over the Nyquist bandwidth using 6-bit equivalence, from which the results are displayed in Fig. 10.

The total measured analog power is 6.6mW, including the flash ADC (1.05mW), all CABS ADCs (1.19mW), SHDACs with decoders (0.81mW), and the four unity-gain buffers with eight OTAs (3.55mW). The total digital power is 0.86mW, including the D flip-flops and thermometer-to-binary encoders at the flash ADC output. The measured power consumption of the clock generation circuitry and the clock buffer are 3.54mW and 2.35mW, respectively. Therefore, the total power consumption of the 8-bit 1GS/s ADC is 11mW, excluding the clock buffer that was used for testing. For a fair 6-bit evaluation of the hybrid ADC, the power consumption should be adjusted to account for the fact that the last two LSBs of the ADC output are not used. Reducing the CABS ADC resolution to 3-bit, results in a significant reduction of the area and input capacitance of the CABS ADC. Moreover, the number of active comparators in the CABS ADC is reduced from 5 to 3, leading to 40% reduction of the power consumed by the CABS ADC, which is 0.5mW. Therefore, the total power consumption of the hybrid ADC for 6-bit evaluation is 10.5mW, strictly based on measurement data.



(a)



(b)

Fig. 9. Measured output spectra (8192-point FFT) of the 6-bit 1GS/s hybrid ADC output for (a) f_{in} = 10.193MHz, (b) f_{in} = 493.958MHz before and after flash offset calibration.

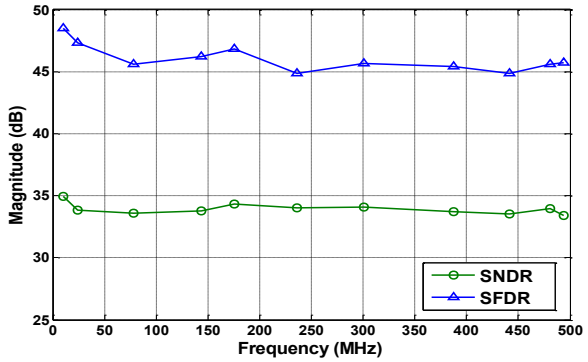


Fig. 10. SNDR & SFDR vs. input frequency at f_s = 1GS/s (6-bit evaluation).

Table III lists the measured performance specifications of the fabricated hybrid ADC chip in comparison to the other reported ADCs with similar resolutions and sampling rates. The power consumption of the hybrid ADC is reported as the measured power for the 8-bit and 6-bit cases. Furthermore, an estimated power for a 6-bit redesign of the hybrid ADC is reported for comparison. The hybrid ADC fabricated in 130nm CMOS technology stands amongst the ADCs with a low FoM due to its power efficiency. A lower FoM would be expected if the hybrid ADC was designed and fabricated in a technology with smaller channel length because the architecture would benefit from transistors with higher transition frequencies (f_T) and considerably lower parasitic capacitances. Furthermore, a CABS ADC offset calibration method could be explored for DNL/INL improvement. Overall, in comparison to the specifications of other works in Table III, the measurement results of the proposed ADC architecture provide a proof-of-concept for its efficiency and performance.

IV. CONCLUSION

The proposed hybrid ADC architecture was demonstrated with a design fabricated in 130nm CMOS technology to verify its feasibility with measurements. Offsets of the comparators in the flash ADC were calibrated using a digital calibration technique, which revealed significant performance improvement. From the measurement results, the 6-bit 1GS/s ADC output has an ENOB of 5.51 and 5.26 when applying a full-scale sinusoidal input signal at low and high (near Nyquist-rate) input frequencies, respectively. The 6-bit 1GS/s ADC consumes 10.5mW from a 1.2V supply. Even though it was fabricated in 130nm CMOS, it has a relatively low FoM amongst other reported works due to its power efficiency.

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