Study of Performance Impact from Powering RF Receiver Front-End Circuits with a DC-DC Converter

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***Abstract* — This paper studies the effects of DC-DC switching converters on RF and analog baseband circuits. Simulations of a low-noise amplifier, mixer, and lowpass filter have shown that the impact of switching supply noise can be kept to small levels by design. For the case of loads with frequency conversion, a boost converter design technique to shift the switching frequency of the converter out of the band of interest is proposed.**

***Keywords* — DC-DC converter, low-noise amplifier, mixer, operational transconductance amplifier (OTA), OTA-C filter.**

I. Introduction

In recent years, there have been rapid advancements in ultra-low power systems such as wireless sensors, implantable devices and Internet of Things (IoT) devices [1], [2]. These devices are usually powered from limited power sources and hence require highly efficient power supplies [3]. A low-power system-on-a-chip (SoC) often includes multiple power supplies to meet the performance specifications of different analog and digital blocks. Energy harvesting circuits employing switching converters and low-dropout regulators (LDOs) are often used to power such ultra-low power (ULP) SoCs.

Conventionally, LDOs are employed to supply analog and sensitive radio frequency (RF) blocks [4], [5], [6] as depicted in Fig. 1(a). This is because the ripple and the switching activity of a DC-DC converter can potentially degrade the performance of sensitive RF and analog circuit by generating noise components at signal band frequencies, and can cause interference via supply feedthrough. LDOs have a high power supply rejection ratio (PSRR), but at the cost of low efficiency, especially with light loads. On the other hand, DC-DC switching converters have high efficiencies, but also have supply ripples. Owing to the ripples, they are mostly used for digital blocks, where signals are resilient to noise. They are not yet widely adopted for RF and analog circuits.

The use of DC-DC converters for supplying one or multiple analog and digital blocks in ultra-low power (ULP) IoT SoCs has recently been discussed in the literature due their high efficiency [1], [7], [8]. A recent system level SoC design analysis indicates that the life-time of an IoT device can be increased by over 4x by simply operating the SoC with a single inductor multiple output (SIMO) buck-boost DC-DC converter with a lower minimum operating voltage [2], when compared to a more conventional IoT SoC designed with an LDO based power management [9]. Such a significant improvement in life-time makes a case for using DC-DC converters in ULP IoT SoCs. However, we need to analyze the impact of DC-DC converters on sensitive RF and analog circuits to understand the design space well. This paper evaluates the performance of RF receiver front-end and analog baseband circuits when operated directly from a DC-DC converter supply. Various performance metrics of a low-noise amplifier (LNA), mixer, and baseband filter are evaluated through simulations with both an ideal supply and a DC-DC switching converter. Our analysis indicates that there is negligible impact on the examined analog/RF circuits. This paper also presents a way to dynamically change the switching frequency of a boost converter to reduce interference and provide further design robustness.

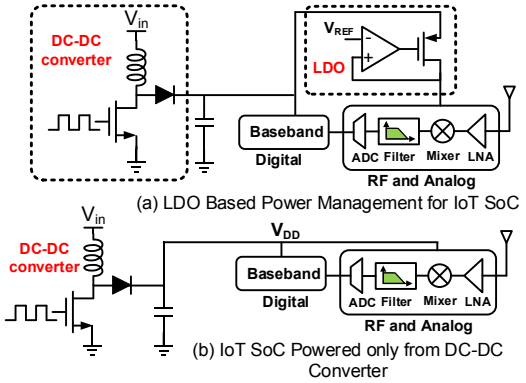

Fig. 1. Power management techniques for IoT SoCs: (a) high performance, (b) high efficiency.

Section II contains a literature review of previous works with RF transceiver circuits supplied by switching DC-DC converters. Section III describes the methodologies and the simulation procedures to assess performance of the different circuits while being powered by an ideal supply and or a supply with ripples. Section IV illustrates performance improvement using a boost converter with controlled pulse frequency modulation (PFM). Section V provides concluding remarks on the method and results.

II. Use of DC-DC Converters for Analog Circuits

Previous analyses of powering RF and analog circuits with DC-DC converters have mainly focused on mobile applications with relatively high power consumption. An analysis of the output spectrum of buck converters in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) mode can be found in [10] and [11]. A detailed analysis along with the mathematical equations are provided to predict the magnitude and frequency spread of the output voltage ripple. Prior research has been conducted to nullify the effects of switching harmonics on noise-sensitive loads. Passive filters can also be used to suppress harmonic distortions, but this results in area overhead or costly off-chip components.

An efficient method to operate analog loads with switching converters is to avoid the frequencies of the harmonics. This can

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be achieved through frequency hopping. In [12] and [13], the switching frequency is randomly varied between different values, which leads to a reduction of the spurs from the converter. Reduction of spurs requires high hopping rate, which can be difficult to achieve while maintaining clock and switching frequency synchronization with complex circuitry.

A master-slave hybrid architecture with linear regulation and switched modulator is employed for a power amplifier (PA) [14]. The ripple cancellation is achieved by a linear amplifier that provides a current that is out-of-phase to the inductor current in the switching converter. This technique leads to efficiency reduction in low-power applications with light load conditions.

A multistage interleaved synchronous converter with multiphase operation is presented in [15]. Although this technique reduces output spurs, it leads to large area overhead, as multiple inductors are required. Furthermore, the multiple clock phases require synchronization. Noise shaping is used in [16] to reduce switching noise, where the PWM controller is replaced with a Σ-Δ modulator such that the noise power is moved away from low frequencies of interest to the high-frequency range.

Most of the efforts on supplying power to RF circuits from switching converters have been focused on PAs [17], [18]. This is because the PA is the most power-hungry component in the RF front-end and hence should have very efficient power supplies. Wake-up radios have also been powered from switching converters [19]. This paper addresses the need to investigate the effects of DC-DC converters on low-power RF receiver front-end circuits, and proposes a technique to avoid in-band noise with a PFM-controlled boost converter.

III. Methodology and Case Studies

In this work, low-power RF receiver front-end circuits (from [20], [21], and [22]) and an analog baseband filter (from [23]) are investigated in the presence of supply noise. The circuits of interest are a differential LNA operating at 2.4 GHz, a double-balanced active mixer with an output frequency of 10 MHz, and a second-order baseband filter with 0.5 MHz cutoff frequency. Fig. 2 shows the schematics of the LNA and mixer, and Fig. 3 shows the baseband filter with its operational transconductance amplifier (OTA) and common-mode feedback (CMFB) circuit.

A. RF Front-End

A differential LNA and a double-balanced active mixer are utilized to examine the effect of switching harmonics from the supply. The front-end was operated with both an ideal voltage supply and a supply with emulated switching noise.

A DC-DC switching converter output waveform is characterized by its ripple and switching frequency. A large ripple can shift the operating point of the circuit under test, while the switching frequency and its harmonics can fall within the band of interest as interference. The triangular waveform of the boost converter can be approximated by a sine wave of equal ripple magnitude and frequency in order to permit the use of

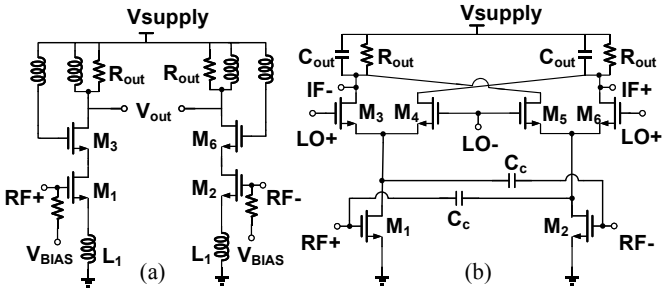


Fig. 2. RF front-end: (a) LNA and (b) mixer from [20] under evaluation.

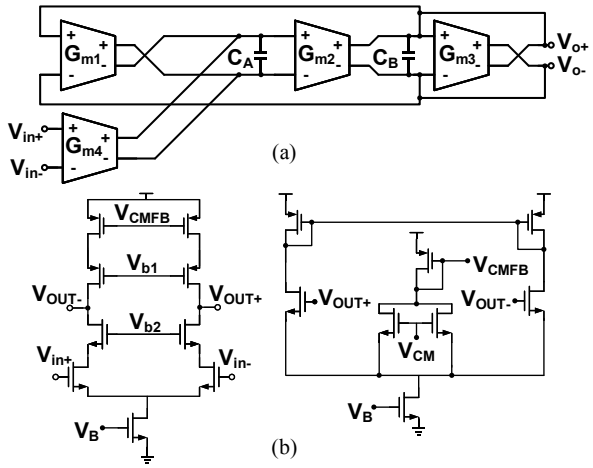


Fig. 3. (a) Filter from [23] re-designed with a conventional (b) OTA and CMFB.

standard simulation methods such as periodic steady-state (PSS) analysis. Hence, we employed a power supply with a superimposed sinusoidal ripple to emulate the waveform of a DC-DC converter. The performance of the LNA was evaluated with this power supply model. The supply voltage has an amplitude of 4 mV (8 mV peak-to peak ripple, around 1.5%) for a 600mV DC supply, which is in the typical range for practical DC-DC converters. The RF front-end was simulated with this supply over a wide range of DC-DC converter switching frequencies up to 250 MHz. We chose this emulation of the DC-DC converter waveform to realize a combined simulation setup for the RF front-end circuits and DC-DC converter with standard Cadence simulation tools. Furthermore, a wide sweep of the converter's switching frequency also captures the impact of high-frequency harmonics of a triangular waveform or other noise.

For the LNA, the noise figure (NF) simulation was performed with PSS analysis to capture the effect of the supply ripple. Since noise figure of the LNA is added directly to the equivalent noise figure of the subsequent blocks in the receiver chain, it is a critical performance metric. As figure of merit for the mixer, the spurious free-dynamic range (SFDR) was assessed from the output spectra after transient simulations which included noise. The SFDR is a good measure of the noise and distortion characteristics, and hence it was chosen as the performance metric for the mixer.

Important performance metrics of both the LNA and mixer were compared with an ideal supply and a supply with noise. Fig. 4(a) shows the NF of the LNA with ideal supply and with supply noise having a frequency of 10 MHz.

The NF degrades by 0.38 dB. Since the switching frequency of the converter is small compared to the operating frequency of the LNA, its harmonics do not degrade the performance of the LNA significantly. Also, Fig. 4(b) reveals that the noise figure

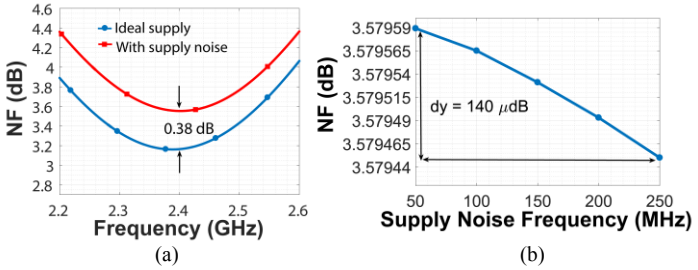


Fig. 4. Simulated noise figure of the LNA: (a) with ideal supply (in blue) and supply noise (in red) with 8 mV ripple and 10 MHz frequency, (b) with supply noise of varying frequency.

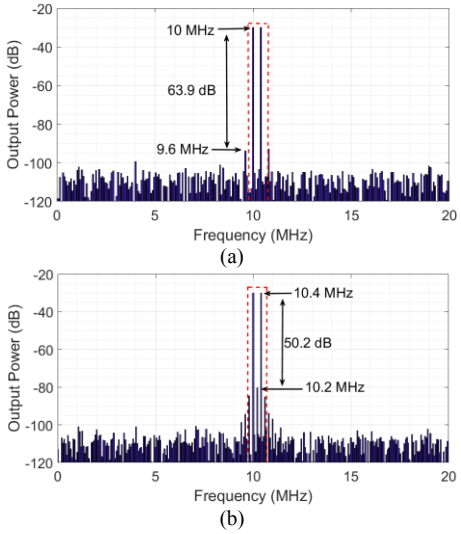


Fig. 5. (a) SFDR of the mixer with ideal supply, (b) SFDR of mixer with supply having a ripple of 20 mV and a frequency of 200 KHz. The region within the dashed red line is the 1 MHz band of interest.

does not degrade significantly with higher converter frequencies, as long as they are far from the center frequency of the LNA.

To assess the impact of the DC-DC converter on the mixer, it was powered by an ideal supply and a triangular wave supply of 20mV ripple and 200 KHz frequency to emulate the output waveform of a boost converter. The SFDR of the mixer is shown in Fig. 5. Its output is centered around 10 MHz, and a bandwidth of 1 MHz is annotated as an example aligned with Bluetooth Low Energy (BLE) receivers [24]. The SFDR degrades by 13.7 dB when powered by a switching converter. This degradation is seen because the mixer mixes the signal with the power supply noise and generates components that fall within the band of interest (9.5 MHz - 10.5 MHz). As illustrated in Section IV, this impact can be improved by shifting the converter frequency out of band such that the switching harmonics from the DC-DC converter do not appear as close to the band of interest at the mixer output.

B. Baseband OTA-C Filter

The effect of DC-DC switching converter ripples on the performance of analog baseband circuits was investigated by simulating the analog baseband lowpass biquad filter in Fig. 3. The filter was supplied with an ideal 600 mV DC voltage source in one scenario representing an LDO, and a sawtooth-shaped voltage source of a DC value of 600 mV and a ripple of 8 $mV_{p\text{-}p}$ in the other scenario representing a DC-DC switching converter.

Baseband filters are often assessed by a figure of merit (FoM), such as the one from [25]:

$$FoM = \frac{Power}{n \cdot f_c \cdot SFDR}, \quad (1)$$

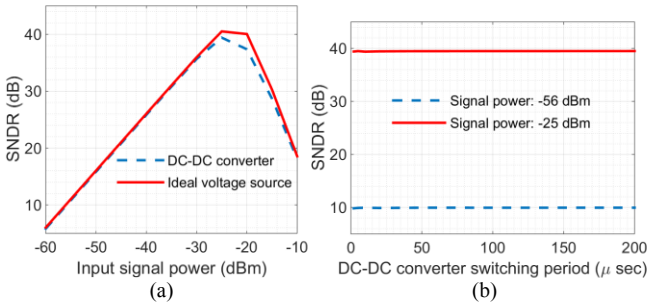


Fig. 6. Filter SNDR vs. (a) input signal power, and (b) DC-DC converter switching period.

where n is the filter order, f_c is the cutoff frequency of the filter, and SFDR is the spurious free-dynamic range. This FoM is affected by a DC-DC switching converter as it impacts the SFDR. Other parameters (power, order, and cutoff frequency) are not affected by the supply noise. The SFDR does not depend on noise floor unless the noise is excessive. Since noise floor is raised due to supply noise, the signal-to-noise and distortion ratio (SNDR) was chosen instead of the SFDR to assess the effect of DC-DC switching converters.

In each of the two scenarios, the SNDR was evaluated by running transient simulations with noise enabled. A wide range of DC-DC converter frequencies were tested to simulate the effect of the switching frequency on the SNDR. The aforementioned assessment was conducted with two input levels: a high-amplitude signal and a low-amplitude signal, allowing to observe the cases where the SNDR is limited by the noise floor and where it is limited by distortion.

Fig. 6(a) displays the SNDR of the filter at different input power levels with a signal frequency of 50 KHz. The two curves demonstrate that the difference between powering the filter from an ideal voltage source and a DC-DC converter is negligible within the linear range. At low input signal power levels, the SNDR is limited by the noise floor. Therefore, it increases linearly with a slope of 1 dB/dBm at low input signal power levels until it peaks at 25 dBm. After the peak, the SNDR begins to degrade due to the increase of harmonic distortion components.

Fig. 6(b) shows the variation of the filter SNDR with different DC-DC converter switching periods. This assessment was made to investigate the effect of switching frequency on SNDR to determine if there is any correlation between the input signal frequency and the switching frequency. The input frequency during this simulation was 50 KHz. Two input signal power levels were chosen (-56 dBm and -25 dBm) to evaluate cases with low and high SNDR. To account for worst-case ripples, the ripple amplitude of the DC-DC switching converter was kept constant at 8 $mV_{p\text{-}p}$, even though it reduces at lower switching periods. It can be observed from the curves that there is almost no effect of the DC-DC converter switching frequency on SNDR in both cases.

Fig. 7 displays the Monte Carlo mismatch simulation results for the SNDR of the filter with an input signal frequency of 50 KHz and power of -25 dBm, which corresponds to one of the highest achievable SNDRs for this filter. The number of Monte Carlo simulation runs was 200 for each of the two histograms. The results in Fig. 7(a) are for the case with an ideal voltage source powering the filter, and the results in Fig. 7(b) are for the case with supply ripples. It can be observed that there is almost no change in the SNDR average or standard deviation, and that both histograms follow the same profile.

The described simulation results indicate that there is only a minor effect on SNDR of the filter whether it is powered by an ideal voltage source or a source with ripples emulating a DC-DC converter.

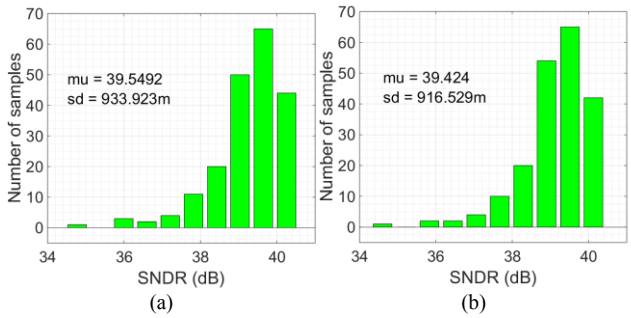


Fig. 7. Filter SNDR Monte Carlo simulation results: (a) with ideal voltage source, (b) with supply ripples to emulate a DC-DC converter.

IV. Performance Improvement with a Controlled PFM Boost Converter

To maintain high efficiency at light loads, pulse frequency modulation (PFM) in discontinuous conduction mode (DCM) is a preferred control scheme for ULP IoT devices because pulse width modulation (PWM) control becomes inefficient at light loads. In PFM mode, the switching frequency scales directly with output load, which helps in achieving higher efficiencies at light loads. However, this also results in a switching frequency and its harmonics that are load-dependent, and can cause interference in the downstream analog circuits. In this work, we present a boost converter with a PFM controller, where the switching frequency can be modulated while avoiding the frequency band of interest.

Fig. 8 shows the architecture of a typical boost converter circuit that operates with a PFM control scheme. This architecture is well suited for low-power SoCs where the inductor in the boost converter is operated in DCM. The boost converter architecture follows the circuit architecture of the low-voltage boost converter circuit detailed in [26]. A typical operation of the boost converter incorporates two switching cycles. The low-side (LS) switching is where transistor M_{LS} is turned on and the inductor is charged to its peak value (I_{PEAK}). In the next cycle, the total charge in the inductor is sent to the storage capacitor and a zero-detection circuit controls transistor M_{HS} to accurately use it as a diode. The control of the M_{HS} switch is realized with a zero detection and control circuit. This way the inductor is charged and discharged to raise the output voltage.

The comparator C_1 is used for regulation, which is performed in the following manner: Once V_{DD} goes below V_{REF}, the comparator turns on, which puts the boost converter in a continuous switching loop. In this loop, first the LS switching and then the high-side (HS) switching are performed. After the HS switching, the next switching cycle commences after a finite amount of dead time. In this manner, several switching cycles are performed until the V_{DD} level goes above V_{REF} and the comparator transitions to low, disabling the switching loop. Now in the absence of switching from the boost converter, the load at the output will start discharging the capacitor until its voltage is below V_{REF}. Once it crosses V_{REF}, the switching loop is enabled again.

The comparator C_1 is the key component that regulates the supply. The time that comparator takes to respond to the change in V_{REF} directly depends on its bandwidth, which can be controlled through the bias current (I_{BIAS}). Fig. 9(a) shows that with higher power consumption, the comparator can operate at higher frequency. In this case the converter will generate a lower ripple. With lower power consumption, the comparator will switch at a lower frequency, resulting in a higher ripple. We observed from the analysis of the RF front-end that low-frequency ripples have more adverse effects on the SFDR of mixers if frequency-translated components fall into the passband.

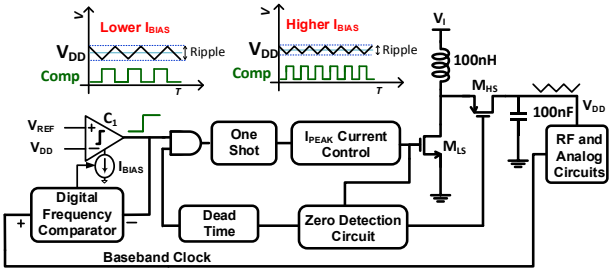
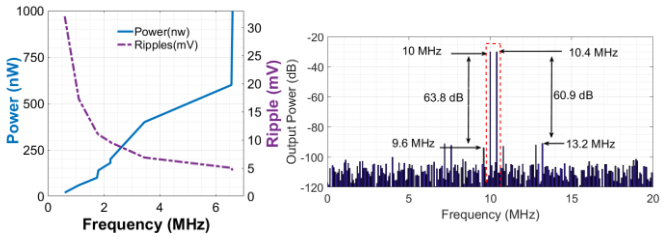


Fig. 8. DC-DC converter model with variable frequency.



(a) (b)

Fig. 9. (a) Comparator power consumption and ripples vs. frequency of the V_{DD} signal generated by the proposed DC-DC switching converter at the same output power of 1.64 mW. (b) SFDR of the mixer with supply noise of 2.8 MHz frequency. The region in red indicates the 1 MHz band of interest.

We can control the amplitude of the ripple and its frequency by directly controlling I_{BIAS}. The controller in Fig. 8 controls I_{BIAS} through a frequency comparator by comparing the switching frequency and the baseband frequency. If both frequencies are close to each other, then I_{BIAS} is increased to achieve higher switching frequency. This method of controlling the power supply ripple and frequency has a nominal effect on the efficiency of the converter. The converter efficiency will largely be determined by the LS and HS switching, which is controlled through peak inductor control every cycle [26]. In this control scheme, we do not change the LS and HS timing, but only the number of switching cycles that are performed in one period of the comparator output. We estimate that in the high-power mode for lower ripples, the efficiency will degrade by 0.05% when supplying a 1.64 mW load.

We utilized the above described method to improve the SFDR of the mixer, which degraded in the presence of a 200 KHz ripple (see Fig. 5 (b)). The switching frequency of the converter was shifted to a higher frequency of 2.8 MHz by increasing the bias current of comparator C_1. This lowered the ripple in the boost converter output. The improved SFDR with 8 mV ripple is annotated in Fig. 9(b). The SFDR of the mixer does not degrade (in comparison to Fig. 5 (a)) with high-frequency supply noise. This is because the high frequency supply noise falls outside the band of interest of 1 MHz and also has a lower ripple compared to the lower frequency case. Table 1 provides a summary of the simulated performance evaluations for the LNA, mixer, and filter.

V. Conclusion

In this paper, a study based on simulations was carried out to investigate the performance impacts on receiver front-end circuits supplied by a DC-DC switching converter. This study included both RF blocks (LNA and mixer) and a baseband block (filter). It was observed that the performance effects were small for the LNA and baseband filter. However, the SFDR of the mixer was reduced by approximately 14 dB due to the supply noise ripple. This impact can be minimized using a controller architecture whose switching frequency can be adjusted by changing the comparator bias current. A boost converter design technique to shift the switching frequency of the converter out of the band of interest was introduced for this purpose.

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Table 1. Performance comparison

	Ideal Supply	Supply with Ripple
LNA NF (dB)	3.18	3.58
Mixer SFDR (dB)	63.9	63.8*
Filter SNDR (dB)	39.55	39.42

* After switching frequency of boost converter is shifted to 2.8 MHz

REFERENCES

[1] A. Klinefelter, N. Roberts, Y. Shakhsheer, P. Gonzalez, A. Shrivastava, A. Roy, K. Craig, M. Faisal, J. Boley, S. Oh, Y. Zhang, D. Akella, D. Wentzloff and B. Calhoun, "A 6.45µw self-powered IOT SoC with integrated energy-harvesting power management and ULP asymmetric radios," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015.

[2] N. Shafiee, S. Tewari, B. H. Calhoun, A. Shrivastava, "Infrastructure circuits for lifetime improvement of ultra-low power IoT devices," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 64, no. 9, pp. 2598-2610, Sep. 2017.

[3] Y.-J. Park, J.-H. Park, H.-J. Kim, H. Ryu, S. Kim, Y. Pu, K. Hwang, Y. Yang, M. Lee and K.-Y. Lee, "A design of a 92.4% efficiency triple mode control DC–DC buck converter with low power retention mode and adaptive zero current detector for IoT/wearable applications," *IEEE Trans. Power Electronics*, vol. 32, no. 9, pp. 6946-6960, Sep. 2017.

[4] S. Chunlei, B. C. Walker, E. Zeisel, B. Hu, G. H. McAllister, "A highly integrated power management IC for advanced mobile applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1723-1731, Aug. 2007.

[5] C.-J. Park, M. Onabajo, and J. Silva-Martinez, "External capacitor-less low drop-out regulator with 25dB superior power supply rejection in the 0.4-4MHz range," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 486-501, Feb. 2014.

[6] M. El-Nozahi, A. Amer, J. Torres, K. Entesari and E. Sanchez-Sinencio, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565-577, March 2010.

[7] A. Shrivastava, Y. K. Ramadass, S. Khanna, S. Bartling and B. H. Calhoun, "A 1.2µW SIMO energy harvesting and power management unit with constant peak inductor current control achieving 83–92% efficiency across wide input and output voltages," in *Proc. Symp. VLSI Circuits (VLSIC)*, June 2014.

[8] M. Alhawari, D. Kilani, B. Mohammad, H. Saleh and M. Ismail, "An efficient thermal energy harvesting and power management for µWatt wearable BioChips," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2016.

[9] Y. Zhang, F. Zhang, Y. Shakhsheer, J. Silver, A. Klinefelter, M. Nagaraju, J. Boley, J. Pandey, A. Shrivastava, E. Carlson, A. Wood, B. Calhoun and B. Otis, "A batteryless 19 µW MICS/ISM-band energy harvesting body sensor node SoC for ExG applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 199-213, Jan. 2013.

[10] C. Tao and A. Fayed, "Analysis and modelling of buck converters output spectrum in CCM with PWM control," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 2011.

[11] Tao, Chengwu, and Ayman Fayed. "Output spectrum analysis of buck converters in DCM with PFM control," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2012.

[12] C. Tao and A. A. Fayed, "Spurious-noise-free buck regulator for direct powering of analog/RF loads using PWM control with random frequency hopping and random phase chopping," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 396-397.

[13] Chen, Jau-Horng, Pang-Jung Liu, and Yi-Jan Emery Chen. "A spurious emission reduction technique for power amplifiers using frequency hopping DC-DC converters," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, June 2009, pp. 145-148.

[14] Chu, Wing-Yee, Bertan Bakkaloglu, and Sayfe Kiaei. "A 10 MHz bandwidth, 2 mV ripple PA regulator for CDMA transmitters," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2809-2819, Dec. 2008.

[15] S. Abedinpour, B. Bakkaloglu and S. Kiaei, "A multistage interleaved synchronous buck converter with integrated output filter in 0.18 µm SiGe process," *IEEE Trans. Power Electronics*, vol. 22, no. 6, pp. 2164-2175, Nov. 2007.

[16] S. K. Dunlap and T. S. Fiez, "A noise-shaped switching power supply using a delta-sigma modulator," *IEEE Trans. on Circuits Syst. I: Reg. Papers*, vol. 51, no. 6, pp. 1051-1061, June 2004.

[17] A. A. Fayed, "Efficient powering of RF PAs using DC-DC power supplies," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2013.

[18] E. J. Kim, C. H. Cho, W. Kim, C. H. Lee and J. Laskar, "Spurious noise reduction by modulating switching frequency in DC-to-DC converter for RF power amplifier," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2010, pp. 23-25.

[19] N. Roberts, K. Craig, A. Shrivastava, S. Wooters, Y. Shakhsheer, B. Calhoun and D. Wentzloff, "A 236nW -56.5 dBm-sensitivity Bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 450-451.

[20] L. Xu, C. H. Chang and M. Onabajo, "A 0.77 mW 2.4 GHz RF front-end with -4.5 dBm in-band IIP3 through inherent filtering," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 5, pp. 352-354, May 2016.

[21] L. Xu, K. Wang, C.-H. Chang, and M. Onabajo, "Inductorless linearization of low-power active mixers," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2015.

[22] C.-H. Chang, and M. Onabajo, "Low-power low-noise amplifier IIP3 improvement under consideration of the cascode stage," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2017.

[23] M. A. A. Ibrahim and M. Onabajo, "Linear input range extension for low-voltage operational transconductance amplifiers in Gm-C filters," in *Proc. IEEE Intl. Symp. on Circuits and Systems (ISCAS)*, May 2017.

[24] A. A. Emira and E. Sanchez-Sinencio, "A pseudo differential complex filter for Bluetooth with frequency tuning," *IEEE Trans. Circuits Syst. I*: Analog and Digital Signal Processing, vol. 50, no. 10, pp. 742-754, Oct. 2003.

[25] S. Peng, Y.-H. Lee, T.-Y. Wang, H.-C. Huang, M.-R. Lai, C.-H. Lee and L.-H. Liu, "A power-efficient reconfigurable OTA-C filter for low-frequency biomedical applications," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 65, no. 2, Feb. 2018.

[26] A. Shrivastava, N. E. Roberts, O. U. Khan, D. D. Wentzloff, and B. H. Calhoun, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and -14.5 dBm, 915 MHz RF kickstart," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1820–1832, Aug. 2015.