Design Techniques for Mitigation of Intermodulation Distortion Components in CMOS RF Receiver Front-End Circuits with Subthreshold Operation

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Abstract:

This paper provides an overview of target applications and design aspects for emerging radio frequency (RF) front-end circuits with subthreshold biasing to reduce power consumption. Design methods are described to linearize a subthreshold pseudo-differential common-source cascode low-noise amplifier (LNA) and a subthreshold active mixer. The linearization techniques can improve the third-order intermodulation intercept point (IIP3) through the use of passive components, which implies that they do not require auxiliary amplifiers to suppress third-order distortion components, and therefore do not incur any extra power consumption. A 1.95 GHz receiver front-end chip with a narrowband LNA and down-conversion mixer was designed and fabricated in 110nm CMOS technology. Measurement results show that the linearized low-power front-end has a 20.6 dB voltage gain, a 9.5 dB double sideband noise figure, and a -10.8 dBm IIP3 with a power consumption of 0.9 mW.

Keywords: Subthreshold low-noise amplifier; subthreshold active mixer; linearization; low-power RF design; RF front-end circuits

1 Introduction

A number of low-power wireless standards and circuit design approaches have been developed for low-rate wireless personal area network (WPAN) and wireless body area network (WBAN) communication [1]-[5]. The associated standards include IEEE 802.15.4, IEEE 802.15.6, Bluetooth low energy (BLE), Near Field Communication (NFC), and Global Positioning System (GPS). Their range of applications includes health and fitness monitoring, wireless sensor nodes, automated payments, and smart home applications. Fig. 1 illustrates an envisioned WBAN scenario as an example of remote medical monitoring. In this application, patients can use implantable or wearable biomedical sensors with wireless connectivity to upload their health information to doctors immediately [6]-[9]. As shown in Fig. 2, the required power consumption of WBAN devices is lower than for other existing wireless standards [6]. Table 1 summarizes some key parameters of BLE, IEEE 802.15.4, and IEEE 802.15.6 for the physical layer [3], [10]. From Fig. 2 and Table 1, it can be observed that many low-data rate wireless standards have two key characteristics, which are low-power consumption and short communication distance.

Transistors operated in the subthreshold (or weak inversion) region offer opportunities to minimize power consumption in low-power CMOS RF front-end circuits. Over the past years, some of such LNAs and mixers were reported with very low power consumptions [5] and [11]-[15], which were made possible by high transconductance-to-drain current ratios (g_m/I_D) and low power supply voltages (V_{DD}). However, the prevalent design challenge associated with subthreshold RF front-end circuits has been linearity degradation. For example, in earlier published subthreshold LNAs and mixers [5], [11]-[15]; the third-order intermodulation intercept point (IIP3) is typically equal to or below -10 dBm.

In [16], measurement results were presented for the combination of the subthreshold LNA simulated in [17] and the mixer simulated in [18], demonstrating the feasibility of the proposed design approach. In this extended article, the context has been expanded to include more general subthreshold design

aspects and considerations related to the target applications. Section 2 reviews the characteristics of transistors biased in the subthreshold region. Section 3 summarizes the linearity improvement techniques for the subthreshold LNA and mixer in the discussed RF receiver front-end. Prototype chip measurement results are reported in Section 4, and Section 5 contains conclusions from the work.

2 Subthreshold Operation Characteristics

The key distinguishing characteristics of subthreshold biasing compared to strong inversion biasing are stated below to summarize our prior simulation-based works [17]-[19].

1) Higher power efficiency: transistors biased in subthreshold can provide a higher g_m/I_D ratio than when biased in strong inversion. As can be seen in Fig. 3, power-efficient subthreshold biasing involves the use of gate-to-source (V_{GS}) bias voltages below the threshold voltage (V_{TH}), where the overdrive voltage on the x-axis is $V_{OV} = V_{GS} - V_{TH}$. Hence, the drain-to-source voltage (V_{DS}) can be low (e.g., $V_{DS} > 80$mV) with subthreshold biasing, which permits the use of reduced power supply voltages at the expense of slightly higher noise figure. In Fig. 3, the transconductance can be approximated by $g_m = I_D/(n \cdot V_t)$ when the value of V_{OV} is between -0.2V and 0V, where n is a nonideality factor and $V_t = kT/q$ [20] is calculated from the Boltzmann constant (k), absolute temperature (T), and electron charge (q). However, the transconductance is slightly higher than the approximation when V_{OV} is less than -0.2V in this example. Note that the simulated curves in Fig. 3 were obtained with a device model from the foundry's design kit that includes the resistances of the drain and source, causing minor differences compared to theoretical approximations. Typically, for a given bias current, subthreshold operation requires relatively large transistor width compared to strong inversion operation, but the transconductance is independent of width (at least in a simple analytical approximation) once a device operates in the subthreshold region.

2) Increase of parasitic capacitances and relative changes of their values: In subthreshold mode of operation, the gate-to-source capacitance (C_{gs}) no longer dominates, implying that the gate-to-drain capacitance (C_{gd}) and the gate-to-bulk capacitance (C_{gb}) have to be taken into account for more sophisticated design. As visualized in Fig. 4(a), the simulated C_{gs}/C_{gg} ($C_{gg} = C_{gs} + C_{gd} + C_{gb}$) ratio decreases approximately 20% when g_m/I_D is swept such that the bias point changes from the strong inversion region to the subthreshold region. As a result, C_{gs} no longer dominates in the subthreshold region. Hence, the gate-drain capacitance C_{gd} and the gate-bulk capacitance C_{gb} should be taken into account for precise input impedance matching calculation and linearity estimation. Moreover, to achieve similar transconductance gains as in strong inversion it is required to design with relatively wide transistors, which results in higher parasitic capacitances and lower transition frequency (f_T). Fig. 4(b) shows that the transition frequency f_T changes from 70 GHz to a few GHz when the transistor bias is varied from the strong inversion to the subthreshold region. In the past, transistors biased in subthreshold region were not seriously considered for RF circuit design because f_T was severely limited. However, newer CMOS process technologies have significantly improved f_T values, which has made it possible to design subthreshold circuits with operating frequencies up to several gigahertz using 130nm CMOS and smaller technology nodes.

3) Linearity degradation due to highly positive g_3/g_1, where $g_1 = g_m$ and g_3 is the third-order nonlinearity coefficient: For a weakly nonlinear transistor, the relationship of the small-signal gate-source voltage (v_{gs}) and the drain current (i_d) can be expressed by the first three power series terms [21]-[22]:

$$i_d = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 , \tag{1}$$

where g_1, g_2 and g_3 are the linear gain, second-order nonlinear coefficient and third-order nonlinearity coefficient of the transistor, respectively. Notice that these parameters can be obtained by taking derivatives of the DC drain current (I_D) with respect to the DC gate-source voltage (V_{GS}) at the bias point:

$$g_1 = \frac{\partial I_D}{\partial V_{GS}} \quad , \quad g_2 = \frac{1}{2!}\frac{\partial^2 I_D}{\partial V_{GS}^2} , \quad g_3 = \frac{1}{3!}\frac{\partial^3 I_D}{\partial V_{GS}^3} . \tag{2}$$

Fig. 5 shows the normalized g_2 and g_3 transconductance characteristics of an NMOS transistor with 130nm channel length, where g_2 and g_3 are divided by g_1. The plots reveal that the g_2/g_1 ratio is always positive, but the sign of g_3/g_1 depends on the mode of operation. In the subthreshold region, g_3/g_1 is positive and its value depends strongly on the g_m/I_D ratio. The sign of g_3 transitions from negative to positive when the transistor biasing changes from strong inversion to subthreshold. In addition, the value of g_3/g_1 strongly depends on the g_m/I_D ratio in the subthreshold region.

3 Linearity Enhancement Techniques

In RF front-end circuits, the third-order intermodulation products due to receiver nonlinearities have be minimized to avoid that interference signals corrupt the desired signal. This leads to circuit design challenges, especially when designing with sub-1V supply voltage and sub-mW power consumption with reduced voltage headroom and degraded transistor transconductance values. Consider the scenario in Fig. 6 as example, in which the receiver is designed to receive signals at 1.95 GHz using a local oscillator with a frequency of 1.94 GHz, which results in an intermediate frequency of 10 MHz. However, due to the intermodulation of the interference signals (at 1.96 GHz and 1.97 GHz), an intermodulation distortion signal is created in the same frequency band (around 10 MHz) as the desired signal, and this interference cannot be filtered out by the band-pass filter (or low-pass filter) after the mixer. The ongoing improvements of filters with high quality factors after the antenna can help to attenuate the interferences at the low-noise amplifier input. However, it is difficult to realize on-chip high-Q filters due to the low quality factors of inductors in CMOS technologies, and off-chip components would create extra cost and would increase the printed circuit board (PCB) size of portable wireless devices. Passive mixer-first structures have been proposed for enhanced RF filtering and high linearity [23]-[24], especially in combination with oversampling. However, the local oscillator (LO) signal generation for such architectures is more complicated and consumes more power compared to conventional low-power receiver designs.

The IIP3 of mixers is typically more critical than their noise figure, since mixers are often the bottleneck of the RF front-end linearity. Fig. 7 displays a Gilbert mixer without tail current source to save voltage headroom. For subthreshold operation, M_1-M_3 should be designed with high W/L ratios to realize the same g_m as that in strong inversion. Hence, the mixer would suffer from significant conversion gain loss due to AC current leakage through the total parasitic capacitance (C_P) at the sources of the LO transistors, as well as relatively high distortion from the transconductance stage (M_1). In previous work [18] (Fig. 8), an inductor was inserted between each drain of the RF transistors and the common source node of the LO transistors to resonate with C_p, and a g_m-boosting structure was introduced with inductive degeneration for the RF transistors and cross-coupling capacitors between the source of one RF transistor and the drain of the RF transistor in the other branch. Post-layout simulations of the mixer in [18] resulted in an IIP3 of 6.7 dBm, a voltage gain of 8.6 dB, and a single-sideband noise figure of 19.2 dB with a power consumption of 0.423 mW and a layout area of 0.745 mm^2. A key aspect of this IIP3 enhancement method with nonlinearity cancellation is that g_3 and g_1 of the RF transistors have same sign because of the subthreshold biasing, while inductors and cross-coupling capacitors are used to cancel C_p and boost the conversion gain.

Fig. 9 displays the schematic of the differential RF front-end with LNA (consisting of transistors M_1-M_4) and mixer (consisting of transistors M_5-M_{10}). The extra passive components (inductors L_{g2}, L_1, L_2 and capacitor C_{gd2_ext}, C_c) improve the IIP3 as explained next. Fig. 10 depicts the small-signal model of the LNA input stage with three terminal impedances: Z_1, Z_2, and Z_3 signify the impedances when looking out from the gate, source and drain of the transistor, respectively. The IIP3 of the input stage can be derived with Volterra series analysis [25]-[26] as

$$IIP3 = \frac{1}{6R_s \cdot |H(\omega)| \cdot |A(\omega)|^3 \cdot |\varepsilon(\Delta\omega, 2\omega)|}, \tag{3}$$

where ω is the center frequency of the two intermodulation tones at ω_{RF1} and ω_{RF2}, $\Delta\omega$ is defined as $|\omega_{RF1} - \omega_{RF2}|$, and R_s is the antenna impedance of 50 Ω. $H(\omega)$ is the third-order nonlinearity transfer function from V_{in} to the drain-source current (i_d) of the transistor (M_1), $A(\omega)$ is the linear transfer function from the input

voltage (V_x) to the gate-to-source voltage (V_{gs}), and $\varepsilon(\Delta\omega,2\omega)$ represents the nonlinear contribution from the second-order and third-order terms of the transistor in the input stage. Minimization of $\varepsilon(\Delta\omega,2\omega)|$ in (3) leads to improved IIP3. Note that this approach cancels third-order intermodulation distortion under the impact of the second-order contribution, which does not necessarily imply that second-order intermodulation distortion is simultaneously canceled. The $\varepsilon(\Delta\omega,2\omega)$ term of M_1 can be expressed as

$$\varepsilon(\Delta\omega,2\omega) = g_3 - g_{oB} \ , \tag{4}$$

where:

$$g_{oB} = \frac{2}{3} g_2^2 \left[\frac{2}{g_1 + g(\Delta\omega)} + \frac{1}{g_1 + g(2\omega)} \right], \tag{5}$$

$$g(\omega) = \frac{\begin{array}{l} 1 + j\omega C_{gd} \cdot [Z_1(\omega) + Z_3(\omega)] \\ + j\omega C_{gs} \cdot [Z_1(\omega) + Z_2(\omega)] \\ + j\omega C_{gb} \cdot [1 + j\omega C_{gd} Z_3(\omega)] \cdot Z_1(\omega) \end{array}}{Z(\omega)}, \tag{6}$$

$$\begin{array}{l} Z(\omega) = Z_2(\omega) + j\omega C_{gb}[1 + j\omega C_{gd} Z_3(\omega)] Z_1(\omega) Z_2(\omega) \\ + j\omega C_{gd}[Z_1(\omega) Z_2(\omega) + Z_1(\omega) Z_3(\omega) + Z_2(\omega) Z_3(\omega)] \end{array}. \tag{7}$$

For the input stage of the LNA, Z_1-Z_3 can be expressed as

$$Z_{1,\mathrm{LNA}}(\omega) = R_s + j\omega L_{g1}, \tag{8}$$

$$Z_{2,\mathrm{LNA}}(\omega) = j\omega L_s \ , \tag{9}$$

$$Z_{3,LNA}(\omega) = \frac{1 + j\omega C_{gd3} Z_3(\omega) + [j\omega C_{gs3} + j\omega C_{gd3} - \omega^2 C_{gs3} C_{gd3} Z_d(\omega)] \cdot Z_{22}(\omega)}{g_{1,M3} + j\omega C_{gs2} + [j\omega C_{gd3} g_{1,M3} - \omega^2 C_{gd3} C_{gs3}] \cdot [Z_{22}(\omega) + Z_d(\omega)]}, \tag{10}$$

where the combined impedances are:

$$Z_{22}(\omega) = (j\omega L_{g2}) // (j\omega C_{gb3})^{-1} \tag{11}$$

and

$$Z_d(\omega) = R_d // (j\omega L_d) // (j\omega C_d)^{-1} . \tag{12}$$

For the input stage of the mixer, Z_1-Z_3 can be expressed as

$$Z_{1,mixer}(\omega) = (1/(R_s/2) + j\omega C_{gb5})^{-1}, \tag{13}$$

$$Z_{2,mixer}(\omega) = (1/(j\omega L_1) + j\omega C_c(1 + K(j\omega)))^{-1}, \tag{14}$$

$$Z_{3,mixer}(\omega) = (1/(Z_{M3}) + j\omega C_c(1 + 1/K(j\omega)))^{-1}, \tag{15}$$

where

$$Z_{M3}(\omega) = j\omega L_2 + \frac{1}{g_{m7} + j\omega_{RF}(C_{gs7} + C_{gs8})} \tag{16}$$

and

$$K(\omega)=\frac{v_d(\omega)}{v_s(\omega)}=\frac{g_{m5}(j\omega C_{gd5}-2j\omega C_c-\frac{1}{j\omega L_1})+\frac{C_{gd5}}{L_1}-\omega^2(C_{gs5}C_{gd5}+C_{gd5}C_c-C_{gs5}C_c)}{g_{m5}(j\omega C_{gd5}+2j\omega C_c+\frac{1}{Z_{M3}})+\frac{j\omega C_{gs5}}{Z_{M3}}-\omega^2(C_{gs5}C_{gd5}+C_{gs5}C_c-C_{gd5}C_c)}. \quad (17)$$

As described in [17] and [18], the impedances Z_1, Z_2 and Z_3 of the LNA and mixer input stages can be designed to minimize $|\varepsilon(\Delta\omega,2\omega)|$. Fig. 11(a) visualizes that the mechanism of the partial third-order intermodulation cancellation in (4) entails changing the magnitude and phase of g_{oB} in (5) such that they are almost identical to those of g_3, where g_{oB2} represents a better design point (with more cancellation of g_3) than g_{oB1} as result of different parameters. Fig. 11(b) was obtained with the proposed LNA as a design example, where L_{g2} and C_{gd2_ext} (Fig. 9) are the design parameters that strongly impact equations (4)-(10). From Fig. 11(b), it can be observed that sweeping the value of L_{g2} with different C_{gd2_ext} values allows to minimize $|\varepsilon(\Delta\omega,2\omega)|$ in (4). We have proposed this design approach in our previous works together with theoretical analyses and simulation results. The next section introduces proof-of-concept measurement results from an RF front-end that combines the LNA and mixer architectures from [17] and [18]. The noise factor analysis for the subthreshold common-source LNA with inductive source degeneration has been reported in [27] with the following result:

$$F=1+C_t^2\times\frac{\omega_o^2R_s\gamma n^2V_T}{I_D}\left[\frac{\delta\alpha^2}{5\gamma}\left(1+Q_{in}^2\right)\frac{C_{gs1}^2}{C_t^2}+1-2|c|\frac{C_{gs1}}{C_t}\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right], \quad (18)$$

where $C_t = C_{gs1} + C_{gs1\_ext}$, ω_0 is the operating frequency, γ and δ are the channel and gate noise coefficients, $\alpha = g_{1,M1}/g_{d0,M1}$, $g_{d0,M1}$ is the channel conductance with zero drain-source voltage, V_T is the thermal voltage, Q_{in} is the quality factor of the input matching network, and c is the correlation parameter between the gate and channel noise currents.

4 Measurement Results

A low-power linearized RF receiver front-end (Fig. 9) was designed using subthreshold biasing, and fabricated in Dongbu 0.11μm CMOS technology with an RF frequency of 1.95 GHz (second tone in the two-tone tests at 1.948 GHz) and an LO frequency of 1.96 GHz. Down-conversion to a frequency of 10 MHz is helpful to alleviate the impact of flicker noise. Table 2 lists the important parameters of the

LNA and mixer designs. Fig. 12 visualizes the test setup for the RF front-end, which consumes 1.5 mA of current from a 0.6 V power supply instead of the nominal 1.2 V supply voltage in 0.11µm CMOS technology. As shown in Fig. 13, the prototype die was bonded to a conventional QFN24 package that was assembled on a printed circuit board (PCB) for measurements. Fig. 14 displays the chip micrograph of the pseudo-differential LNA and mixer with a total area of 1.5 mm × 1.1 mm.

Fig. 15 displays the measured S11 parameter of the linearized subthreshold RF front-end. Its value is below -10 dB at 1.95 GHz. Fig. 16 shows the measured IIP3 performance of the front-end, and the output spectrum from a test with a two-tone input signal having a power of -36.5 dBm. In Fig. 16(a), the third-order curve of the proposed topology demonstrates that significant third-order distortion cancellation occurs in the weakly nonlinear regime (input power below -30 dBm). With larger input power levels, the higher-order distortion terms and strong nonlinearities with subthreshold biasing reduce the effectiveness of the cancellation [21]. Fig. 17 shows the plot of output power measurements from a power level sweep of a single 10 MHz tone to determine the 1-dB compression point (P_{1dB}) of the front-end. The IIP3 and P_{1dB} of the subthreshold RF front-end are -10.8 dBm and -22.7 dBm, respectively. After de-embedding the effects of the losses (9.5 dB) due to the loading at the output, the overall voltage gain of the front-end based on the measured transient output voltage in Fig. 18 is 20.6 dB. Fig. 19 displays the plot of the measured double sideband noise figure (NF_{DSB}) that is 14 dB at 10 MHz with the input balun. After de-embedding the effect of the input balun loss (5.5 dB), the double sideband noise figure of the RF front-end is 9.5 dB at 10 MHz.

Table 3 summarizes the performance of low-power narrowband RF front-ends with operating frequencies ranging from 1.95 GHz to 5.1 GHz. The presented design in 130nm CMOS technology exhibits a combination of high linearity with low power consumption and adequate noise figure. However, the relatively high number of inductors in the architecture creates a layout area tradeoff. The pseudo-differential LNA stage in this work has the benefit of creating robustness to phase shift imbalances. On the other hand, the designs in [28]-[30] include single-ended LNAs, which saves power. The design in [33] contains a complete RF front-end including

a two-stage LNA, mixer and voltage-controlled oscillator (VCO), while only consuming 0.382mW with 0.18V supply in 28nm CMOS technology. The low-power transceiver in [34] has a voltage gain of 46dB, an IIP3 of -33dBm, and a power consumption of 8.52 mW for its receiver in 90nm CMOS technology.

5 Conclusion

This paper described the low-power and low-voltage characteristics of designing RF receiver front-end circuits using transistors biased in the subthreshold region under consideration of tradeoffs related to parasitic capacitances, linearity, and layout area. The example front-end design consisted of a linearized low-noise amplifier and mixer, which were combined within a 1.95 GHz subthreshold RF receiver front-end that was fabricated and tested in 0.11μm CMOS technology. The applied linearization techniques employ extra passive components to accomplish partial cancellation of third-order nonlinearity products, which was demonstrated through prototype chip measurements. The RF front-end has an IIP3 of -10.8 dBm, a voltage gain of 20.6 dB, and a double sideband noise figure of 9.5 dB with a power consumption of 0.9 mW from a 0.6 V supply.

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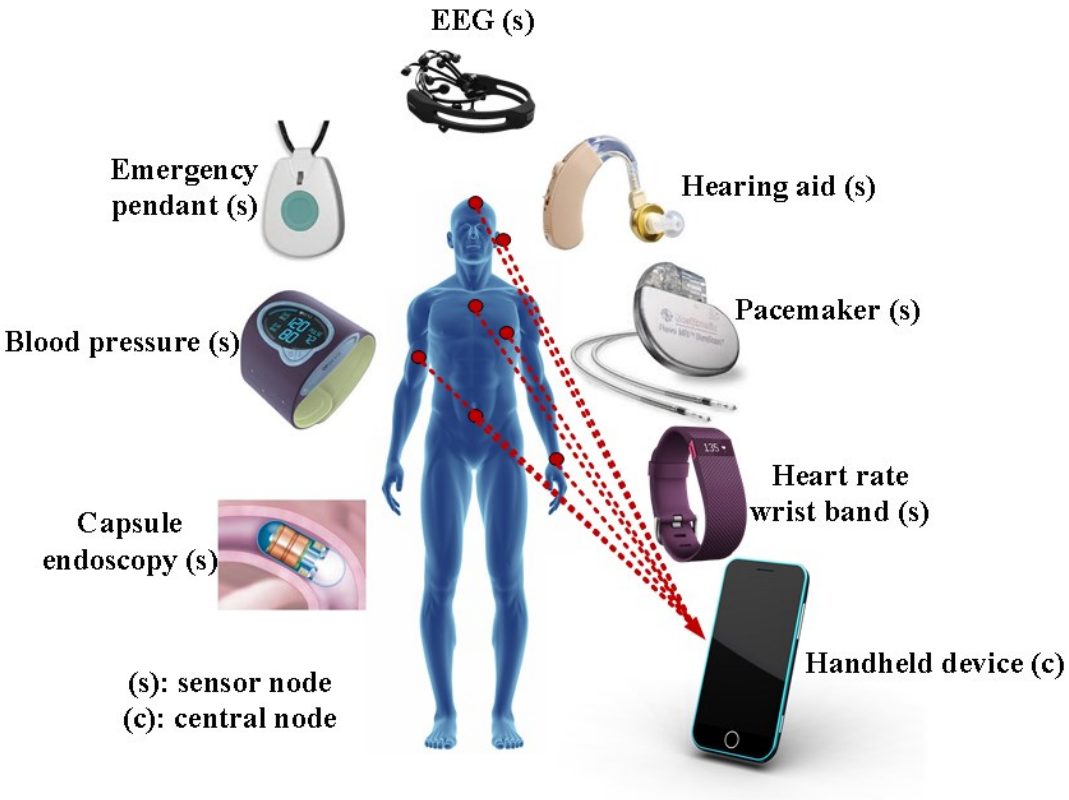


Fig. 1. WBAN example for medical applications.

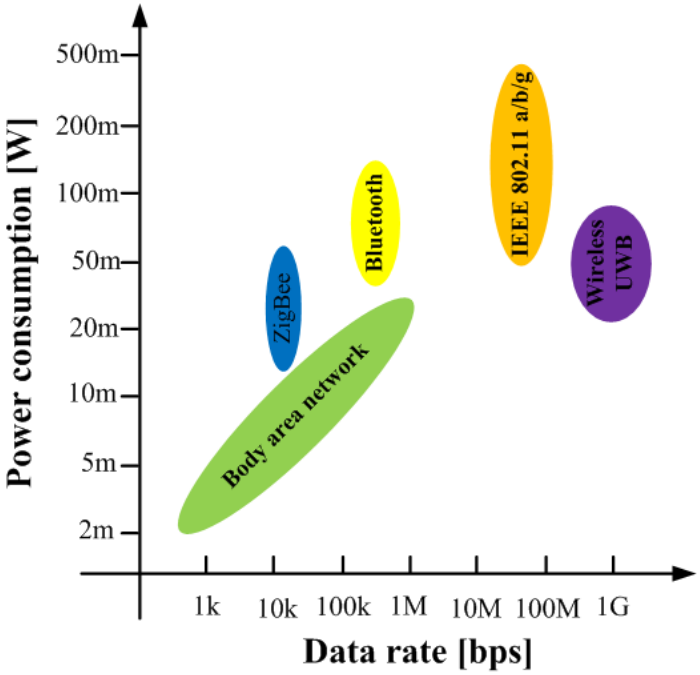


Fig. 2. Comparison of power consumption vs. data rate for various wireless standards (data from [6]).

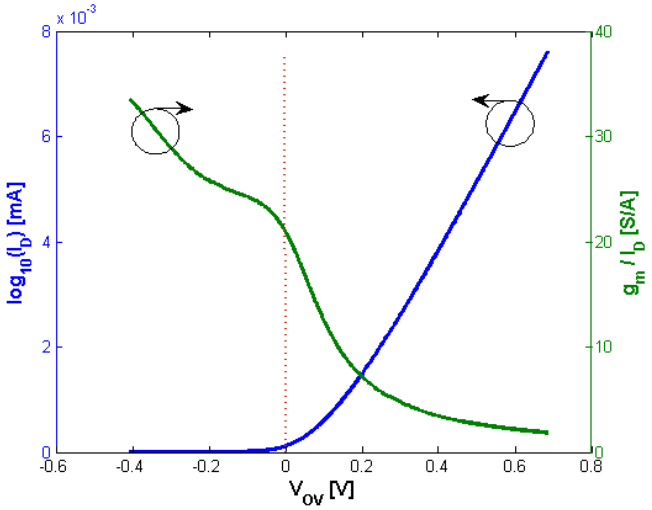
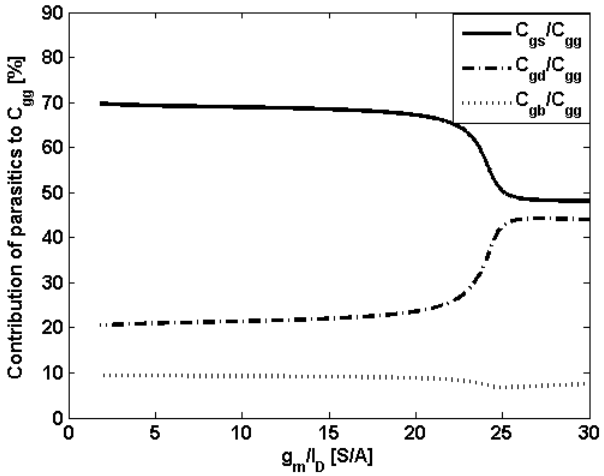
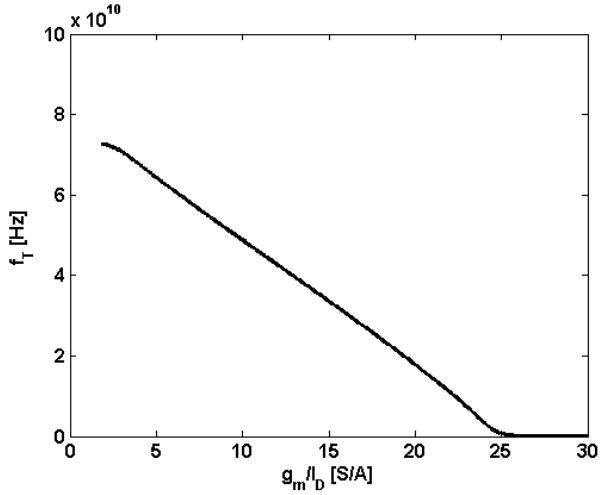


Fig. 3. Drain current (I_D) with logarithmic scale and current efficiency (g_m/I_D) vs. overdrive voltage (V_{OV}) of an NMOS transistor with 130nm channel length.



(a)



(b)

Fig. 4. (a) Contribution of parasitic capacitances to the total gate capacitance (C_{gg}) vs. g_m/I_D; (b) transition frequency (f_T) vs. g_m/I_D of an NMOS transistor with 130nm channel length.

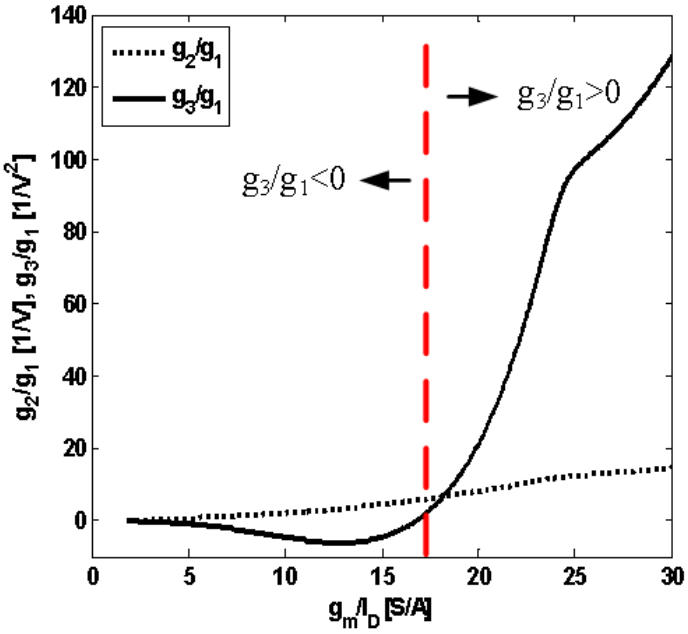


Fig. 5. Normalized second-order (g_2) and third-order (g_3) transconductance characteristics of an NMOS transistor with 130nm channel length.

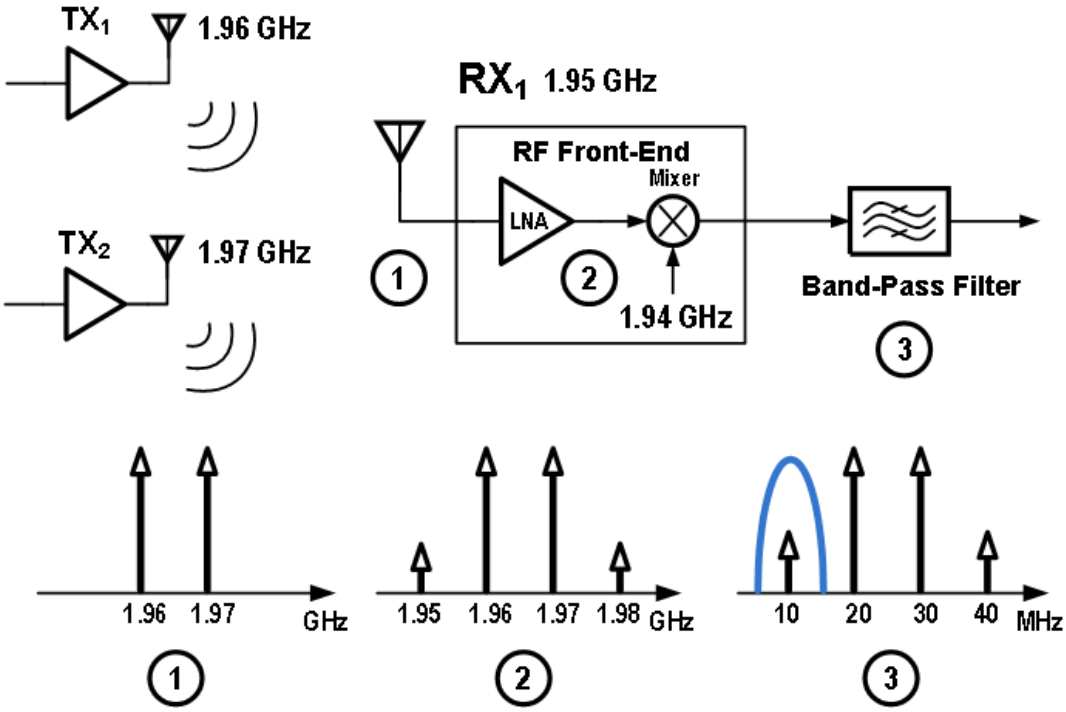


Fig. 6. The effect of intermodulation distortion due to the presence of multiple transmitters (TX).

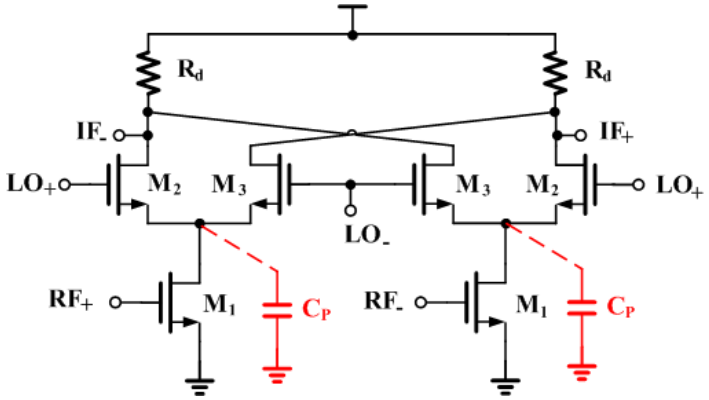


Fig. 7. Conventional mixer with annotated parasitic capacitance C_P.

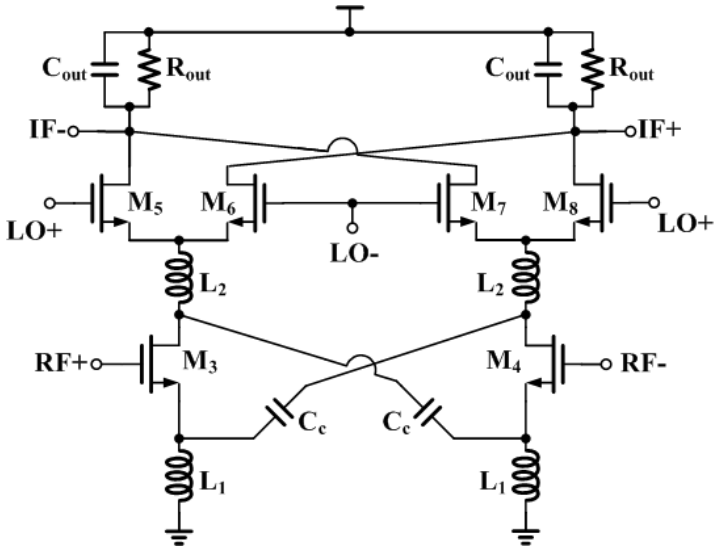


Fig. 8. Linearized mixer with inductors and cross-coupling capacitors in [18].

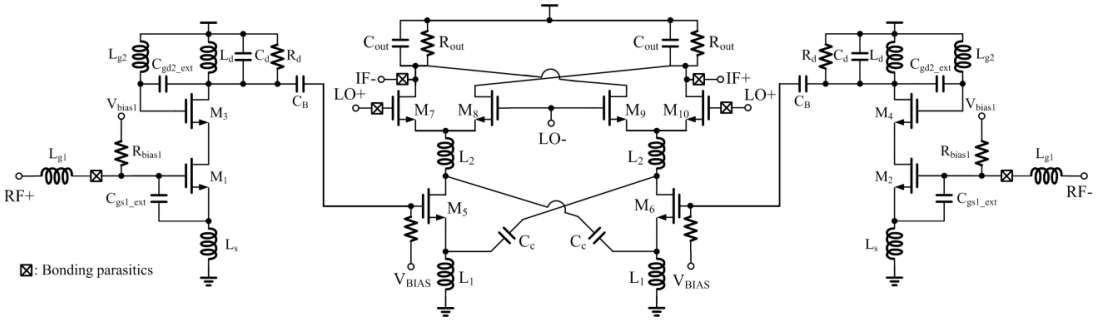


Fig. 9. Schematic of the linearized subthreshold RF front-end circuit with pseudo-differential LNA and mixer.

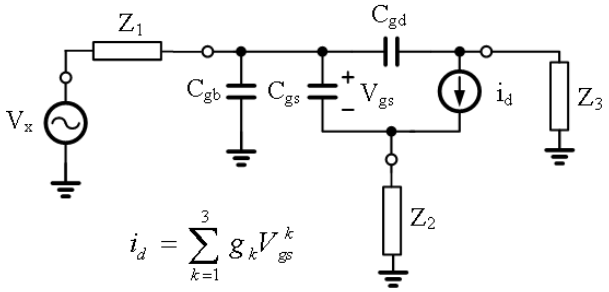
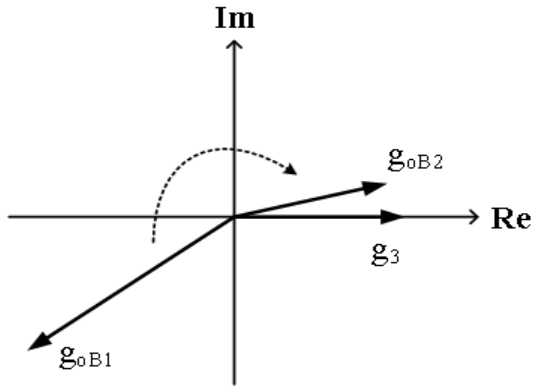
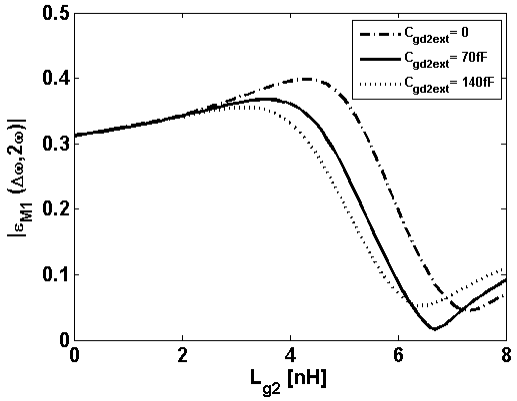


Fig. 10. Small-signal model of a common-source amplifier with nonlinear drain-to-source current.



(a)



(b)

Fig. 11. (a) Vector diagram of the third-order intermodulation cancellation, where g_{oB1} and g_{oB2} are g_{oB} realizations in (4) with different design parameters; (b) sweeps of the L_{g2} value for different C_{gd2_ext} values to minimize $|\varepsilon(\Delta\omega,2\omega)|$ for an example LNA design.

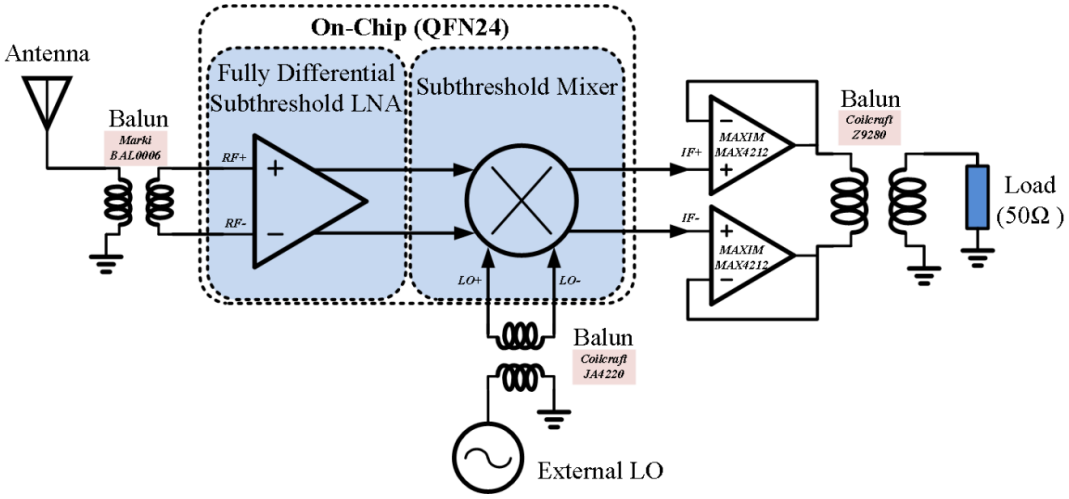


Fig. 12. Block diagram of the RF front-end measurement setup.

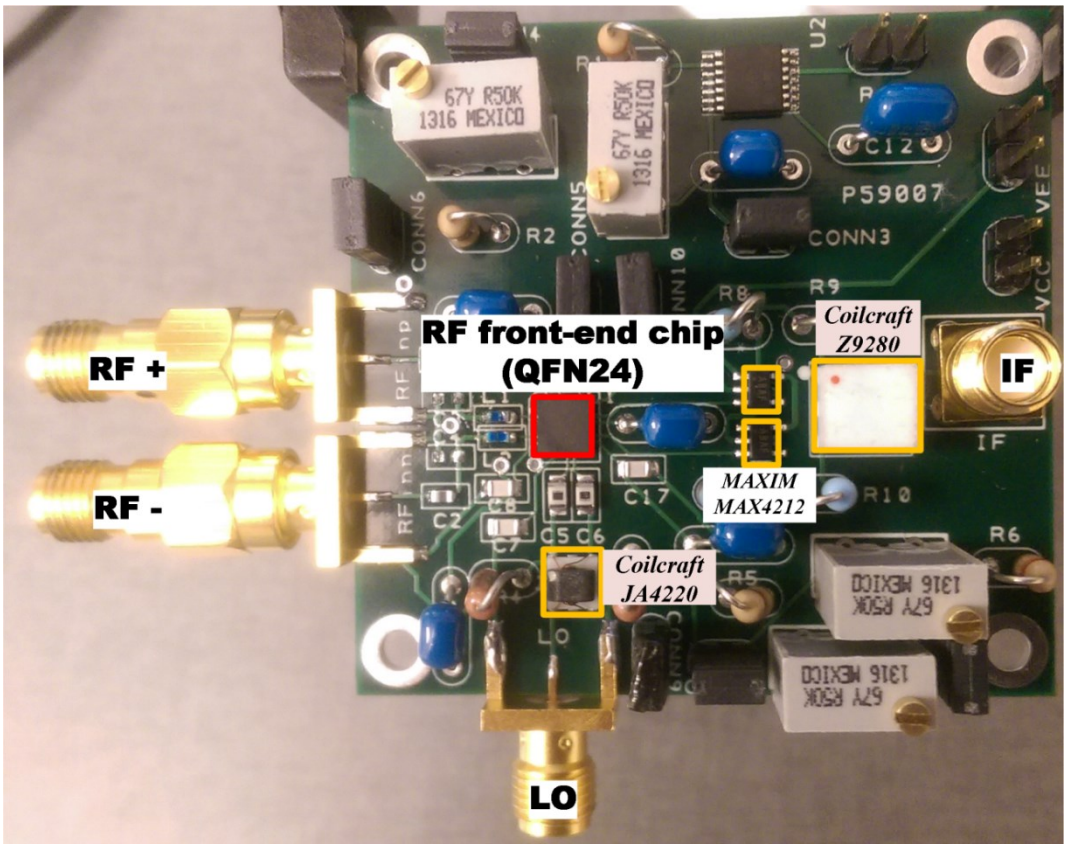


Fig. 13. PCB for RF front-end testing.

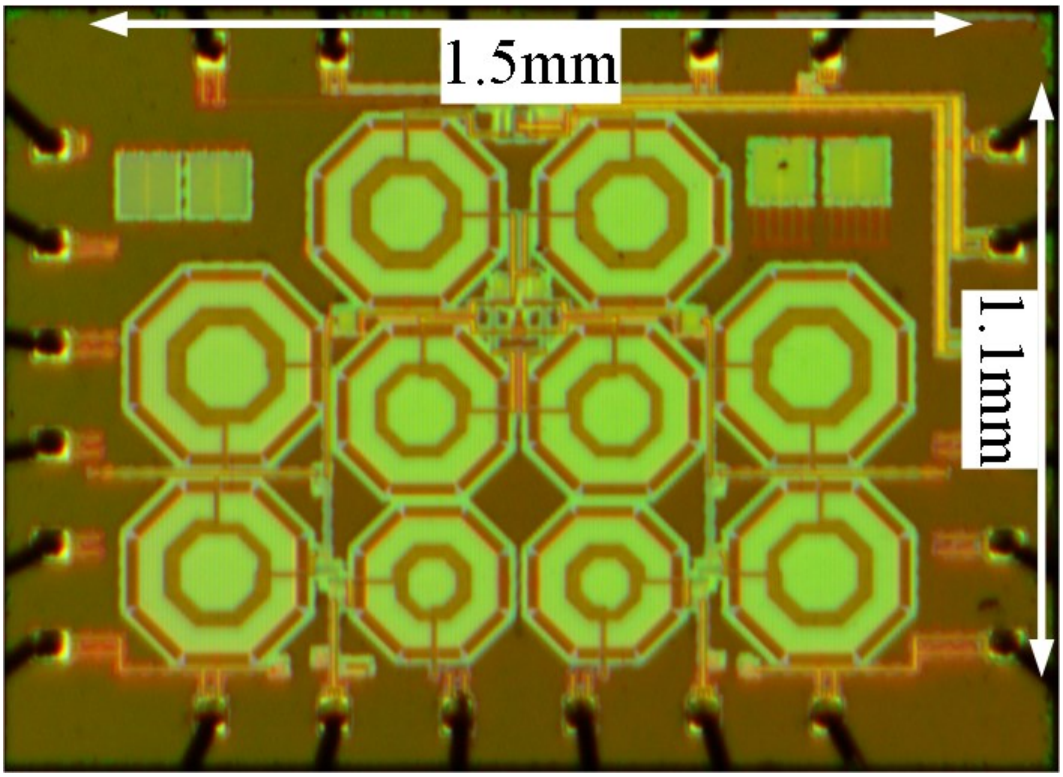


Fig. 14. Chip micrograph of the fabricated linearized subthreshold RF front-end in Dongbu 0.11μm COMS technology.

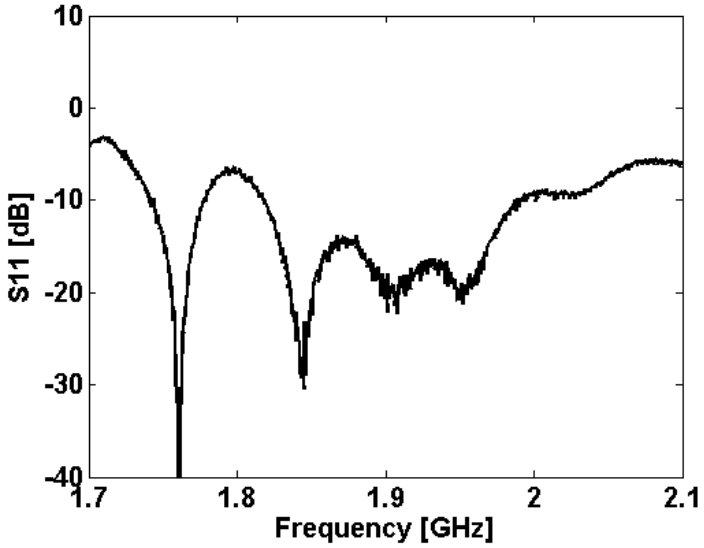
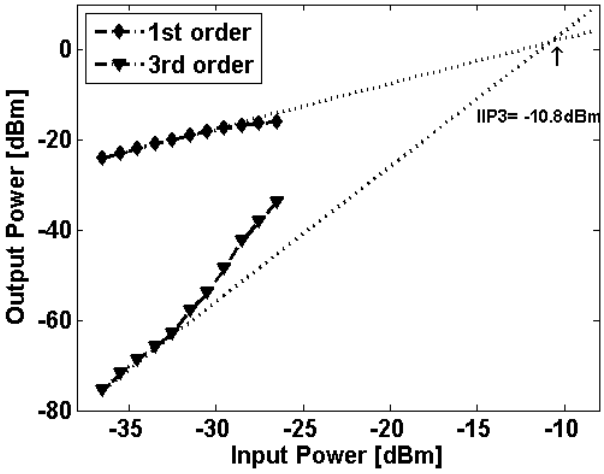
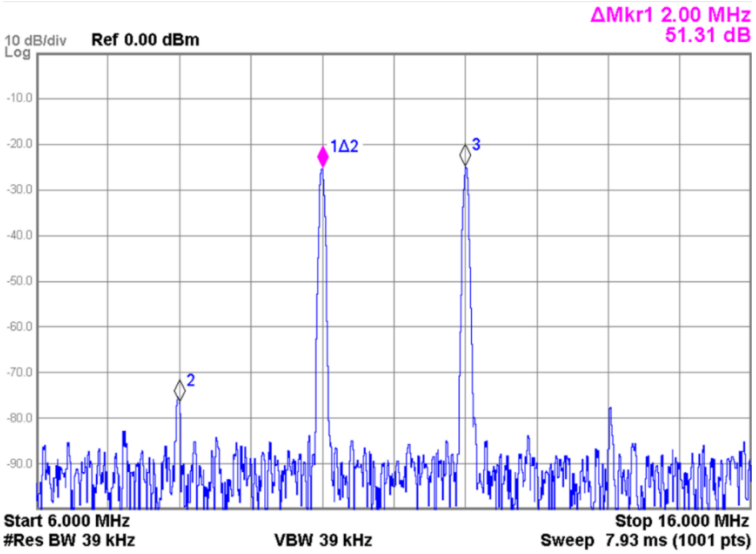


Fig. 15. Measured S11 of the RF front-end.



(a)



(b)

Fig. 16. (a) Measured IIP3 of the RF front-end with balun (9.5dB loss), (b) output spectrum from a test with two tones at 10 MHz and 12 MHz and an input power of -36.5 dBm.

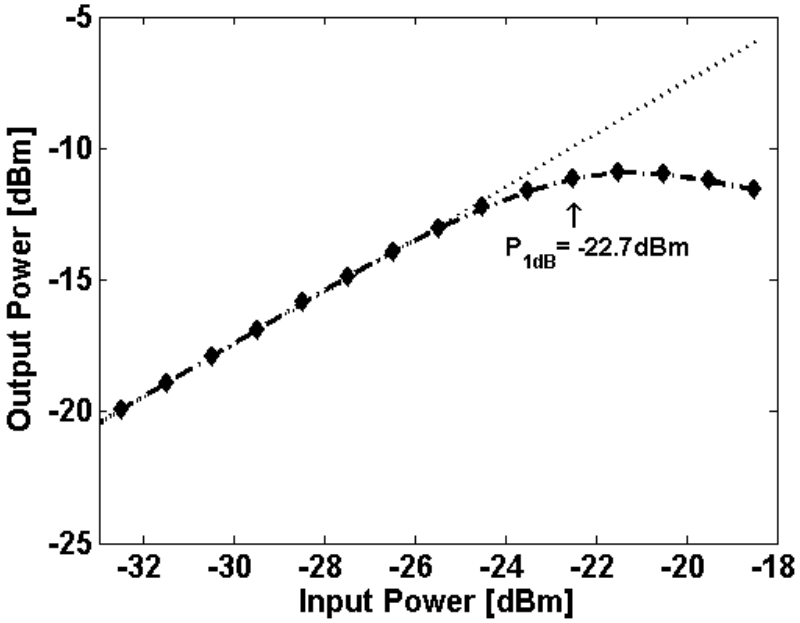


Fig. 17. Measured 1-dB compression point of the RF front-end with input and output baluns (at IF = 10 MHz).

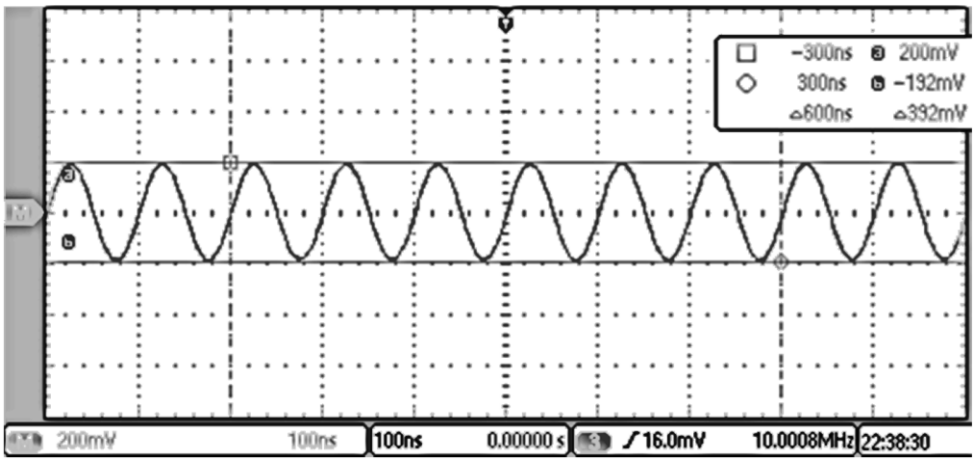


Fig. 18. Measured output amplitude before the output balun.

Fig. 19. Measured NF_{DSB} of the RF front-end (IF = 10 MHz).

Table 1. Examples of low-power wireless communication standards

	Wireless Personal Area Network (WPAN)		Wireless Body Area Network (WBAN)
	Bluetooth Low Energy (BLE)	IEEE 802.15.4 (ZigBee)	IEEE 802.15.6
Frequency range	2.4-2.4835 GHz	2.4 GHz, 868 MHz, 915 MHz,	2.4-2.2483 GHz, 2.36-2.4 GHz (US), (400/868/915/950 MHz)
Data rate	1 Mbps	20 Kbps - 250 Kbps	75.9 Kbps - 971.4 Kbps
Network size	Undefined	Up to 65536 devices	Up to 256 devices
Range	10-75 m	10-100 m	2-5 m

Table 2. Design parameters of the RF front-end circuits

LNA	
V_{DD}	0.6 V
I_D	875 µA
L_{g1}	6.2 nH
L_{g2}	3.5 nH
L_s	2.4 nH
C_{gs1_ext}	130 fF
C_{gd2_ext}	150 fF
L_d	6.4 nH
C_d	88 fF
R_d	720 Ω
W/L per finger ($M_{1,2,3,4}$)	6µm / 0.13µm
Number of fingers ($M_{1,2,3,4}$)	64
Mixer	
V_{DD}	0.6 V
I_D	625 µA
L_1	2.7 nH
L_2	5.8 nH
C_c	337 fF
C_{out}	1178 fF
R_{out}	1 KΩ
W/L per finger ($M_{5,6}$)	6µm / 0.13µm
Number of fingers ($M_{5,6}$)	64
W/L per finger ($M_{7,8,9,10}$)	5.8µm / 0.13µm
Number of fingers ($M_{7,8,9,10}$)	64

Table 3. Comparison of low-power RF front-ends

	THIS WORK	[28]*#	[29]#	[30]#	[31]	[32]	[33]◊#	[34]&
f_{RF} [GHz]	1.95	5.1	2.4	2.445	2.4	2.4	2.4	2.4
f_{IF} [MHz]	10	10	2	10	2	2	1	1
P_{LO} [dBm]	-9	-5	n/a	n/a	n/a	n/a	n/a	n/a
S11 [dB]	-20	n/a	-17	n/a	<-16	-9	< -7.5	n/a
Gain [dB]	20.6	27	20.5	30	55.5	32	34.5	46
NF_{DSB} [dB]	9.5	16	10.2	7.5	15.	8.8	11.3	5.5
IIP3 [dBm]	-10.8 (IB)	-3 (IB)	-7.8 (IB)	-16.2 (IB)	-15.8 (OOB)	-7 (OOB)	-12.5(OOB)	-33(OOB)
P_{1dB} [dBm]	-22.7	n/a	-20	-26	n/a	n/a	n/a	n/a
P_{DC} [mW]	0.9	1	1.08	4.68	0.6	1.4	0.382	8.52
Tech. [nm]	110	180	180	90	130	65	28	90
Area [mm^2]	1.65$	0.856‡	1.69‡	0.74$	0.25$	1.4$	1.65‡	1.95‡^

* passive mixer # single-ended LNA

◊ includes on-chip voltage-controlled oscillator (VCO) & includes on-chip VCO with a phase-locked loop (PLL)

$ without pads ‡ with pads ^ with transmitter

IB = in-band OOB = out-of-band