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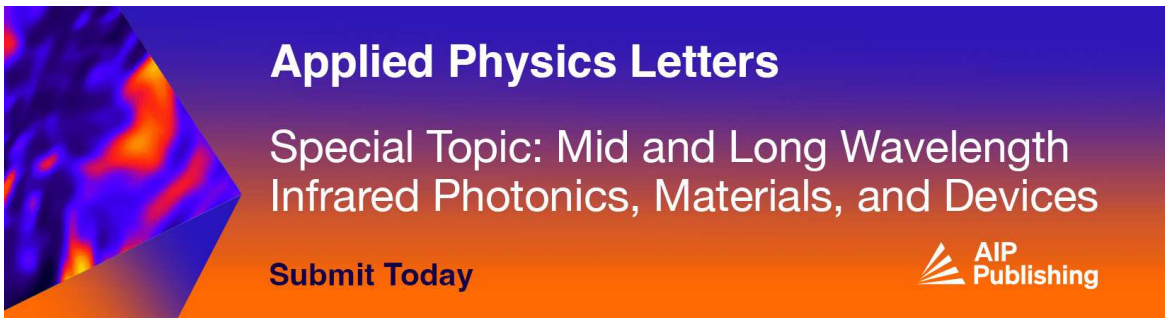

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Experimental demonstration of an electroacoustic transistor

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ABSTRACT

We experimentally demonstrate a topologically protected electroacoustic transistor. We construct a reconfigurable phononic analog of the quantum valley-Hall insulator composed of electrically shunted piezoelectric disks bonded to a patterned plate forming a monolithic structure. The device can be dynamically reconfigured to host one or more topological interface states via breaking inversion symmetry through selective powering of shunt circuits. Above a threshold, the amplitude of wave energy at a chosen location in one topological interface creates a second interface by dynamically switching power between two groups of shunts using relays. This enables the flow of wave energy between two locations in the reconfigured interface analogous to the voltage-controlled electron flow in a field effect transistor. The amplitude of wave energy in the second interface is used for bit abstraction to implement acoustic logic. We illustrate the various states of the transistor and experimentally demonstrate wave-based switching. The proposed electroacoustic transistor is envisioned to find applications in wave-based devices and edge computing in extreme environments and inspire novel technologies leveraging acoustic logic.

The growing need for low power, high speed devices for applications in industry internet of things (IIoT) coupled with the challenges of system complexity in analog-to-digital conversion in electronic integrated circuits has led to a renewed interest in analog computing.[1,2] Photonic and phononic metamaterials have been proposed to achieve high throughput, ultrafast responses in wave-based computations[3–5] demonstrating superiority over their mechanical counterparts.[2] Of particular interest are devices capable of performing logical operations while being an integral part of a structure or robot deployed at the edge of a network (referred to as edge computing),[6,7] especially in extreme environments. Such devices can augment (or fully replace) existing electronics to pave the way to hybrid technologies with greater speed, performance, and energy efficiency. For instance, a hybrid electrical–mechanical system may be employed for remote implementation of logic in surroundings with relatively high temperature by exposing the structural components to interact with the surroundings while thermally isolating the electrical components.

While mechanical means to achieve Boolean logic have been demonstrated using multistable soft structures,[8] conductive mechanical materials,[9] and micro/nanoelectromechanical systems (M/NEMS),[10,11] these are known to be limited by one or more factors, such as speed, scalability, flexibility in setting up computing rules, ability to return to their original state, or functional-completeness. Acoustic systems where the information is carried via waves offer significantly higher speeds and therefore faster processing. Acoustic analogs to electronic switches have been reported in the literature using compressible/soft[12–14] and granular[15] media. Acoustic logic has been proposed using density-near-zero metamaterials,[16] phase modulation,[17] self-collimated beams,[18] and shunted piezoelectric-based membrane-type metamaterial.[19] However, the lack of reconfigurability and the need for separate acoustic structures for different logic are major limitations in these designs. Furthermore, it is essential for the accuracy of the information being carried that these wave-based devices be robust to disorder or fabrication defects. Recently demonstrated reconfigurable acoustic topological insulators (TIs)[20,21] offer a promising platform to overcome the aforementioned limitations. Acoustic or elastic TIs,[22–24] similar to photonic TIs,[25,26] are enabled by classical analogs of the quantum Hall, spin-Hall, and valley-Hall effects and are observed in systems with broken symmetries such as time reversal and spatial inversion.[27–30] Specifically, in the context of elastic waves in plate-like systems, topological interface modes have been realized using various designs, such as patterned plates,[31–33] mesh-like lattices[34–36] and lattices with localized masses[37] and acoustic black holes.[38] Acoustic edge or interface states localized at the boundaries

of symmetry-protected phases of acoustic TIs are known to be robust to disorder and exhibit low backscattering. Although the degree of robustness may vary between different types of TIs,[39] the waveguiding offered is superior to conventional waveguides.[40] These features along with dynamic reconfigurability[20] and the scope of miniaturization[41] make TIs optimal platforms for developing wave-based logic devices.[36,42]

In recent literature, reconfigurability in phononic metamaterials has been achieved using external force in soft matter,[13] electric shunting of piezoelectric media,[43–45] magnetic interaction,[46,47] and liquid-[48] and light-induced[49] response, among others.[50] Particularly, topological phononic logic has been demonstrated by reconfiguring the geometry of TIs by utilizing thermal expansion due to ultrasonic heating[51] and through programmed actuation of solenoids.[21] However, these designs reconfigure on relatively slow time scales and involve one or more moving parts. Altering material properties is another approach to reconfigurability in topological systems and has been demonstrated using piezoelectric media and active shunt circuits.[20,52] Using a similar platform, we recently proposed and numerically modeled the response of an electroacoustic transistor.[53] Here, we experimentally demonstrate the topologically protected electroacoustic transistor in which a wave input through a topological interface switches a wave output at a second topological interface. This is analogous to a field effect transistor (FET) where a voltage above a threshold when applied at the gate terminal results in a conductive region between source and drain terminals enabling current flow.[54] In the electroacoustic transistor, the current is replaced by elastic waves. A wave at a gate terminal located in a topological interface switches off or on the wave propagation between a source terminal and a drain terminal located in a second topological interface, as illustrated in Figs. 1(a) and 1(b). Our goal is to obtain such an acoustic switching behavior in a relatively small lattice without crosstalk. To this end, we consider a 10×6 lattice with two possible output states: OFF and ON. The amplitude of the acoustic wave can be used for bit abstraction such that value above (below) a set threshold is defined as a logical high (low). Similar to a FET, a wave amplitude above the set threshold at the gate enables a topological waveguide such that waves generated by a second input at the source propagate to the drain. Although a similar device may be possible using conventional waveguides such as an array of shunted PZT disks bonded to a plate, the acoustic energy in such a device is easily dissipated through geometric spreading. Topology of the phonon bands offers superior localization and protection against fabrication disorders

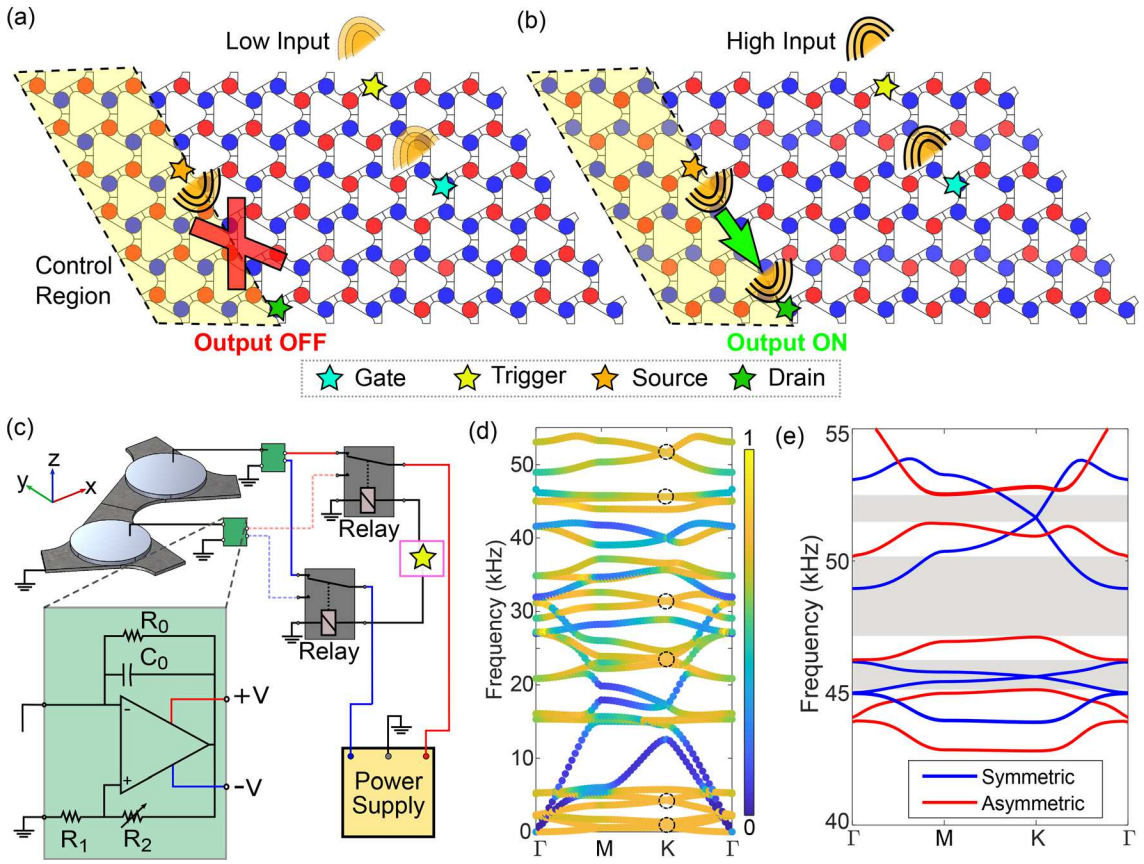

FIG. 1. Schematic illustration of the topologically protected electroacoustic transistor in the (a) OFF and (b) ON states. (c) Representative unit cell of the transistor along with negative capacitance shunt circuits powered via mechanical relays. (d) Band structure of the unit cell with both PZT disks open-circuited. The colorbar indicates the out-of-plane (z-direction) polarization of the eigenmodes. Dirac points (circled in black) can be identified at several frequencies for modes with predominant z-displacement of the structure. (e) Band structure for unit cells with (blue) and without (red) inversion symmetry highlighting multiple complete bandgaps (gray).

while ensuring robust device output and minimal crosstalk. We believe the proposed electroacoustic transistor is a stepping stone toward achieving advanced wave-based logic that may find useful applications in edge computing, particularly in harsh environments, and will complement the existing capabilities of SAW devices such as switching and filtering in communication and network infrastructure.

The proposed transistor is a monolithic structure constructed by bonding piezoelectric (PZT) disks to a patterned aluminum plate forming a hexagonal phononic lattice with a unit cell size, $a = 0.045$ m (refer to Sec. S1 of the supplementary material for unit cell geometry). Similar to a FET, we identify gate, source, and drain terminals in the device. These are the PZT disks marked with cyan, orange, and green stars, respectively, in Figs. 1(a) and 1(b). The signal at the "trigger" marked by the yellow star is used to switch the state of the device as explained later. To enable reconfigurability, the two PZT disks in the transistor unit cell are shunted via negative capacitance (NC) circuits built using an operational amplifier (OpAmp),[54] one of which is supplied electrical power through mechanical relays depending on the trigger signal as illustrated in Fig. 1(c). Actuating the relays allows swapping the shunt status of the PZT disks in the unit cell. For the device functioning, such a swapping is needed only within the control region in Figs. 1(a) and 1(b). In the remainder of the transistor, the shunt status of the PZT disks remains unchanged and we fix (i.e., without using relays) the electrical termination as shunted or open-circuit, as necessary for establishing the required topological interfaces.

The NC circuit used in our experiments effectively reduces the elastic modulus of the shunted PZT disks. The details of the circuit implementation and estimated elastic modulus are provided in the supplementary material (Sec. S1). When both the PZT disks have the same shunt configuration (for example, both are open-circuited) the hexagonal lattice has both C_3 and inversion symmetry. The unit cell band structure is computed by solving an eigenvalue problem (EVP) formulated by applying Bloch boundary conditions in a finite element[55] model of the system (refer to Sec. S2 of the supplementary material). The band structure contains Dirac degeneracies[56,57] at the K-point in the Brillouin zone (BZ) at multiple frequencies encircled (black) in Fig. 1(d). The colorbar indicates the extent of out-of-plane (z-direction) polarization such that 0 indicates a completely in-plane displacement field and 1 indicates a fully out-of-plane displacement field in the eigenmode. To obtain an elastic valley-Hall topological insulator (VHTI),[34] we break the inversion symmetry by shunting one of the two PZT disks in the unit cell. Breaking inversion symmetry opens a bandgap where the Dirac point was previously located. Figure 1(e) depicts the band structure for the symmetric and asymmetric unit cells along the irreducible BZ highlighting multiple complete bandgaps in the range $40 - 55$ kHz. Among them, we choose to work with the lowermost gap near 45 kHz. The topological nature of the bandgap is revealed using valley-Chern number calculations provided in the supplementary material (Sec. S2).

We set up the transistor in the OFF or ON state by shunting the PZT disks in an arrangement illustrated in Fig. 2(a) where blue and red filled circles represent open-circuit and NC shunted PZT disks, respectively. The OFF state contains one zigzag interface (identified by label Z and green arrows) and one bridge interface (identified by label B and red dashed line), both with neighboring open-circuited PZT disks. The shunt state for the PZT disks in the control region highlighted in yellow in Fig. 2(a) is swapped (i.e., NC shunt to open and open to NC shunt) to switch between the OFF and ON states of the transistor. Note that such a swapping of the shunt state in the control region results in the creation (or removal) of a second zigzag

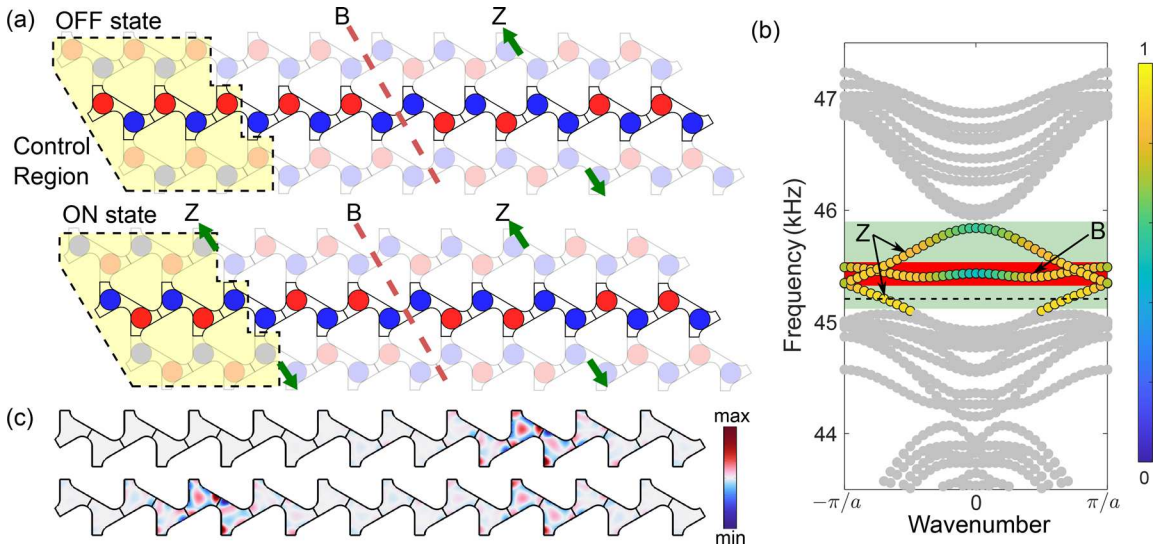

FIG. 2. (a) Illustration of the transistor supercell in OFF (top) and ON (bottom) states. Zigzag (bridge) interface is marked by green arrows (red dashed line) and identified using the letter Z (B). PZTs in the highlighted control region are changed between shunt and open-circuit electric terminations to reconfigure the supercell. (b) Computed band structure of the OFF state. The germane interface states are colored while the rest are grayed out. The colorbar indicates out-of-plane (z-direction) polarization of the modes. The frequency range highlighted in green has zigzag interface states useful for transistor action. The frequency range highlighted in red has additional bridge interface states and must be avoided. (c) Computed z-displacement mode shapes in the OFF (top) and ON (bottom) states of the transistor supercell illustrating localization at the zigzag interfaces at the frequency marked by the black dashed line in (b). The colorbar indicates relative displacement.

interface with neighboring open-circuited PZT disks. Figure 2(b) depicts the band structure computed by solving an EVP using FE model of the transistor supercell in the OFF state illustrated in Fig. 2(a) (top). The colorbar represents the polarization of the interface modes where a value of 1 indicates out-of-plane polarization. Only the germane interface modes are shown in color while the remaining modes are grayed out. In the frequency range highlighted in green in Fig. 2(b), only zigzag modes are present while in the frequency range highlighted in red both zigzag and bridge modes exist. It is required to operate the device in the frequency range highlighted in green where the absence of bridge modes isolates the two topological waveguides needed for the transistor action. Since the two zigzag interfaces in the ON state are identical, a second mode exists at the same frequency and Bloch wavenumber in the band structure of the ON state supercell (refer to Sec. S3 of the supplementary material). The mode shapes illustrating the localization at the zigzag interfaces are shown in Fig. 2(c) for OFF (top) and ON (bottom) states of the transistor at the frequency marked by the black dashed line in Fig. 2(b). Mode shapes illustrating the localization in the bridge interface are provided in Fig. S2 of the supplementary material.

From the computed band structure, we expect the zigzag topological mode to be near 45 kHz. As a preliminary step, we experimentally identify the appropriate operating frequency by measuring response across the transistor while providing an input with spectral content in the range of 42–48 kHz to the gate and source (refer to Sec. S4 of the supplementary material). From the measured data averaged across all scan points, we identify a peak in the response at 43.6 kHz, close to the predicted 45 kHz. Such a downshift in the topological interface frequency is within the expected range considering the tolerance on the thicknesses of the host aluminum structure and PZT disks.

We begin with experiments to observe the two distinct output states of the device at the identified operating frequency, which allow for bit abstraction to implement logic. Details of data acquisition are provided in the supplementary material (Sec. S4). The experimentally measured out-of-plane vibration depicted in Figs. 3(a) and 3(b) (Multimedia view) demonstrates the presence of one and two zigzag interfaces in the OFF and ON states, respectively. In the OFF state, the waves from the source decay evanescently into the bulk as the excitation frequency is within the bandgap. In the ON state, the reconfigured interface enables propagation of acoustic energy from the source to the drain. The steady state amplitude along the interface depends on the position of the acoustic input, the length of the lattice along the interface, the complex impedance at the boundary as well as the damping present in the system. Figures 3(c) and 3(d) depict the out-of-plane field across the transistor in OFF and ON states, respectively, obtained using FE simulations at a frequency of 45.2 kHz [black dashed line in Fig. 2(b)]. The results obtained in the experiment are comparable to those obtained through FE computation with a uniform damping (isotropic loss factor) $\eta = 0.005$ assumed for all materials used in the computational model.

Next, we engineer the device to achieve transistor ON–OFF action with the obtained distinct topologically protected states. In order to switch between the experimentally observed OFF and ON states for an input provided at the gate, we use a wave sensing module akin to one described in our previous work.[53] Acoustic energy input to the gate at the operating frequency propagates to the trigger along the topological waveguide. We feed the oscillating voltage generated by the PZT disk at the trigger to the wave sensing module. The module consists of a full-precision rectifier that converts the oscillating voltage signal into a DC voltage that triggers the mechanical relays [shown in

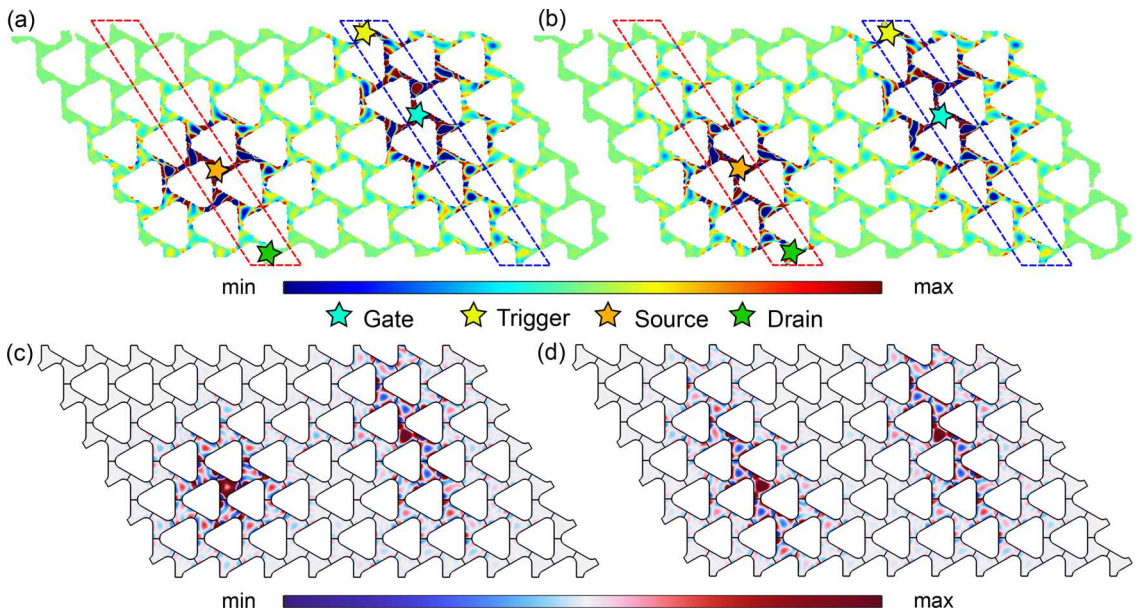

FIG. 3. Experimentally obtained steady state harmonic response of the transistor in (a) OFF and (b) ON states for an input at 43.6 kHz. The input and output topological interface positions are marked with blue and red dashed boxes, respectively. Various terminals in the device are marked with stars. FE simulated z-displacement of the transistor in (c) OFF and (d) ON states at 45.2 kHz [topological interface mode frequency marked by the dashed line in Fig. 2(b)]. The colorbars indicate relative displacement. Multimedia available online.

Fig. 1(c)] switching the shunt circuit power supplies. For bringing the voltages into an operable range at the input and output of the wave sensing module, we use a charge amplifier circuit and a buffer circuit, respectively. The circuit is experimentally tuned to set a normalized threshold of 0.7 such that a normalized input of 0.5 at the gate keeps the transistor in the OFF state while a normalized input of 1 switches the transistor to the ON state, enabling the second zigzag interface between source and drain. An acoustic energy input at the source then propagates to the drain. The circuit implementation is discussed in the supplementary material (Sec. S5).

To experimentally demonstrate the switching performance of the transistor, we input a varying amplitude sine wave, as illustrated in Fig. 4(a), at the gate terminal while a second input at the operating frequency is provided at the source terminal. During a single ON–OFF cycle, the normalized input signal amplitude goes from low (0.5) to high (1) and then reduces to low while the source terminal is maintained high. The input at the gate propagates along the zigzag topological interface and reaches the trigger. As the amplitude at the trigger increases beyond the threshold, the wave sensing module actuates the relays to switch the transistor state from OFF to ON by reconfiguring the second topological interface between source and drain.

The input is switched high for 20 ms between $t = t_a$ and $t = t_c$. The gray and green regions in Fig. 4(b) represent normalized voltage below and above the normalized threshold (= 0.7), respectively. The output rises above the normalized threshold at $t = t_b$, indicating the activation of the second interface. The delay $\Delta t = t_b - t_a \approx 4$ ms is attributed to the response time of the mechanical relays that switch power between shunt circuits. Although propagation of the interface waves from source to drain takes a finite amount of time, this duration is an order of magnitude smaller than the relay response time. The settling time $t_s = t_e - t_d$ where $t_d = t_c + \Delta t$ is measured to be approximately 10 ms and limits the maximum usable clock speed for a system built upon the transistor. It is worth noting that the settling time here is the time taken for the energy localized in the topological interface to dissipate into the bulk and only applies when switching from logic high to low. In the absence of damping (or smaller value of damping), the acoustic energy would scatter repeatedly from the boundaries of the system when the device switches from high to low, which may in turn interfere with the input topological channel. Thus, the presence of damping is advantageous in the finite system. The performance of the device for multiple ON–OFF cycles and construction of logic gates using the transistor are discussed in the supplementary material (Sec. S6).

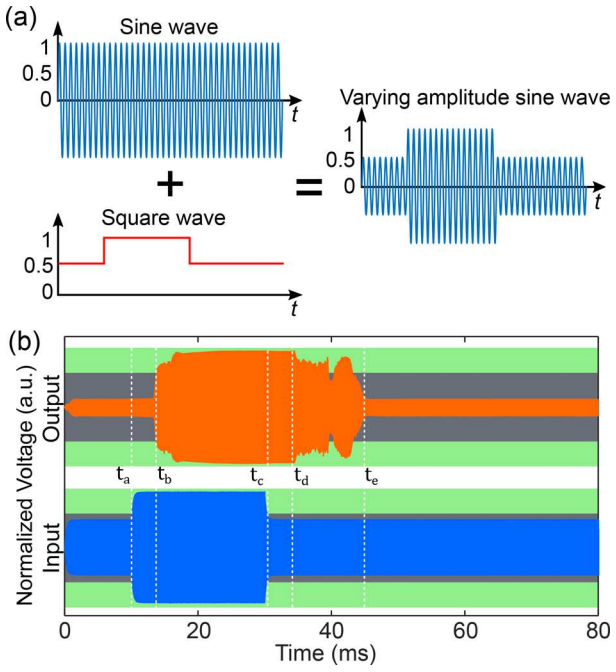

FIG. 4. (a) Illustration of the varying amplitude sine wave used to observe the switching behavior of the transistor. (b) Normalized input and output of the transistor for a single ON–OFF cycle. Experimental results are normalized to signal maximum. Gray and green regions represent normalized amplitude levels below and above threshold set at a normalized voltage of 0.7. Refer to main text for an explanation of labeled time instances.

In summary, we experimentally demonstrated a topologically protected electroacoustic transistor as a fundamental building block of wave-based logic. While multiple transistors may be cascaded to construct basic AND and OR gates, specially laid out reconfigurable interfaces maybe required for more advanced logic. The electroacoustic transistor may find utility in harsh surroundings where conventional electronics may fail or be prone to damage. We envision the proposed electroacoustic transistor (and transistor-enabled acoustic logic) to find applications in IIoT and edge computing by enabling *in situ* decision making, thereby reducing the computing load on a central processor. Similar devices developed for use with surface waves may find applications alongside SAW filters and switches in communication devices. Furthermore, we believe the topologically protected electroacoustic transistor will inspire novel technologies in soft materials that could potentially be used in next-generation wearables and medical devices.

See the supplementary material for details of the geometry of the unit cell, implementation of negative capacitance circuits, topological invariant calculation, supercell band structures, experimental setup, wave sensing circuit, switching and logic with the topologically protected transistor.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Sai Aditya Raman Kuchibhatla: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Michael J. Leamy:** Conceptualization (equal); Funding acquisition

(equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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