Exceptional Gate Overvoltage Robustness in P-Gate GaN HEMT with Integrated Circuit Interface

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***Abstract*—The narrow gate overvoltage margin of classical enhancement-mode p-gate GaN high electron mobility transistors (HEMT). is a major concern in both soft and hard switching applications. This work evaluates the gate overvoltage robustness of a smart p-gate GaN HEMT featuring a monolithic IC interface designed to enable a wide range of gate driving voltages (ICeGaN^{TM} HEMT). An external circuit is employed to produce a resonant gate-voltage (V_{GS}) overshoot to characterize the device's V_{GS} boundary under the stress of a single V_{GS} ringing. The ICeGaN^{TM} devices are stressed under different IC biases, at two temperatures (25 and 150 ºC), and under two power-loop conditions, i.e., the drain-and-source grounded (DSG) and the 400-V inductive hard switching (HSW). The V_{GS} limit of the ICeGaN^{TM} HEMT is found to be up to 92 V well in excess of that of a discrete classical p-gate GaN HEMT (35 V). The device failure mechanisms under different IC biases are also explored. It is found that, under the dynamic gate overvoltage, the IC interface could re-distribute the surge energy in the driver loop and limit the stress on the gate of the power HEMT. These results show the key role of the monolithic IC in enabling a superior gate overvoltage robustness in ICeGaN^{TM} devices.**

Keywords—GaN HEMT, monolithic IC interface, gate reliability, robustness, gate spike, ringing, power switching

I. Introduction

GaN HEMTs have enabled revolutionary advances in the frequency, efficiency, and form factor of power electronics systems [1], [2]. Among different GaN HEMT technologies, the Schottky-type p-gate GaN HEMTs (SP-HEMTs) have been widely adopted by device vendors and foundries with a voltage class range from 15 to 650 V in commercial devices. A critical issue of SP-HEMTs is the small margin between the typical drive voltage (e.g., 6 V) and the maximum allowable voltage (e.g., 7 V), which can be as low as 1 V [3], [4]. This small margin raises concerns on the GaN HEMT gate reliability in practical applications and poses challenges on the gate driver design [5] and the connection between the driver and the GaN HEMT.

Recently, a novel 650 V power ICeGaN^{TM} (Integrated Circuit Enhancement-mode GaN) technology has been demonstrated in the industry, which monolithically integrates a gate interface with a power SP-HEMT [6]–[8]. The ICeGaN^{TM} device offers the advantages of a high threshold voltage (V_{TH}) ~ 3 V and a wide range of gate driving voltages up to 20 V, which allows the device to be driven by the standard Si gate drivers. Despite a wider range of gate driving voltages, the gate overvoltage robustness of this device under the transient switching conditions is still unknown. It is the aim of this work to address this issue. For this, an inductive-load circuit has been designed and built to characterize the dynamic gate overvoltage boundaries of the ICeGaN^{TM}. To best mimic gate overshoot in practical converters, a resonance-like gate overshoot is produced with a pulse width down to 20 ns in different power loop conditions. The tests are also performed under multiple IC-interface biases, demonstrating a gate overvoltage boundary over 90 V for ICeGaN^{TM}. In comparison, the intrinsic gate overvoltage boundary of the discrete SP-HEMT is only 35 V. This is measured by applying the same stress condition directly to the inner gate of the GaN HEMT (therefore bypassing the smart ICeGaN^{TM} interface). The tests in this work also reveal an enhanced parametric stability before device failure as well as a soft failure mode with the gate functionality largely retained.

II. Device Under Test and Test Methodology

A. Devices Under Test

The devices under test (DUTs) in this work are the 650 V/130mΩ ICeGaN^{TM} from Cambridge GaN Devices Ltd.. Fig. 1 illustrates the schematic of the smart ICeGaN^{TM} integrated circuit (IC) which is powered by a 12~20V voltage source V_{DD}. This smart IC interface comprises a Sense FET, an Auxiliary low-voltage GaN HEMT, a voltage regulator, a voltage limiter, logic circuits and a novel Miller Clamp. The Auxiliary HEMT is responsible for absorbing a large fraction of the driver voltages applied on the external gate under both static and dynamic conditions. The Miller Clamp comprises a new device which can be described as a combination of a depletion HEMT and an enhancement HEMT for a fast switching from high-impedance mode to ON state, enabling the fast re-directing of the surge energy to ground when the

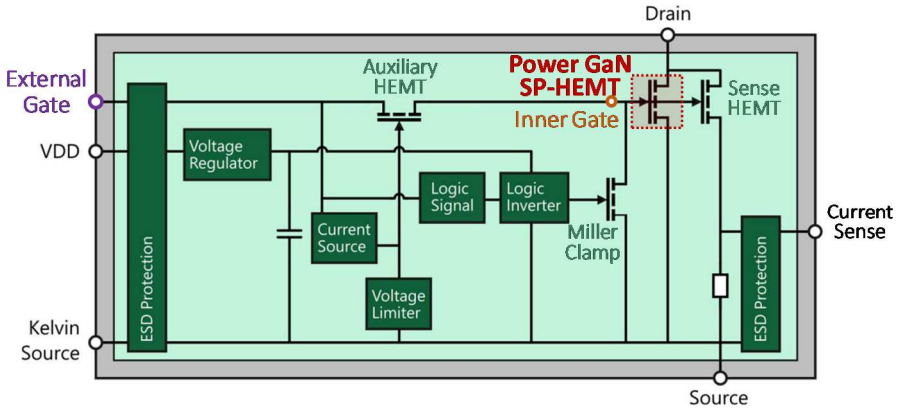

Fig. 1. Schematic of the ICeGaN^{TM} HEMT which consists of a power GaN SP-HEMT and a monolithically integrated power IC interface.

external gate sees an overvoltage, achieving an extra protection for the ICeGaN^{TM} inner [6]. Another functionality of this Miller Clamp is to sharply turn OFF the ICeGaN^{TM} [6] to enable a safe OFF-state operation and avoid the transient-induced false turn-on events (e.g., in bridge-leg configurations [9]) even under a non-negative OFF-state driving voltage. The voltage limiter sets a limit on the inner gate voltage terminal in order to protect the gate. An ESD protection circuit is monolithically integrated and connected between the external gate and V_{DD}. The detailed architecture and working principle of the ICeGaN^{TM} are presented in [6]–[8].

B. Test Platform

The resonant V_{GS} overshoot across the gate (either inner or external gate) and the source (G-S) of the ICeGaN^{TM} is generated by a carefully designed circuit with flexible load conditions in the drain-source (D-S) loop during the V_{GS} overshoot. In this paper, the D-S switching schemes are configured as either the drain-and-source grounded (DSG) condition to mimic the zero-voltage switching or the hard switching (HSW) at 400-V bus voltage (V_{BUS}) with inductive load. Fig. 2(a) and Fig. 2(b) illustrate the exemplary circuit schematics for dynamic-gate-overvoltage test at ICeGaN^{TM}'s external gate in the DSG and HSW conditions, respectively. The test methodology and circuit operation principles are described in more detail in [10]–[12]. Fig. 2(c) shows the photo of the test board configured for the HSW condition.

The gate-overvoltage-generation circuit produces an overshoot in the device's G-S loop, similar to how an overshoot is generated in the D-S loop in the classic unclamped inductive switching (UIS) test [13]–[19]. The core idea is to build up and store energy in a gate-loop inductor (L_G, which mimics the parasitic inductance in practical converters), with the L_G being charged by a voltage source (V_{DD} = 0.5 V in this work). A low-voltage GaN HEMT [20] is used as a fast switch (S_1) to create a V_{GS} overshoot directly at the DUT's gate. In *Stage I*, S_1 turns ON, allowing L_G to be charged by V_{DD}. In *Stage II*, S_1 turns OFF, the energy in L_G creates a resonant overvoltage across the L_G (V_{LG}). The V_{LG} overshoot can be regarded as the resonance between L_G and an equivalent capacitance (the sum of the C_{ISS} of DUT and the C_{OSS} of S_1). As the DUT's V_{GS} = V_{LG} + V_{DD}, a resonant overvoltage added on a DC component (V_{DD}) is applied directly across the DUT's gate and source.

The pulse width (*PW*) of the V_{GS} overshoot can be thus approximated as a half of the V_{LG}-overshoot resonance period,

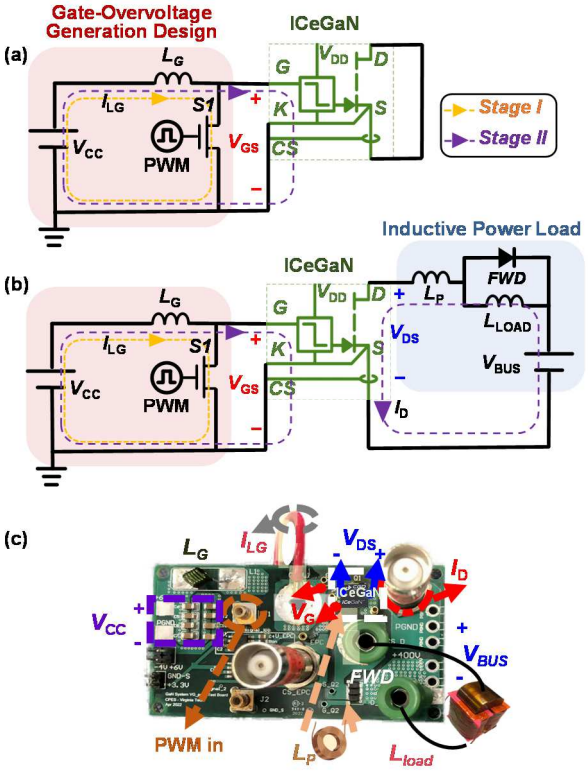

Fig. 2. Exemplary circuits schematics and working stages of the dynamic-gate-overvoltage test at ICeGaN^{TM}'s external gate in (a) drain-and source-grounded (DSG) condition, and (b) 400-V hard-switching (HSW) with inductive load. (c) Photo of the test circuit board configured in the HSW condition.

which can be modulated by varying the L_G value. The *PW* is selected as 20 ns in all tests in this work to best mimic the common transient overshoots in practical operations. After L_G is determined, the V_{GS}-overshoot peak magnitude [$V_{GS(PK)}$] can be modulated by the V_{DD} value and the ON-time of S_1.

In the HSW condition, the power loop is configured with a 400-V V_{BUS} with capacitor bank, a load inductor L_{LOAD} (24 mH), a free-wheeling diode (*FWD*), as well as a smaller inductor L_P (1 µH) to mimic the power-loop parasitic inductance and to suppress the drain-source current (I_D) and its overlap with high drain-source voltage (V_{DS}) for preventing the thermal runaway. When the V_{GS} overshoot exceeds DUT's V_{TH}, the device goes through the hard turn-ON process, with

an overlap between high V_{GS}, high V_{DS}, and high I_D. This process resembles the nature of the V_{GS} ringing in practical converter operations, which is generally induced during the device's turn-ON transients in power switching by the gate-loop parasitic inductance. The DUT's V_{GS} and V_{DS} are sensed by a 1-GHz-bandwidth low-voltage passive probe (Tektronix TPP1000) and an 800-MHz-bandwidth high-voltage passive probe (Tektronix TPP0850), respectively, for fast-switching measurements.

Devices are tested at 25 and 150 ℃ to study the temperature impact on the gate robustness. In tests under 150 ℃, the DUTs are heated by a power resistor attached to their case, with the case temperature carefully calibrated by a K-type thermocouple as well as a thermal camera.

III. Test Results

To investigate the interface IC's functionality, the dynamic gate breakdown voltage ($BV_{G,DYN}$) is first tested at the inner gate to evaluate the intrinsic gate robustness of the SP-HEMT, and then stressed at the external gate (i.e., the gate of the ICeGaN^{TM}) under multiple IC biases for a comparison.

In each test, the $BV_{G,DYN}$ is measured by consecutive single-pulse V_{GS} overshoots with a step increase in $V_{GS(PK)}$ (1 V for inner-gate tests and 2 V for others) untill a failure is observed from the test waveform. As shown in the red V_{GS} waveforms in Fig. 3, for either the inner gate or the external gate of ICeGaN^{TM} under different IC biases, the fast damped V_{GS} ringing after $V_{GS(PK)}$ suggests a possible G-S failure. These possible failures have been confirmed by the post-stress static I-V characterizations performed on Keysight B1505 Power Device Analyzer or the extra circuit tests for dynamic characterizations. Despite the discrepancies in behaviors after the gate failure under multiple test conditions, degradations in these DUTs' static or dynamic functionalities have been observed.

Fig.3(a) shows the last two survival and the failure V_{GS} waveforms of the DUT measured at the inner gate of power HEMT (with V_{DD} floating) under DSG condition at 25℃, revealing a 33-V $BV_{G,DYN}$, which is ~9 V higher than a recently reported limit of a commercial 650-V SP-HEMT from another vendor [10]. Enabled by the IC interface (with V_{DD} = 20 V), the overvoltage limit of the ICeGaN^{TM} external gate is found to be boosted up to 66 V under DSG condition at 25℃ (see Fig.3(b)). This $BV_{G,DYN}$ is ~6 V higher under either HSW condition [(see Fig.3(c))] or at 150 ℃.

Finally, the $BV_{G,DYN}$ is measured on the external gate of the ICeGaN^{TM} under the condition where V_{DD} is shorted together with the external gate. This test condition removes the overvoltage stress applied to some critical components within the ESD protection circuit and measures the gate overvoltage withstanding capability of the inherent auxiliary modules within the IC interface. The gate failure boundaries of the ICeGaN^{TM} are found to be 84 V at 25 ℃ [(see Fig.3(d))] and 92 V at 150 ℃ [(see Fig.3(e))]. Note that, the external V_{GS} waveform in Fig.3(d) deviates from a standard resonance waveform during the V_{GS} drop. This is probably due to the very fast turn-ON of the IC Miller Clamp which re-directs a large portion of the surge energy to ground. Table I summarizes the $BV_{G,DYN}$ data of the power SP-HEMT, as well as the ICeGaN^{TM} external gate under multiple IC biases, in DSG condition at 25 and 150 ℃.

This $BV_{G,DYN}$ of the external gate enabled by the IC platform (92 V under the V_{DD} shorted with the external gate condition or 72 V under V_{DD} = 20 V, measured in DSG and 150 ℃) is comparable to the $BV_{G,DYN}$ of a commercial 650-V Silicon IGBT (80 V) [21] and SiC MOSFET (70 V) [22] measured using the same circuit setup [10], and is much higher than the $BV_{G,DYN}$ of a commercial GaN SP-HEMT (25

Table I. $BV_{G,DYN}$ of the ICeGaN^{TM} tested under various stress and IC-bias conditions, under DSG condition and two temperatures.

Stress and IC-bias Conditions	25℃	150℃
Internal Gate (V_{DD} floating)	33 V	35 V
External Gate (V_{DD} = 20 V)	66 V	72 V
External Gate (V_{DD} short with external gate)	84 V	92 V

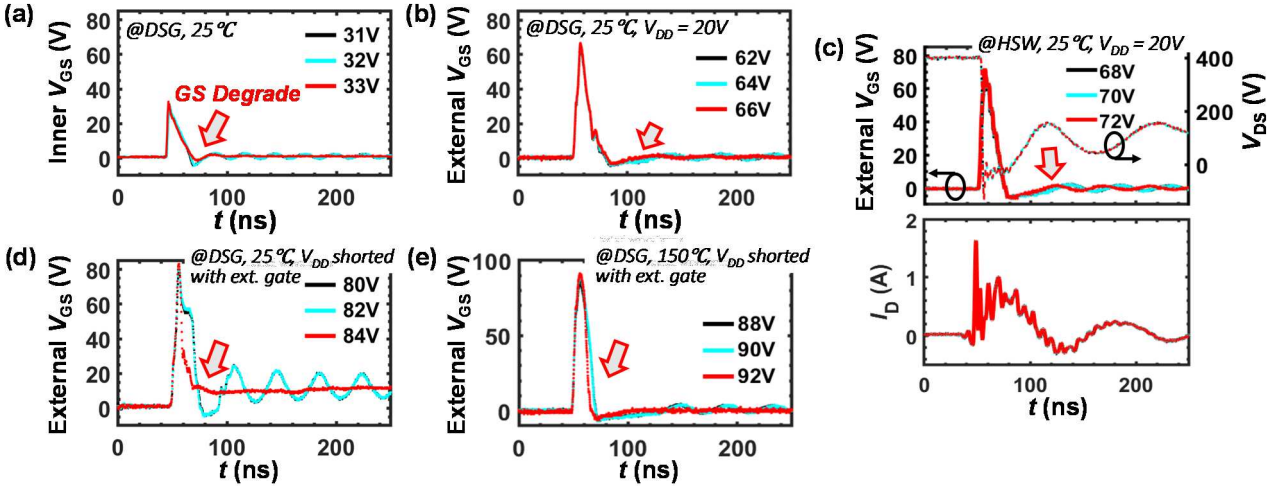

Fig. 3. Tested waveforms under stressing at ICeGaN device's (a) inner gate under DSG, 25℃, as well as external gate with V_{DD} = 20 V under (b) DSG, 25℃ and (c) 400-V inductive-load HSW, 25℃. The highest $BV_{G,DYN}$ occurs in the V_{DD} shorted with the external gate condition at external gate, with (d) 84V at 25℃ and (e) 92V at 150℃. The pulse width of gate overvoltage is fixed at 20 ns. The V_{GS} waveforms after failure or failure in all conditions show fast damping after the V_{GS} overshoot, suggesting a gate-to-source failure.

Table II. $BV_{G,DYN}$ of the external gate of ICeGaN™ when it is shorted with V_{DD} , in comparison with the $BV_{G,DYN}$ of a commercial 650-V GaN SP-HEMT, SiC MOSFET, and Si IGBT measured under the same circuit setup. The measurements are in DSG condition at 25 and 150 °C.

DUTs	25°C	150°C
GaN SP-HEMT [23]	24 V	25 V
SiC MOSFET [22]	70 V	70 V
Si IGBT [21]	80 V	80 V
ICeGaN™ (V_{DD} short with external gate)	92 V	84 V

V) from another vendor [23] as reported in [10]. Such comparisons are summarized in Table II.

In addition to the high $BV_{G,DYN}$ strengthened by the smart interface, the ICeGaN™ retains the V_{DS}-blocking capability after the G-S failure or failure in all tests in this work, as can be seen from the intact V_{DS} and I_D waveforms in the failed DUT stressed in HSW condition [see Fig.3(c)]. This V_{DS}-blocking functionality is further confirmed by the post-stress I-V characterizations.

IV. Failure Mechanism of ICeGaN™ Under IC Bias with V_{DD} = 20 V

Under positive gate overvoltage, the failure of SP-HEMT usually occurs at the p-GaN Schottky contact [10], which is different from the failure mechanism of the insulated gate in IGBT and MOSFETs. In ICeGaN™, the IC network improve the gate robustness of the power HEMT by multiple functioning physics. The dominant protecting mechanisms depend on the stress and IC-bias conditions, resulting in different failure physics under stress, explaining the variation of the $BV_{G,DYN}$ measured under multiple tests listed in Table I. This session is an extended study for the failure physical mechanisms of the ICeGaN™ stressed under IC bias with V_{DD} = 20 V.

Post-test failure analysis has been done on the failed ICeGaN™ HEMTs stressed under multiple tests listed in Table I. The failed DUT under V_{DD} = 20 V shows burn marks within a forward bias diode present in the ESD block, as shown in Fig. 4. This suggests the measured $BV_{G,DYN}$ is limited by the ESD circuit. The ESD circuit could simply be redesigned to remove this stress (future work).

The I-V characteristics of ICeGaN™ are also measured after each V_{GS} overshoot test with the increased $V_{GS(PK)}$. All characterizations are performed by taking the DUT from the circuit board and measuring it on the B1505 curve tracer at 25 °C and biased with IC powered by V_{DD} = 20 V. Hence, the measured parametric shifts reflect those that cannot recover in a few minutes. Fig. 5 shows the gate leakage, transfer, output, and reverse conduction characteristics of the DUT stressed in circuit tests and biased under V_{DD} = 20 V [corresponding to the waveforms shown in Fig.3(b)]. The DUT is measured in different stages (i)fresh, (ii) after the last survival pulse ($V_{GS(PK)}$ 2-V lower than $BV_{G,DYN}$), as well as (iii) after gate failure at $BV_{G,DY.}$, Minimal shifts in I-V characteristics are observed between stage (i) and stage (ii).

Moreover, the functional reverse conduction of the ICeGaN™ after the gate failure characterized at V_{GS} = 0 V [see Fig.5(d)] (as the DUT's G-S has failed to short) after the breakdown suggests that the failure occurs in the G-S loop, with a functional current-conducting capability in the D-S loop.

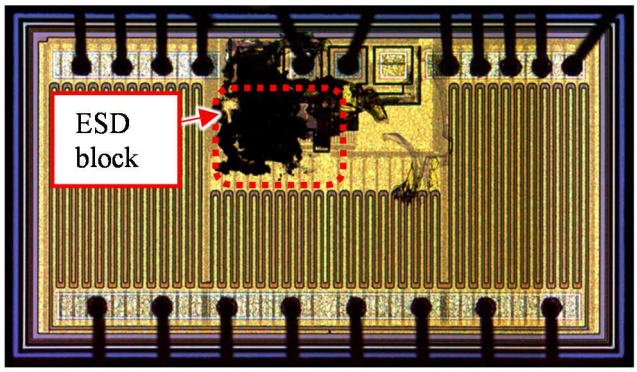

Fig. 4. Optical microscope photo of the surface of the decapsulated failed DUT, which is stressed at external gate with V_{DD} = 20 V. Burn track is observed within the ESD block.

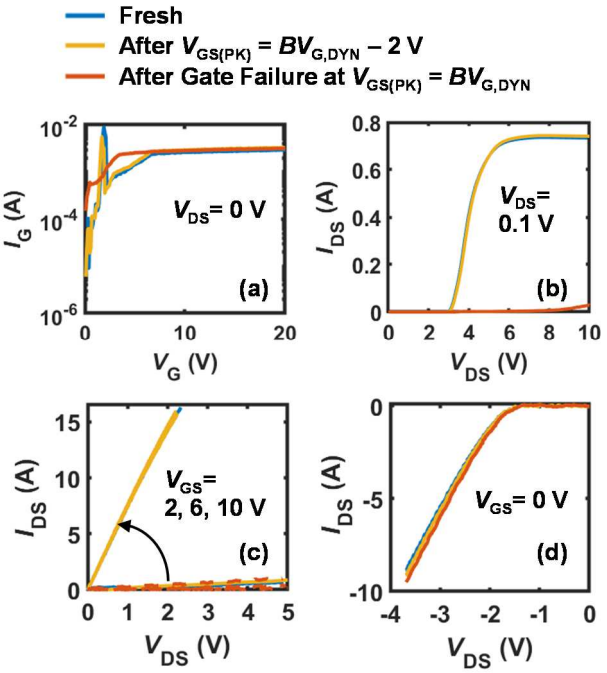

Fig. 5. I-V characteristics of the ICeGaN™ when being fresh, survived the last V_{GS} overshoot at $V_{GS(PK)}$ 2-V below the $BV_{G,DYN}$, and after the gate failure at $BV_{G,DYN}$. From (a) to (d) are the I_G-V_G, transfer, output and reverse-conduction characteristics, respectively.

V. Failure Mechanism of ICeGaN™ Under IC Bias with V_{DD} Shorted with External Gate

In Section III, it has been revealed that, when the V_{DD} is shorted to the external gate (the accessible gate terminal of ICeGaN™) to avoid the preliminary breakdown of the ESD circuit, a higher $BV_{G,DYN}$ is observed (84 V at 25 °C and 92 V at 150 °C). This session is an extended study for the failure physics mechanisms of the DUT stressed under such IC bias. Fig. 6 shows the static characteristics of a DUT failed in the circuit tests with the V_{DD} shorted with the external gate [corresponding to the waveforms shown in Fig.3(e)]. Minimal parametric shifts are observed in these device I-V

characteristics after failure. No visible burn marks are observed in the post-failure analysis after the decapsulation.

For an insight into the physical mechanisms of this soft failure, we perform additional tests to examine the functionalities of the auxiliary circuits within the IC interface. A V_{GS} overshoot with a $V_{GS(PK)}$ below the $BV_{G,DYN}$ is first generated at the DUT's external gate when the DUT is being fresh and operated at 25 °C. The V_{DD} is deliberately shorted to the external gate, as shown in Fig. 7(a). This test is repeated after the DUT failed in the $BV_{G,DYN}$ circuit test. The surge energy of the V_{GS} overshoot in each of the two tests are kept as the same by the circuit.

As shown in the IC interface schematics in Fig. 7(a), in a fresh ICeGaN™ under such test condition, the surge energy generated from the driving loop can be re-directed to ground by the fast turn-ON of the Miller Clamp (Path 1) as well as being dissipated in the loop of Auxiliary HEMT and the C_{ISS} of the power HEMT (Path 2). As compared in Fig. 7(b) and Fig. 7(c), under the same surge current, the $V_{GS(PK)}$ of the overshoot created at the external gate of ICeGaN™ after failure is much higher than that in the DUT's fresh state. This suggests a higher energy flowing through Path 2, which generates the resonant component in the external-gate overvoltage. This can be attributed to a degradation in the Miller Clamp which loses the surge-energy discharging functionality after the soft failure.

VI. Conclusion

This paper evaluated the gate robustness against transient overvoltage of a novel industrial 650-V power ICeGaN™ with superior gate driver margin over conventional p-gate GaN HEMT. The results show a significantly boosted gate-overvoltage failure boundary under converter-operation stresses. A circuit is developed to characterize the gate-voltage boundary with multiple IC biases, at 25 and 150 °C, as well as under the drain-source-grounded and 400-V inductive hard switching. The ICeGaN™ enables a dynamic gate-overvoltage boundary up to 72 V when the IC is powered, and reaches 92 V when the external gate is shorted together with the IC power supply (V_{DD}), hence yielding a very significantly enhanced safety boundary when compared to a standalone power SP-HEMT (35 V). Finally, post-stress characterizations and analyses verify the protection functionalities of multiple auxiliary components in the smart GaN interface to boost the gate robustness and reliability of ICeGaN™ under the gate overvoltage stress.

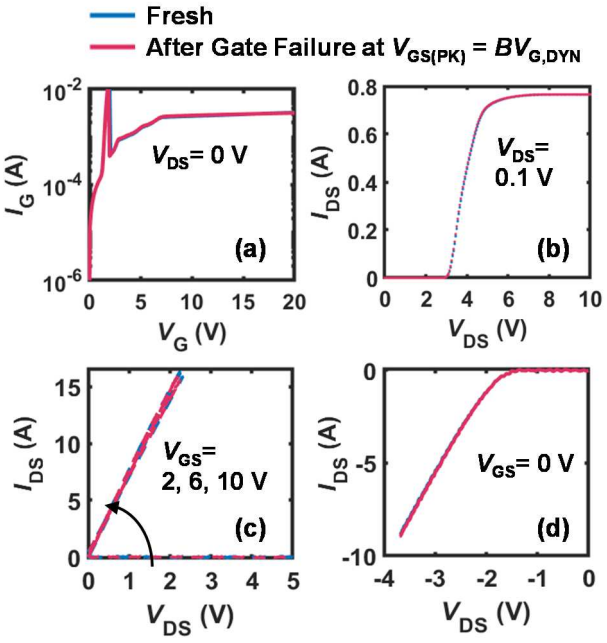

Fig. 6. Typical I-V characteristics of the ICeGaN™ when being fresh and after the soft failure. From (a) to (d) are the I_G-V_G, transfer, output and reverse-conduction characteristics, respectively.

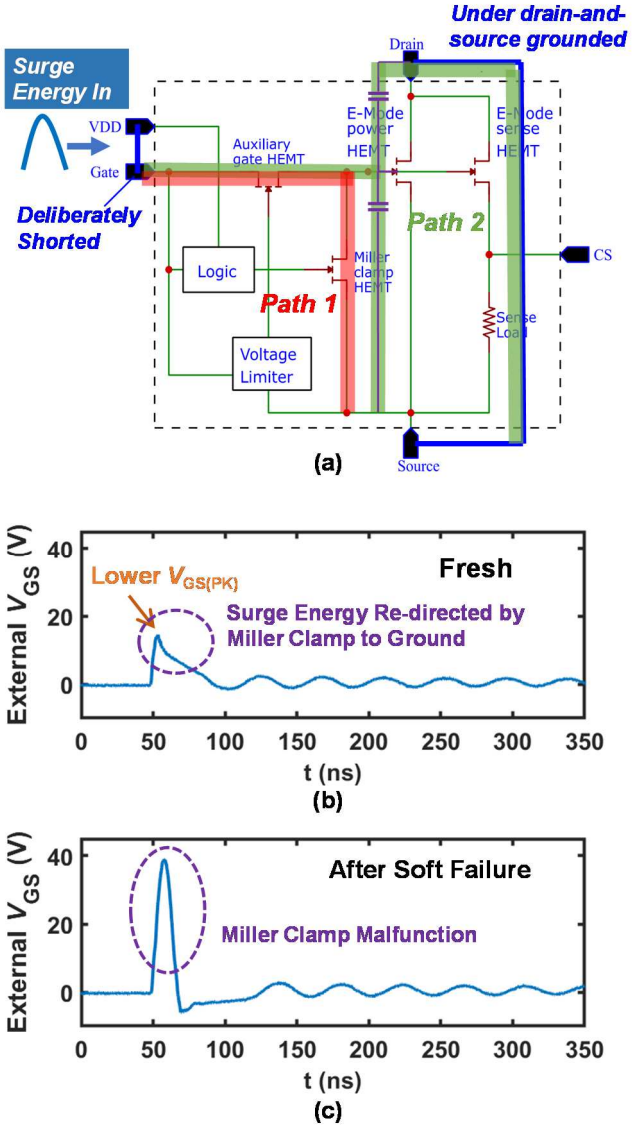

Fig. 7. Failure mechanisms of ICeGaN™ under driving-loop overvoltage stress with the auxiliary IC power source (V_{DD}) deliberately being shorted to the external gate (in DSG condition at 25 °C). (a) Schematics of the surge energy path in ICeGaN™. In the DUT fresh state, the Miller Clamp in Path 1 turns ON to re-direct a large portion of surge energy to ground. The rest of the energy passes through the gate-loop of power HEMT (Path 2). The ICeGaN™ external-gate V_{GS} waveform when DUT is (b) fresh and (c) after the soft failure under the same overvoltage surge energy. After failure, the presence of the much higher $V_{GS(PK)}$ suggests a malfunction of Path 1.

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