Three-dimensional Environmentally Sustainable Neuromorphic Computing System Based on Natural Organic Memristor

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***Abstract*—Three-dimensional environmentally sustainable neuromorphic computing system based on natural organic honey-memristor is proposed in this paper. The experimental results indicates the proposed systems have high inference accuracy over 90% with device variation and nonlinearity. What is more, four conductance drift scenarios, ADC (Analog-to-Digital Converter) quantization effects, and different algorithms (VGG8 and DenseNet-40) are considered to further verify the proposed systems.**

***Index Terms*—Natural organic memristor, honey-memristor, neuromorphic system, artificial intelligence (AI), inference accuracy, variation, nonlinearity, three-dimensional (3D)**

I. Introduction

The scaling down of CMOS (Complementary Metal-Oxide Semiconductor) technology has greatly enabled and supported the growing computation in last decades [1]. However, some physical limitations have suppressed the further development of CMOS technology, especially for AI applications. Accordingly, a new device with high speed and low power enabling computationally intensive applications, such as large data centers and edge devices, is urgently needed. Memristor is such a promising device which has a potential of making smooth transition from CMOS-based systems to advanced devices by unlocking CIM (Computing in Memory) capability. Memristor uses multi-level conductance sates to regulate current flow as well as store charges that have previously been flowed through it. Even if powering off, such programmed states and charges are not lost. Besides non-volatility and multilevel resistive state property, memristor exhibits wonderful characteristics, such as low computational complexity [2], sub-nanosecond switching speed [3] sub-10-nm scalability [4], low energy dissipation of few pJ per bit [3], [5]–[8], long write-erase endurance [9], and CMOS-compatibility [10], [11]. As a result, it can efficiently implement high performance neural networks in hardware for CIM [12].

However, most of existing memristors are made from inorganic metal oxide [13], [14] and synthetic polymer [15], although they contributed to neuromorphic computing, they all failed to consider environmental sustainability in manufacture and disposal. In 1987, the Bruntland Report defined sustainability as "development that meets the needs of the present without compromising the ability of future generations to meet their own needs [16]". Therefore, sustainable computing that makes future generations thrive becomes central to the core purpose of electronics and semiconductor industries, which results in a commitment to the exploration of greener material and process pathways that enable environmentally friendly and sustainable manufacturing solutions for novel devices.

Natural organic memristor, such as honey-memristors [17]–[23], is one of such most prospective sustainable devices. It is low cost, earth-abundant, renewable, bio-degradable, and has eco-friendly disposal. Therefore, in this paper, our team proposes novel honey-memristor based 3D (three-dimensional) neuromorphic computing systems for environmental sustainability in computing. Our team firstly manufacture honey-memristors and then use reliable platform to evaluate the inference accuracy of systems with different algorithms, retention, and ADC (Analog-to-Digital Converter) quantization, which shows the significant potential of 3D natural organic memristor-based neuromorphic systems for AI applications and also gives the design reference for the following researchers and designers.

II. Honey-Memristor

A. Honey-memristor Fabrication

Our honey-memristors are fabricated on a 2.5 cm × 2.5 cm glass slide. The glass slide is cleaned by acetone, IPA

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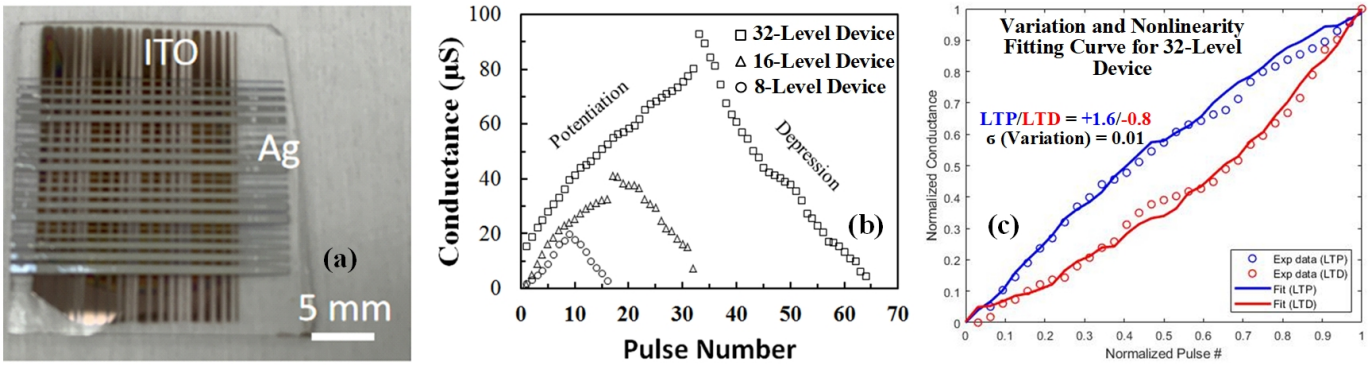

Fig. 1: (a) Photograph of a honey-memristor crossbar array on the glass substrate. (b) LTP and LTD characteristics for 8-, 16-, and 32-level potentiation and depression. (c) Variation and nonlinearity fitting curve for 32-level device.

(Isopropyl Alcohol) and D.I. (deionized) water in ultrasonic bath each for 10 mins, followed by the deposition of indium tin oxide (ITO) as bottom electrodes with the width of 100 μm, 200 μm, 300 μm, 400 μm and 500 μm through a stencil mask. The final sheet resistance of the ITO film was 10 Ω/sq. The honey solution with a concentration of 30 wt% was prepared by dissolving commercial honey (100%, US Grade A) in D.I. water at room temperature until no honey crystals were visible. The honey solution was coated on the ITO/glass substrates at 1000 rpm for 90 s on a spinner, followed by baking on a hotplate in air at 90°C for 9 hours to dry the honey film. Finally, *Ag* top electrodes (100 nm-thick) are deposited on the honey film through the same stencil mask rotated by 90° to form a crossbar array. A photograph of the honey crossbar structure is shown in Fig. 1 (a) with each cross point representing an *Ag*/honey/ITO memristor.

B. Honey-memristor Characterization

8-, 16-, and 32-level honey-memristors are throughly tested. During the test, consecutive square voltage pulses (duty cycle: 50%) in positive polarity with 0.8 V amplitude are applied first, and followed by pulses in negative polarity with 0.6 V amplitude. The magnitude of the current steadily increased as the number of positive voltage pulse increases, indicating that honey-memristor device can mimic synaptic long term potentiation (LTP) of a biological synapse. When the pulse voltage changed to negative polarity, magnitude of the current decayed until the last negative voltage pulse, a behavior analogous to synaptic long term depression (LTD). Fig. 1 (b) summarizes the LTP and LTD characteristics for 8-, 16-, and 32-level honey-memristors using the same pulse width, duty cycle, and amplitude. They all follow that the conduction gradually increases with an increase in the positive pulse train. In contrast, if we change the polarity of the pulse to negative, the conduction of the memristor decreases with an increase in the pulse train.

C. Variation and Nonlinearity

Similar to inorganic memristors, the weight update variation and nonlinearity of the honey-memristor happen as the conductance is not updated following the ideal curve [24]–[26].

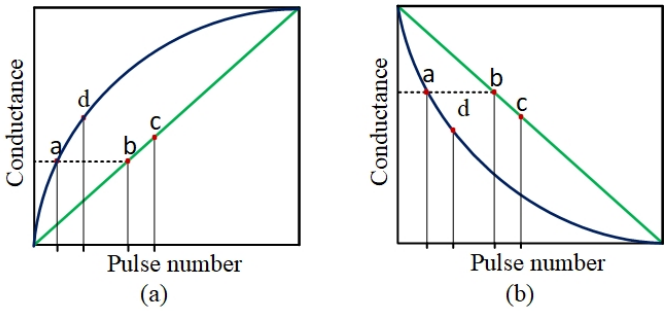

Fig. 2: Conductance Change with Nonlinearity in (a) LTP and (b) LTD

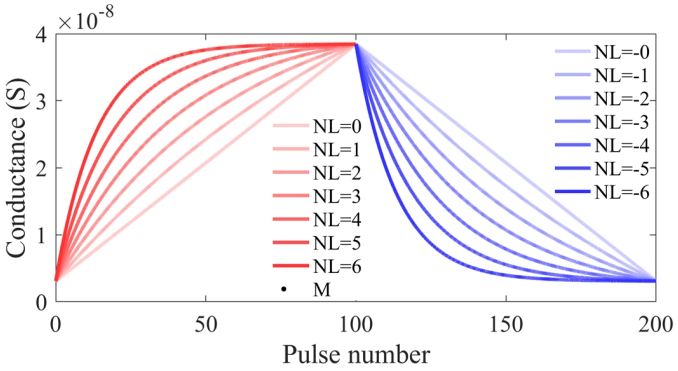

Fig. 3: Conductance Change Curves under Various Nonlinearity of LTP and LTD.

The conductance of the memristor represents the weight of the neural network. The weight update variation is the fluctuation in conductance change at each programming pulse. This fluctuation (σ) is represented as a percentage of the entire conductance range. As for the nonlinearity, as demonstrated in Fig. 2, the dark curve depicts the conductance of an actual memristor. The pulses have the same duration and the same amplitude, and the green line represents the function of the ideal case. In LTP, as shown in Fig. 2 (a), according to the result obtained by the algorithm, the conductance of memristor

theoretically needs to be changed from point b to c. Then, the corresponding number of pulses is calculated according to the ideal curve (green). However, when these pulses are applied to the actual memristor, instead of changing from point b to c, the device conductance changes from point a to d. Consequently, the actual change of conductance and the required change are not same. Similarly, Fig. 2 (b) shows the occurrence in the LTD, where the actual conductance changes to point d instead of point c [27]. The variation and nonlinearity of the memristor cause the weight change to be inconsistent with the change required by the learning algorithm, thereby reducing the inference accuracy.

A nonlinear curve is used to fit the nonlinearity of our honey-memristor, as shown in Fig. 1 (c). This curve is generated from a mathematical model (Equations (1) and (2)) [28], as shown in Fig. 3. The curve is labeled with a NL value (it is the normalized value of parameter A in Equations (1) and (2)) from +6 to -6, which represents the extent to the curve deviates from the ideal linear device. Here the positive (+) and negative (-) signs are merely to label LTP and LTD, respectively.

$$G_{LTP} = B(1 - e^{(-\frac{P}{A})}) + G_{min} \quad (1)$$

$$G_{LTD} = -B(1 - e^{(-\frac{P - P_{max}}{A})}) + G_{max} \quad (2)$$

$$B = (G_{max} - G_{min})/(1 - e^{\frac{-P_{max}}{A}}) \quad (3)$$

where G_{LTP} and G_{LTD} are the conductance for LTP and LTD cases, respectively. G_{max}, G_{min}, and P_{max} are extracted from the experimental and testing data, which represents the maximum and minimum conductance, and maximum pulse number required to switch the device between the minimum and maximum conductance. Parameter A controls the nonlinear behavior of weight update. B is a function of A that fits the functions within the range of G_{max}, G_{min}, and P_{max}.

Through fitting work and adding regulations for device variations, LTP/LTD = +4/-1.8, +0.7/-0.8, and +1.6/-0.8, and σ = 0.08, 0.01, and 0.01 are respectively applied for our 8-, 16-, and 32-level honey-memristors, as listed in Table I.

III. Heterogeneous Three Dimensional (3D) Architecture

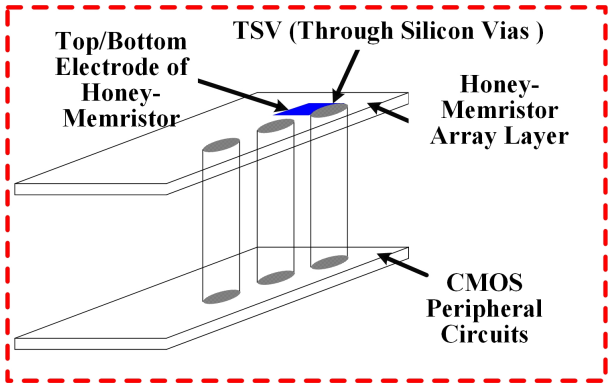

Fig. 4: 3D Architecture with TSV.

For heterogeneous 3D architecture, a two-tier structure is designed as shown in Fig. 4, where the honey-memristor array is on the top tier, and logic circuits are on the bottom tier. The operation strategy is assumed to be layer-by-layer scheme. Each time, the honey-memristor array will be activated to access data from logic tier, and then the data will be sent to honey-memristor array through TSV (Through Silicon Via) path. After the honey-memristor array finishes the analog computation, the output signal will be sent back to the logic tier for further data-processing.

IV. Experimental Results and Discussion

A. Accuracy

Characteristics of honey-memristors are incorporated into DNN+NeuroSim platform for evaluations. DNN+NeuroSim is an integrated framework that emulates deep neural networks (DNN) inference performance on the memristor-based hardware [29]. An 8-layer VGG8 model with random drift and 5-bit ADC precision for CIFAR10 dataset is applied. As listed in Table I, with specific device variation and nonlinerity, neuromorphic systems based on 8-, 16-, and 32-level honey-memristors all have over 90% inference accuracy. This indicates that for VGG8 model, even 8-level honey-memristor is enough for weight value storage and keep high accuracy.

TABLE I: Inference Accuracy for 8-, 16-, and 32-level Honey-memristor Based Neuromorphic Systems

Devices	8-level	16-level	32-level
Variation (σ)	0.08	0.01	0.01
Nonlinerity (LTP\LTD)	+4/-1.8	+0.7/-0.8	+1.6/-0.8
Accuracy	91%	92%	92%

B. Retention

Retention is defined as the ability of the memristor device to retain its programmed state over a long period of time [30]. Typically the retention ability of a memristor is more than 10 years at 85 degree centigrade. An 8-layer VGG8 model with random drift and 5-bit ADC precision for CIFAR10 dataset is utilized, and four conductance drift scenarios with three honey-memristors have been discussed for the retention analysis: Drift to High Resistive State (HRS): 0, Drift to Low Resistive

TABLE II: Impact of Drift on Honey-memristor Based Neuromorphic Systems

Drift	Device	Inference Accuracy
0	32	91%
0.5	32	91%
1	32	91%
RANDOM	32	92%
0	16	91%
0.5	16	91%
1	16	91%
RANDOM	16	92%
0	8	91%
0.5	8	91%
1	8	91%
RANDOM	8	91%

State (LRS): 1, Drift to Middle (0.5), and Random Drift. As listed in Table II, the honey-memristor based neuromorphic system can successfully keep the high inference accuracy even in different drift conditions, which indicates that the system has high immunity to device drift effect.

C. ADC Quantization Effects

In the CIM architecture, there are mainly two read-out schemes. A sequential processing method of the matrix-vector multiplication is to read out the dot-products in a row-by-row manner, which leads to extra energy and latency for accumulations along the rows [31]. In our honey-memristor based neuromorphic system, a more efficient method as parallel processing is used, where multiple rows are activated simultaneously by a switch matrix, and the current summation is read out by an ADC. What is more, a non-linear quantization is employed for the ADC reference, according to the distribution of partial-sums, the references are more spread in high-probability area, while less in low-probability part. To read out the partial-sums in parallel modes, it requires ADC with high enough precision, and guarantee higher accuracy. As listed in Table IV, when ADCs have only 3-bit precision, all systems have the inference accuracy as low as 10%, like randomly guessing. When ADCs have 4-bit precision, they all are increased to 62%, but still low. When the precision is improved to 5 and above, all accuries are increased over 90%.

TABLE III: Impact of ADC Precision on Honey-memristor Based Neuromorphic Systems with VGG8 Model

ADC	Device	Inference Accuracy
3	32	10%
4	32	62%
5	32	92%
3	16	10%
4	16	62%
5	16	92%
3	8	10%
4	8	61%
5	8	91%

D. Different Algorithms

In order to further verify the honey-memristor based neuromorphic systems, DenseNet-40 model is used in experiments. DenseNet is a neural network architecture that is designed to learn feature representations by densely connecting each layer to every other layer in a feed forward fashion. The use of dense connections in Densenet allows for more efficient use of parameters and better gradient flow during training, leading to improved performance. However, the use of dense connections in Densenet also increases the amount of computation that needs to be performed during inference. This increased computational load requires more precise computations and thus higher precision ADCs are needed in Densenet. Accordingly, as listed in Table IV, when ADCs have 3-5 bits, all inference accuracies are below 40%.

TABLE IV: Impact of ADC Precision on Honey-memristor Based Neuromorphic Systems with DenseNet-40 Model

ADC	Device	Inference Accuracy
3	32	10%
4	32	11%
5	32	39%
3	16	10%
4	16	11%
5	16	39%
3	8	10%
4	8	11%
5	8	39%

V. Comparison with State-of-The-Art

3D honey-memristor based neuromorphic systems realize the environmentally sustainable neuromorphic computing. As listed in Table V, as compared with other works, it stands out in terms of many criteria including Bio-degradable and Eco-friendly features, and has the accuracy as high as 92%. It also meets the requirements of device characteristics which makes it an efficient solution for a variety of AI applications.

VI. Conclusion

In this paper, honey-memristors are utilized to implement a 3D environmentally sustainable neuromorphic computing system. The experiment results indicate that the proposed systems with 8-, 16-, and 32-level devices have high inference accuracy over 90% even considering device variation and nonlinearity. Four conductance scenarios with three honey-memristors have been discussed for the retention analysis to show the great immunity against the device drift. ADC quantization effects and different algorithms (VGG8 and DenseNet-40) are also considered to further verify the effectiveness of systems regarding the inference accuracy. It concludes that as for VGG8 model, 5-bit ADCs are needed to guarantee over 90% accuracy, but DenseNet-40 model only has 39% inference accuracy even with 5-bit ADCs.

Acknowledgment

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References

[1] J. Edstrom, Y. Gong, A. A. Haidous, B. Humphrey, M. E. Mccourt, Y. Xu, J. Wang, and N. Gong, "Content-adaptive memory for viewer-aware energy-quality scalable mobile video systems," *IEEE Access*, vol. 7, pp. 47 479–47 493, 2019.

[2] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Team: Threshold adaptive memristor model," *IEEE transactions on circuits and systems I: regular papers*, vol. 60, no. 1, pp. 211–221, 2012.

[3] M. Oli-Uz-Zaman, S. A. Khan, G. Yuan, Z. Liao, J. Fu, C. Ding, Y. Wang, and J. Wang, "Mapping transformation enabled high-performance and low-energy memristor-based dnns," *Journal of Low Power Electronics and Applications*, vol. 12, no. 1, pp. 10–24, 2022.

TABLE V: Comparison with State-of-The-Art [32], [33]

Criteria	Ag:a-Si [34]	TaO_x/TiO_2 [35]	$PCMO$ [36]	AlO_x/HfO_2 [37]	TaO_x/TiO_{2-x} [38]	This Work
Bio-degradabl	×	×	×	×	×	√
Eco-friendly	×	×	×	×	×	√
Accuracy	72%	10%	10%	41%	93%	92%

[4] B. Govoreanu, G. S. Kar, Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. Radu, L. Goux, S. Clima, R. Degraeve *et al.*, "10×10nm 2 Hf/HfO_x crossbar resistive ram with excellent performance, reliability and low-energy operation," in *International Electron Devices Meeting*, 2011, pp. 31.6.1–31.6.4.

[5] S. C. Bartling, S. Khanna, M. P. Clinton, S. R. Summerfelt, J. A. Rodriguez, and H. P. McAdams, "An 8mhz 75μa/mhz zero-leakage non-volatile logic-based cortex-m0 mcu soc exhibiting 100% digital state retention at vdd = 0v with <400ns wakeup and sleep transitions," in *International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 432–433.

[6] Z. Liao, J. Fu, and J. Wang, "Ameliorate performance of memristor-based anns in edge computing," *IEEE Transactions on Computers*, vol. 70, no. 8, pp. 1299–1310, 2021.

[7] N. Sakimura, Y. Tsuji, R. Nebashi, H. Honjo, A. Morioka, K. Ishihara, K. Kinoshita, S. Fukami, S. Miura, N. Kasai *et al.*, "10.5 a 90nm 20mhz fully nonvolatile microcontroller for standby-power-critical applications," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 184–185.

[8] P.-F. Chiu, M.-F. Chang, C.-W. Wu, C.-H. Chuang, S.-S. Sheu, Y.-S. Chen, and M.-J. Tsai, "Low store energy, low vddmin, 8t2r nonvolatile latch and sram with vertical-stacked resistive memory (memristor) devices for low power mobile applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1483–1496, 2012.

[9] K.-H. Kim, S. Hyun Jo, S. Gaba, and W. Lu, "Nanoscale resistive memory with intrinsic diode characteristics and long endurance," *Applied Physics Letters*, vol. 96, no. 5, pp. 05 310.1–53 106.3, 2010.

[10] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov *et al.*, "Memristor-cmos hybrid integrated circuits for reconfigurable logic," *Nano letters*, vol. 9, no. 10, pp. 3640–3645, 2009.

[11] J. Fu, Z. Liao, J. Liu, S. C. Smith, and J. Wang, "Memristor-based variation-enabled differentially private learning systems for edge computing in iot," *IEEE Internet of Things Journal*, vol. 8, no. 12, pp. 9672–9682, 2020.

[12] E. C. Apollos, S. A. Adeshina, and N. A. Nnanna, "Memristor-based cim architecture for big data era," in *2019 15th International Conference on Electronics, Computer and Computation (ICECCO)*, 2019, pp. 1–6.

[13] V. Gupta, S. Kapur, S. Saurabh, and A. Grover, "Resistive random access memory: a review of device challenges," *IETE Technical Review*, vol. 37, no. 4, pp. 377–390, 2020.

[14] M. Oli-Uz-Zaman, S. A. Khan, W. Oswald, Z. Liao, and J. Wang, "Stuck-at-fault immunity enhancement of memristor-based edge ai systems," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 12, no. 4, pp. 922–933, 2022.

[15] W.-P. Lin, S.-J. Liu, T. Gong, Q. Zhao, and W. Huang, "Polymer-based resistive memory materials and devices," *Advanced materials*, vol. 26, no. 4, pp. 570–606, 2014.

[16] T. Younkin. (2022) Creating the future, together. [Online]. Available: https://www.src.org/about/sustainability/

[17] B. Sueoka, K. Cheong, and F. Zhao, "Natural biomaterial honey based resistive switching device for artificial synapse in renewable neuromorphic systems and bioelectronics," *Applied Physics Letters*, vol. 120, no. 8, p. 083301, 2022.

[18] B. Sueoka and F. Zhao, "Memristive synaptic device based on a natural organic material - honey for spiking neural network in biodegradable neuromorphic systems," *Journal of Physics D: Applied Physics*, vol. 55, no. 22, p. 225105, 2022.

[19] B. Sueoka, K. Cheong, and F. Zhao, "Study of synaptic properties of honey thin film for neuromorphic systems," *Materials Letters*, vol. 308, p. 131169, 2022.

[20] B. Sueoka, M. Tanim, L. Williams, Z. Xiao, K. Cheong, and F. Zhao, "Neural facilitation in natural honey-based resistive switching artificial synaptic devices," *Organic Electronics*, vol. 109, p. 106622, 2022.

[21] M. Tanim, B. Sueoka, Z. Xiao, K. Cheong, and F. Zhao, "Study of carbon nanotube embedded honey as a resistive switching material," *Nanotechnology*, vol. 33, no. 49, p. 495705, 2022.

[22] B. Sueoka, A. Vicenciodelmoral, M. Tanim, X. Zhao, and F. Zhao, "Correlation of natural honey-based rram processing and switching properties by experimental study and machine learning," *Solid-State Electronics*, vol. 197, p. 108463, 2022.

[23] A. Sivkov, Y. Xing, K. Cheong, X. Zeng, and F. Zhao, "Investigation of honey thin film as a resistive switching material for nonvolatile memories," *Materials Letters*, vol. 271, p. 127796, 2020.

[24] J. Fu, Z. Liao, N. Gong, and J. Wang, "Mitigating nonlinear effect of memristive synaptic device for neuromorphic computing," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 9, no. 2, pp. 377–387, 2019.

[25] S. A. Khan, M. Oli-Uz-Zaman, and J. Wang, "Pawn: Programmed analog weights for non-linearity optimization in memristor-based neuromorphic computing system," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 13, no. 1, pp. 436–444, 2023.

[26] J. Fu, Z. Liao, N. Gong, and J. Wang, "Linear optimization for memristive device in neuromorphic hardware," in *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2019, pp. 453–458.

[27] M. Oli-Uz-Zaman, S. A. Khan, G. Yuan, Y. Wang, Z. Liao, J. Fu, C. Ding, and J. Wang, "Reliability improvement in rram-based dnn for edge computing," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2022, pp. 581–585.

[28] P.-Y. Chen, X. Peng, and S. Yu, "Neurosim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3067–3080, 2018.

[29] X. Peng, S. Huang, H. Jiang, A. Lu, and S. Yu, "Dnn+neurosim v2.0: An end-to-end benchmarking framework for compute-in-memory accelerators for on-chip training," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 40, no. 11, pp. 2306–2319, 2020.

[30] P.-Y. Chen and S. Yu, "Reliability perspective of resistive synaptic devices on the neuromorphic system performance," in *IEEE International Reliability Physics Symposium (IRPS)*, 2018, pp. 5C–4.

[31] X. Peng, S. Huang, A. Lu, and S. Yu. (2021) User manual of 3d+neurosim framework v1.0. [Online]. Available: https://github.com/neurosim/3D_NeuroSim_V1.0

[32] J. Fu, Z. Liao, and J. Wang, "Memristor-based neuromorphic hardware improvement for privacy-preserving ann," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 12, pp. 2745–2754, 2019.

[33] P.-Y. Chen and S. Yu, "Technological benchmark of analog synaptic devices for neuroinspired architectures," *IEEE Design and Test*, vol. 36, no. 3, pp. 31–38, 2019.

[34] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano letters*, vol. 10, no. 4, pp. 1297–1301, 2010.

[35] L. Gao, I.-T. Wang, P.-Y. Chen, S. Vrudhula, J.-s. Seo, Y. Cao, T.-H. Hou, and S. Yu, "Fully parallel write/read in resistive synaptic array for accelerating on-chip learning," *Nanotechnology*, vol. 26, no. 45, p. 455204, 2015.

[36] S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. R. Lee, B. H. Lee, and H. Hwang, "Neuromorphic speech systems using advanced reram-based synapse," in *2013 IEEE International Electron Devices Meeting*, 2013, pp. 25.6.1–25.6.4.

[37] J. Woo, K. Moon, J. Song, S. Lee, M. Kwak, J. Park, and H. Hwang, "Improved synaptic behavior under identical pulses using alox/hfo2 bilayer rram array for neuromorphic systems," *IEEE Electron Device Letters*, vol. 37, no. 8, pp. 994–997, 2016.

[38] J. Fu, Z. Liao, and J. Wang, "Level scaling and pulse regulating to mitigate the impact of the cycle-to-cycle variation in memristor-based edge ai system," *IEEE Transactions on Electron Devices*, vol. 69, no. 4, pp. 1752–1762, 2022.