Check for updates

ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Scalable Nanoimprint Manufacturing of Functional Multilayer Metasurface Devices

Shinhyuk Choi, Jiawei Zuo, Nabasindhu Das, Yu Yao, and Chao Wang**

Optical metasurfaces, consisting of subwavelength-scale meta-atom arrays, hold great promise of overcoming the fundamental limitations of conventional optics. Due to their structural complexity, metasurfaces usually require high-resolution yet slow and expensive fabrication processes. Here, using a metasurface polarimetric imaging device as an example, the photonic structures and the Nanoimprint lithography (NIL) processes are designed, creating two separate NIL molds over a patterning area of > 20 mm^2 with designed Moiré alignment markers by electron-beam writing, and further subsequently integrate silicon and aluminum metasurface structures on a chip. Uniquely, the silicon and aluminum metasurfaces are fabricated by using the nanolithography and 3D pattern-transfer capabilities of NIL, respectively, achieving nanometer-scale linewidth uniformity, sub-200 nm translational overlay accuracy, and <0.017 rotational alignment error while significantly reducing fabrication complexity and surface roughness. The micro-sized multilayer metasurfaces have high circular polarization extinction ratios as large as ≈20 and ≈80 in blue and red wavelengths. Further, the metasurface chip-integrated CMOS imager demonstrates high accuracy in broad-band, full Stokes parameter analysis in the visible wavelength ranges and single-shot polarimetric imaging. This novel, NIL-based, multilayered nanomanufacturing approach is applicable to the scalable production of large-area functional structures for ultra-compact optic, electronic, and quantum devices.

1. Introduction

Metasurfaces are capable of manipulating fundamental electromagnetic responses, i.e., phase, amplitude, frequency, and polarization,[1–4] at subwavelength scale. They have shown great potential in addressing the fundamental limitations of conventional bulky optical systems and realizing ultracompact optical devices and systems for many applications, such as holography, imaging, spectroscopy, beam shaping, and steering, etc.[5–10] Despite significant progress in metasurface design and proof-of-concept laboratory demonstrations,[11] scalable and cost-effective nanomanufacturing remains one of the major challenges that slow down commercialization of metasurface devices. Conventional prototyping nanofabrication methods, such as electron-beam lithography (EBL) or focused-ion beam (FIB), rely on pixel-by-pixel writing for precise nanopatterning but are not suitable for scalable manufacturing due to long writing time over a large scale.[12] High-resolution semiconductor optical lithography technologies (such as deep-UV or extreme-UV lithography)[13] are ideal for high-throughput production, but are too expensive and complex for prototyping demonstrations. In comparison, nanoimprint lithography (NIL) is suitable for both prototyping demonstration and large-scale production of nanostructures as small as sub-ten nanometers[14] given its unique, optical diffraction-free, parallel patterning capabilities.[15–17] Previously, NIL has been employed successfully in a wide range of optical applications, such as polarizers,[18,19] anti-reflection coatings,[20] light absorbers,[21–23] image or color displays,[24–26] biosensing,[27,28] etc., and demonstrated feasible for geometrically simple, stand-alone, single-layer metasurface structures.[29–32] In addition, various manufacturing methods have been attempted to create quasi-3D metasurface structures (Table S1, Supporting Information), such as stacking NIL-produced bilayer nanostructures,[33–35] angle deposition,[36] etc. The bi-layer structures were formed by manually adjusting the offset angles of periodically patterned structures, such as metallic and dielectric nanogratings,[33] hexagonal nanoholes in photoresist,[34] and nanosphere particles,[35] during NIL to form the stacked layers. The angle-deposition method[36] produced 3D serpentine-shaped structures that were defined by the original structural geometries, deposition angles, and material thicknesses. Despite interesting demonstrations, these methods relied on the structural periodicity and/or geometry rather than

S. Choi, J. Zuo, N. Das, Y. Yao, C. Wang
School of Electrical
Computer and Energy Engineering
Arizona State University
Tempe, AZ 85287, USA
E-mail: yuyao@asu.edu; wangch@asu.edu
Y. Yao, C. Wang
Centre for Photonic Innovation
Arizona State University
Tempe, AZ 85287, USA
C. Wang
Biodesign Center for Molecular Design and Biomimetics
Arizona State University
Tempe, AZ 85287, USA

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202404852

DOI: 10.1002/adfm.202404852

 © 2024 Wiley-VCH GmbH

engineered alignment strategies to achieve precise lateral or rotational alignment control, and therefore are not feasible to integrate functional structures with more complex structure geometries and/or stringent alignment demands, particularly in a complementary metal-oxide-semiconductor (CMOS)-processing compatible fashion.

In this work, we strategically establish a scalable NIL integration approach that is potentially compatible with semiconductor CMOS processes toward manufacturing of metasurfaces over multiple layers, creating subwavelength-thick, functional, metasurface polarization filter arrays (MPFAs) on a chip for full-Stokes parameter analysis and integrating such MPFA chips on a CMOS imager to demonstrate its polarimetric imaging capability. Here NIL was carried out in two steps to produce two sets of nanostructures in dielectric (silicon, or Si) and metallic (aluminum, or Al) materials over an area of 4 mm by 5.2 mm with precise dimensional control (<4 nm in linewidth standard deviation) separated by a dielectric (silicon oxide, or SiO_2) spacer layer. Uniquely, NIL was used as a lithographic technique to faithfully pattern nanostructures in Si metasurface, and then explored as a transfer-printing method to replicate the 3D geometries of the NIL mold into the imprint resist, which directly functioned as a scaffold for the Al metasurface. For precise alignment of the Si and Al metasurfaces, Moiré alignment markers were placed onto both of the NIL molds along with the designed functional nanostructures, which in this work were organized into micrometer-sized arrays and contained dense nanogratings, to achieve a high alignment accuracy (interlayer translational alignment error ≈200 nm, rotational error < 0.017 degrees) between the Si and Al metasurfaces. These vertically integrated microarrays, i.e., MPFAs, functioned as polarimetric imaging pixels, consisting of broadband linear polarization (LP) filters, i.e., grating polarizers in the Al metasurface, and selectively patterned circular polarization (CP) filters across visible wavelength bands (500± 20 nm, 550± 20 nm, and 600± 20 nm) from overlaid multilayer nanostructures. Finally, the metasurface chips were bonded onto CMOS imaging sensors, thus enabling broadband polarimetric imaging and full-Stokes parameter analysis across the different colors at a high accuracy (<5%). Using MPFAs as an example, we showed that the NIL-fabricated devices presented a much smoother surface (4 nm roughness) and gratings compared to EBL-MPFAs (≈16 nm), attributed to the in situ planarization capability of NIL, and the NIL-MPFAs produced much enhanced CP extinction ratios (CPER of ≈20 and ≈80 at blue and red color wavelengths) that are a few times better than EBL ones (≈2 and 20). This significant improvement in optical performance was attributed to our co-designed and greatly simplified manufacturing strategy that minimized fabrication complexity, reduced structure damages owing to minimized defect-generating processing steps (e.g., etching, liftoff, etc.), and suppressed optical scattering loss due to in situ surface planarization. This successful multilayer NIL-metasurface integration approach can be adapted to the fabrication of many other metasurface structures toward high-throughput scalable manufacturing of various metasurface devices, which have broad applications in both rapid prototyping and large-scale production of ultra-compact chip-integrated optic, optoelectronic, electronic, and quantum devices, and systems.

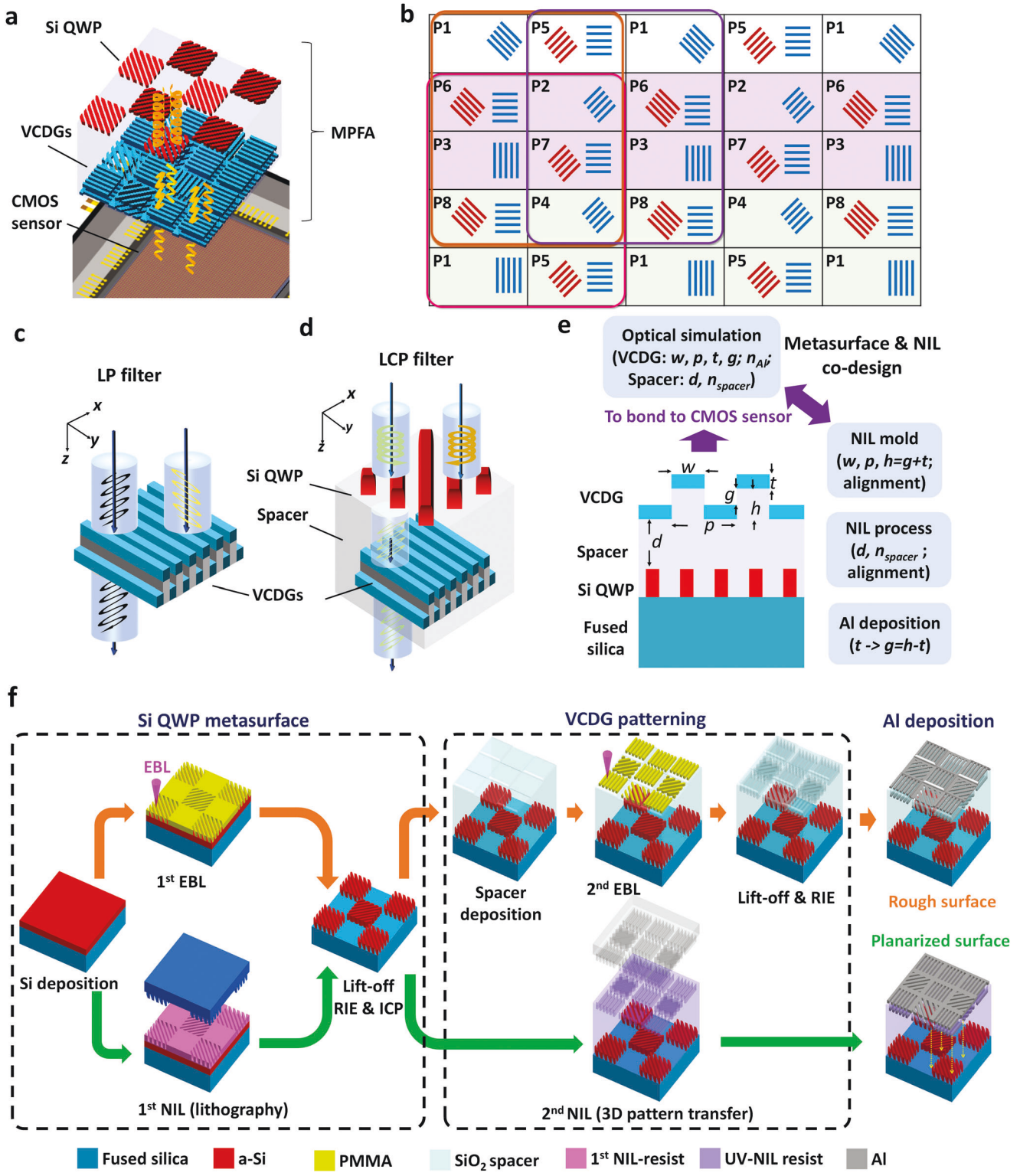
2. Scalable Manufacturing Design and Process

Here, we present a synergistic approach to co-design the multilayered optical metasurfaces and their scalable NIL manufacturing process. Our exemplary polarimetric imaging system was a multilayered metasurface polarization filter array (MPFA) integrated into a CMOS imaging sensor (**Figure 1**a). The MPFA consisted of over 43000 superpixels over an area of 4 mm by 5.2 mm, each having four LP filter pixels and four CP filter pixels (Figure 1b) to ensure accurate full-Stokes polarization measurement. The LP filters were based on vertically coupled double-layer gratings (VCDGs) with a high LP extinction ratio (LPER) over a broad wavelength range (Figure 1c). The CP filters were based on multilayered chiral metasurface structures, consisting of a Si metasurface acting as a quarter wave plate (QWP) (Figure S1, Supporting Information), a dielectric (SiO_2) spacing layer, and VCDGs as LP filters (Figure 1d). Overall, the MPFAs were formed by two levels of vertically aligned, functional structures, i.e., the Si metasurface and the VCDG (Figure 1a,b). In the Si metasurface level, each superpixel had four blank pixels (no nanopatterns, pixels 1 to 4, Figure 1b) and four pixels made of Si nanostructures (pixels 5 to 8). In the VCDG level, the grating polarizers were present in all eight pixels, oriented along 0°, 45°, 90°, or 135° in the 4 LP filters and all along 90 in the four CP filters (Figure 1b). To achieve a broadband coverage in visible (450 to ≈700 nm), two sets of CP filters (VCDGs overlaid to Si metasurface) were designed with broad CPER peak bandwidths, one for green-wavelength operation (520 to 620 nm, pixels seven and eight, Figure 1b), and the other (pixels 5 and 6) for both blue (450 to 520 nm) and red wavelengths (600 to 670 nm) (designs parameters and simulation results in **Table 1**; Figure S2, Supporting Information). This design enabled a single-shot, full-Stokes polarimetric analysis and imaging over a broad bandwidth in visible wavelengths. Further, the LP and CP filter pixels were all shared by neighbor superpixels in the MFPA layout, thus maximizing the number of effective superpixels for optimal imaging resolution. Here the MPFAs were fabricated on a transparent silica substrate and then integrated into a commercial CMOS imaging sensor via polymer-assisted wafer bonding. The process can be readily modified to directly integrate the metasurface onto CMOS chips for wafer-scale production.

Previously, an EBL-based process (Figure 1f top, indicated by orange arrows) was developed by us to fabricate the MPFAs;[37] however, the fabrication was quite complex and expensive, requiring extensive EBL writing time, repeated film deposition, lift-off and etching. Furthermore, the SiO_2 spacer on top of the Si metasurface had a rough surface, which resulted in uneven Al grating surfaces in the VCDGs and limited the polarization selectivity, i.e., LPER and CPER. Motivated by these challenges, we here propose and demonstrate a fundamentally different NIL technology toward scalable multilayer device integration with improved optical performance. Specifically, NIL (Figure 1f bottom, indicated by green arrows) was used first as a high-throughput, high-resolution lithographic technology to pattern Si metasurface gratings by thermal NIL (followed by metal liftoff and etching), and then used as a 3D transfer-printing process to produce the VCDG grating scaffold with the NIL mold geometries preserved in UV-NIL resists, which also acted as a SiO_2-comparable

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License



© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Table 1. Designed structural geometries of metasurface filters.

Filter Function	Working wavelength	Metasurface structure	Period	Grating width	Duty cycle	Thickness and vertical gap	Spacer layer thickness
CP filter for red and blue	Red: 600–670 nm; Blue: 450–520 nm	Si grating	297 nm	100 nm	33.6%	130 nm Si	520 nm
		VCDG	210 nm	105 nm	50%	80 nm Al; 30 nm vertical gap	
CP filter for green	520-620 nm	Si grating	180 nm	70 nm	38.9%	130 nm Si	520 nm
		VCDG	180 nm	90 nm	50%	80 nm Al; 30 nm vertical gap	
Broadband LP filter	450 –700 nm	VCDG	210 nm	105 nm	50%	80 nm Al; 30 nm vertical gap	NA

spacer layer. Moiré patterns were created on both of the two NIL molds to achieve a high overlay accuracy over the patterned areas (4 mm by 5.2 mm, or ≈0.2 cm^2). Very uniquely, the UV-NIL not only effectively transfer-printed 3D grating structures as the VCDG scaffold, but also eliminated multiple manufacturing steps and planarized the resist. Therefore, this innovative NIL integration strategy simultaneously reduced processing complexity, improved performance, and enabled scalable device production.

In this work, the metasurface design required complex patterning of dense and small structures in S and aluminum (period as small as 180 nm and linewidth as small as 70 nm, see Table 1) with different geometries, orientations, and dimensions to act as QWPs and polarizers, respectively, in the vertically stacked MPFAs. Therefore, EBL writing was chosen to create the NIL molds for its design flexibility and high resolution. A low EBL writing current (and therefore a long writing time) was needed for accurate control of structural geometry but in practice limited the demonstrated patterning to 4 mm by 5.2 mm even after 16-h writing. This area size was designed intentionally to the size of a CMOS imager sensor for on-chip polarimetric imaging demonstration. Noticeably, NIL is many times faster than EBL once a mold is available (Table S2, Supporting Information), and its high throughput advantage can be further manifested when scaling to even bigger areas if the molds can be made larger by more advanced lithography tools, such as deep-UV or extreme-UV lithography (Table S3, Supporting Information). Nevertheless, the use of the MPFAs as an example allows us to establish this new manufacturing approach and quantitatively evaluate the device performance by comparing NIL with EBL-based integration processes.

To optimize the manufacturing throughput and device performance, we identified key design parameters closely relevant to NIL processes and crucial to the performance of Si QWP and the VCDGs (Figure 1e and Table 1). At the Si QWP metasurface level, dense gratings of 180 or 297 nm in period and linewidths of 70 or 100 nm are needed for CP polarization filters of green or blue/red operational wavelengths (Figure S2, Supporting Information). Optical simulation results (Figure S3, Supporting Information) indicated that small variations of the Si grating linewidth only slightly modulate the optimal CPER values and the peak wavelengths, showing a high design tolerance. At the VCDG level, the grating period (p), controlled by the NIL mold structure design, and width (w), determined by UV-NIL and subsequent processing conditions, both had a strong influence on the LPER and optical transmission. The duty cycle (w/p) was designed at 50% with a tolerance of ±20% to obtain a high LPER of over 1000 in visible (Figure S4, Supporting Information). The vertical gaps between the Al VCDGs (g) were practically determined by the designed mold height and experimentally optimized Al thicknesses to maximize the LPER. Further, the spacing between the VCDGs and the Si nanostructures (d) also strongly affects the wavelength ranges to achieve the best MPFA performance (Figure S5, Supporting Information), as it affects the phase accumulation of electromagnetic waves traveling between the two layers upon reflection.

2.1. Silicon Metasurface Fabrication

The Si metasurface-based, microscale QWP array was fabricated by thermal-NIL for its simplicity, using a NIL mold fabricated on a thermal SiO_2-coated silicon wafer (**Figure 2**a). We first made the NIL mold by EBL patterning, chromium (Cr) hard mask deposition and liftoff, reactive ion etching (RIE) of SiO_2, and Cr stripping (Experimental Section and Figure S6, Supporting Information). Then the Si metasurface was fabricated from α-Si thin

Figure 1. Conceptual designs of scalable NIL manufacturing for multilayer metasurface polarization filter arrays (MPFAs). a) Illustration of integrating the broadband MPFAs onto a CMOS sensor. The MPFAs consist of a-Si metasurface level as a quarter waveplate (QWP) and a VCDG level as linear polarizers. Here two CP designs targeting green and blue/red spectra (indicated by arrows) are incorporated for the Si metasurface structures. b) Illustration of the arrangement of metasurface polarization filter arrays (pixels) within super-pixels (rectangular boxes). Red lines indicate silicon metasurfaces in the top layer and blue lines indicate VCDG metasurfaces in the bottom layer of the MPFA structures. Here P1-P4 have only VCDGs that transmit 0°, 90°, 45°, 135° LP light, respectively. P5–P8 are chiral metasurfaces constructed by Si QWP and VCDGs in each pixel that transmit RCP and LCP in red and blue color range (P5 and P6, red shaded) and green color range (P7 and P8). c) Schematic illustration of VCDGs to pass light polarized along the x-axis but block light polarized along the y-axis. d) Schematic of multilayer CP filter transmitting LCP but blocking RCP incoming light. d) A co-design concept to produce the VCDGs on Si metasurface structures based on NIL. Here the structural geometries and processing conditions are designed for optimal performance. e) Schematics showing the EBL (top, following orange arrows) and NIL (bottom, following green arrows) based fabrication processes for MPFAs. Here a 1st thermal NIL replaces EBL for the fabrication of Si metasurface, and a 2nd UV-NIL creates a nanostructured scaffold to be converted into VCDGs after Al evaporation.

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

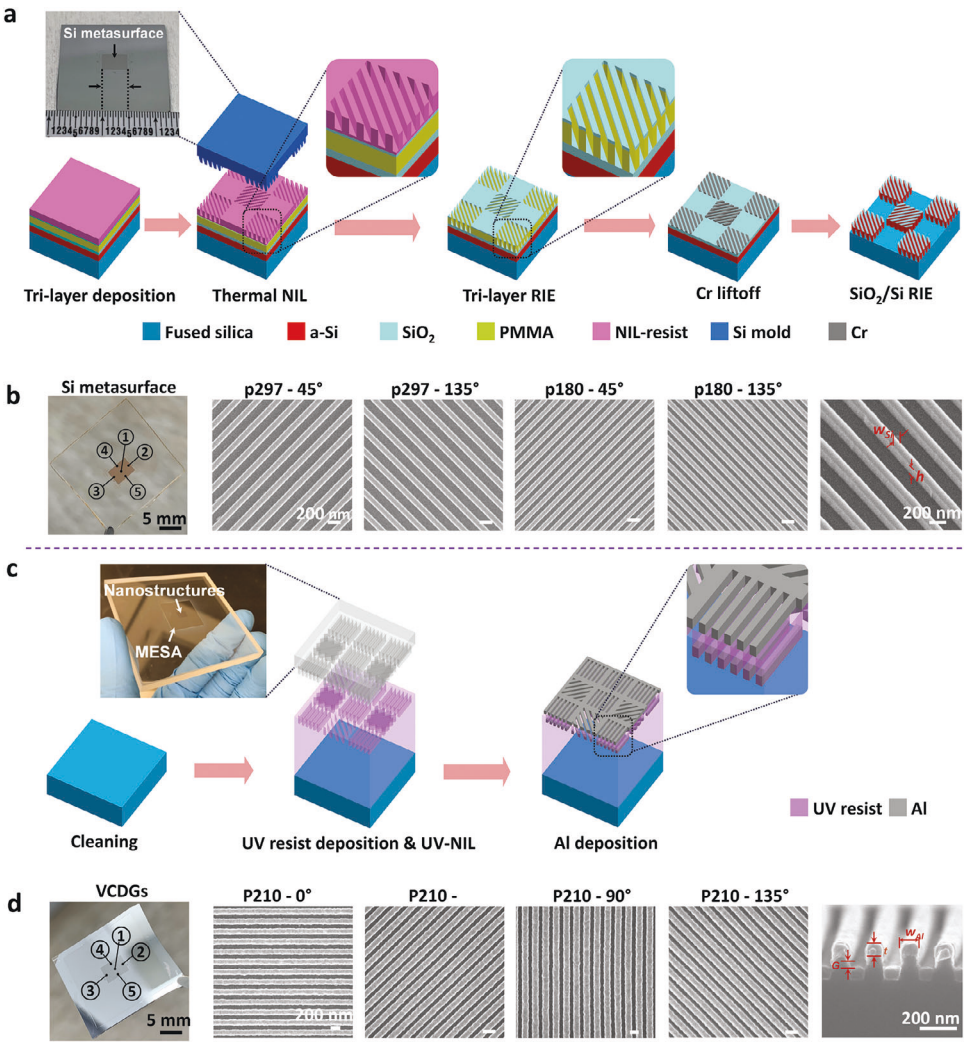


Figure 2. Schematics and fabrication results of Si and VCDG metasurface structures. a) Fabrication process of Si metasurface via thermal NIL on a tri-layered resist structure, including polymethyl methacrylate (or PMMA, bottom), SiO_2 (middle, evaporated) and thermoplastic NIL resist (top). The key processing steps include NIL, RIE of the tri-layer stack, Cr evaporation and liftoff, SiO_2 RIE, Cr stripping, and Si RIE. The top-left insert optical image shows the Si metasurface NIL mold made in a Si wafer. b) Fabricated Si metasurface structures on fused silica. Left: optical image of a fabricated Si metasurface chip (scale bar: 5 mm). Middle: top-view SEM images of unit pixel arrays. Right: side-view SEM image of Si gratings. Scale bar: 200 nm for SEM images. c) Illustration of the fabrication process of VCDGs by UV-NIL followed by Al evaporation. The top-left insert optical image shows the VCDG mold made in fused silica. d) Fabricated VCDG grating structures. Left: optical image of VCDG gratings on a silicon sample for structural inspection (scale bar: 5 mm). Middle: top-view SEM images of unit pixel arrays. Right: a cross-sectional view of fabricated VCDGs after Al deposition, with the key geometrical dimensions highlighted (*g*: gaps between the two sets of Al gratings; *t*: Al thickness; *w*: grating width). Scale bar: 200 nm for SEM images. In Figures (b) and (d), five areas are randomly chosen from the chips to examine the fabrication uniformity: ① Center, ② Right, ③ Left, ④ Top, and ⑤ Bottom. The measured structural dimensions are given in Table S3 (Supporting Information).

film deposited by chemical-vapor deposited (CVD) using a tri-layer pattern-transfer scheme (Experimental Section). Compared to a single-layer resist, the tri-layer film stack could effectively produce high-aspect-ratio nanostructures with improved patterning uniformity over a large area by reducing dimensional distortion and improving the success in Cr liftoff,[38,39] thus favorable for subsequent high-fidelity pattern transfer to the underneath Si metasurface gratings. Additionally, the grating linewidth could be adjusted within a range of about 30 nm by modulating the etching time of the top thermoplastic NIL resist, offering additional flexibility in controlling structure dimensions. The linewidths of Si metasurface gratings were inspected by scanning electron microscopy (SEM) at five different locations of the sample (Figure 2b). and the linewidth variations were found less than 4 nm for all the array designs (**Table 2**), thus confirming good uniformity of the NIL process for large-scale nanomanufacturing of Si metasurface.

2.2. NIL 3D Scaffolding for Metallic Grating Metasurface (VCDG)

The VCDG linear polarizer arrays were fabricated using UV-NIL with a NIL mold fabricated on a transparent fused silica wafer (Figure 2c) for precise vertical stacking and overlay onto

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Table 2. Metasurface grating linewidths of NIL-fabricated Si metasurface and VCDGs. (Unit: nm).

	Si metasurface: W_{si}				VCDGs: W_{Al}			
	$P_{297,\,45°}$	$P_{297,\,135°}$	$P_{180,\,45°}$	$P_{180,\,135°}$	$P_{210,\,0°}$	$P_{210,\,90°}$	$P_{210,\,45°}$	$P_{210,135°}$
①Center	111.2	112.9	91.9	91.7	116.1	115.8	109.2	109.5
②Right	113.4	113.7	91.9	89.6	116.2	115.9	109.1	109.3
③Left	113.0	113.2	92.2	90.9	116.1	115.9	109.2	109.1
④Top	116.3	109.2	91.6	88.8	116.6	116.1	109.2	108.6
⑤Bottom	114.9	119.1	95.5	95.1	116.6	116.3	110.0	108.9
Average	113.8±2.6	113.6±3.8	92.6±2.1	91.1±2.7	116.3±1.3	116.0±1.3	109.4±1.4	109.1±1.7

Si metasurface. The VCDG mold fabrication process was similar to that for the Si metasurface NIL mold, with more details in the Experimental Section. Briefly, the nanostructured mold was intentionally patterned on an etched mesa (Figure S7, Supporting Information) to further improve the NIL pressure, which was beneficial to high imprinting quality. To examine the VCDG NIL process, we coated a Si wafer with an acrylate-based, UV-curable resist and performed UV-NIL on the sample. The NIL transferred the nanograting patterns into the UV resist (optical index very close to SiO_2, Figure S8, Supporting Information) that was more resistant to oxygen plasma damage or heating in metal deposition than organic polymers. Without need of any additional etching or liftoff, the UV NIL resist served perfectly as a rigid, transparent VCDG scaffold, and preserved precisely both the lateral and vertical dimensions of the grating structures from the NIL mold. Subsequently, VCDG fabrication was completed by a simple Al deposition (thickness t) to produce desired vertical gaps ($g = h\text{-}t$) (Figure 1e). Essentially, this single NIL-based pattern transfer-printing step replaced multiple manufacturing steps otherwise needed for EBL fabrication (Figure 1f), including SiO_2 spacer deposition, EBL writing, plasma descum, Cr deposition, liftoff, SiO_2 dry etching, and Cr removal, therefore greatly improving the throughput and minimizing feature distortion. The linewidth SDs of VCDGs were measured <2 nm (Table 2) from SEM images taken at five randomly selected locations across the chips (Figure 2d). The linewidth of angled gratings (116 nm for 45° and 135°, respectively) was found slightly different from vertical and horizontal gratings (109 nm for 90° and 0°, respectively). This difference was mainly attributed to manufacturing variations in the VCDG mold during EBL-based pattern generation and writing process, but was still within the acceptable range for VCDG grating polarizers (Figure S4, Supporting Information). Further, we optimized the Al film deposition conditions to minimize the roughness (Figure S9, Supporting Information), experimentally analyzed the impact of Al thickness (t) on the optical performance of VCDGs (Figure S10, Supporting Information) for optimal LPER, and chose here to have $t = 80$ nm.

2.3. Vertical Alignment and Integration

NIL-based multi-layer metasurface fabrication usually faces two major challenges: 1) precise alignment between the different layers, and 2) the adverse impacts of existing surface topography on the subsequent NIL fabrication.

Table 3. Optically measured cross-square mark gaps and alignment errors. (Unit: μm).

	x-direction			y-direction		
	G_1	G_2	Error Δ_x	G_3	G_4	Error Δ_y
AM_1	1.69	1.79	0.05	1.59	1.89	0.15
AM_2	1.64	1.84	0.10	1.64	1.85	0.10
AM_3	1.82	1.64	0.09	1.82	1.65	0.09
AM_4	1.86	1.62	0.12	1.93	1.55	0.19

To achieve submicron optical alignment for vertical stacking of the VCDG and Si metasurface micro-filter arrays, we designed and fabricated interference-based Moiré patterns[40,41] (**Figure 3a**) on both NIL molds for Si metasurfaces and VCDGs. Here, two sets of gratings with slightly different periods acted as Moiré marks to produce interference patterns with a period P_{fringe}, calculated as $P_{fringe} = P_1 \cdot P_2/(P_2 - P_1)$. Therefore, the theoretical misalignment between the two metasurfaces ($\Delta = G_i - G_j$) could be made much smaller than the visualized Moiré fringe offset (s) as $\Delta = s(P_2 - P_1)/P_1 << s$ when $P_2 \sim P_1$, thus resulting in nanometer-scaled alignment accuracy. When in good alignment, Moiré fringe minima were clearly positioned next to our designed small square and cross marks on the two metasurface layers that served as alignment indicators in each of the alignment mark groups (e.g., AM_1 and AM_2, Figure 3a). Because the thick NIL resist spacer layer blocked electron beam signals but allowed optical visualization, we chose optical microscopy to measure the gaps between the square and cross marks in both x- and y-directions, and determined the translational alignment errors (Δ_1, Δ_2, Δ_3, and Δ_4 for the four alignment mark sets) from the size differences of these gaps G, e.g. $\Delta = |G_1 - G_2)/2|$. The measured alignment errors were found below 200 nm in both x- and y-directions within the mm-scaled structure (**Table 3**), much smaller than our MPFA design requirement of ≈1.6 μm, which was needed to overlay the 4.65 × 4.65 μm² VCDG arrays (Figure 3c bottom, grey squares) to 7.75 × 7.75 μm² Si metasurface arrays (Figure 3c bottom, red squares). The Moiré marks can be designed to achieve much higher overlay accuracy by engineering the optical scanning, stage, and control systems, e.g., sub-10 nm overlay is routinely achieved on ASML scanners using fundamentally similar interferometric marks for larger-scale production. Nevertheless, the Moiré alignment method allows future integration of

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

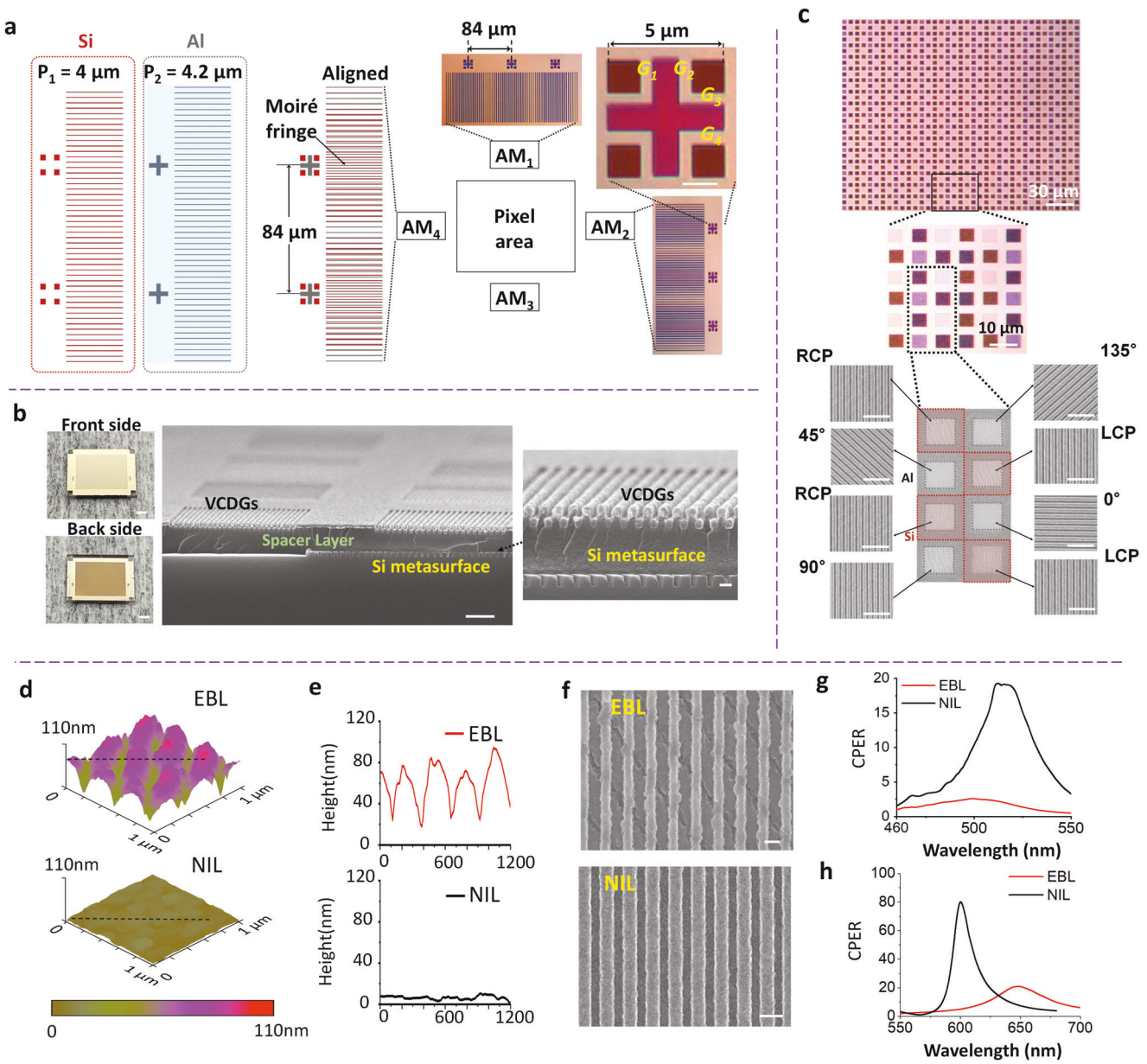


Figure 3. NIL integration of multilayer MPFA chips. a) Moiré fringe-based alignment technique to achieve nano-scale overlay accuracy. Optical images of the top and right alignment marks (AM1 and AM2) showed clear interference patterns produced next to the designed cross-square marks. The images of cross-square marks were used for alignment accuracy analysis (scale bar: 5 μm). b, Integrated multi-layer metasurface chip. Left: Optical images of the diced chip (top: VCDGs-side up; bottom: α-Si side up. Scale bar: 1 mm) Middle and right: representative cross-sectional SEM image of integrated multi-layer metasurface structures (scale bar: 1 μm for middle image, and 200 nm for right image). c) Microscopic images of fabricated MPFAs. Top and middle: optical images (scale bar: 30 μm for the top and 10 μm for the middle). Bottom: representative SEM images of a super-pixel consisting of eight individual pixels (scale bar: 1 μm). The Si and Al metasurface pixels are indicated by red and grey shades overlaid to the SEM images. d) AFM images of a non-patterned area from an MPFA chip fabricated by EBL (top) and NIL (bottom) to show the surface roughness. e) Surface roughness profiles extracted from the AFM images in (d). f) SEM images of Al grating nanostructures from EBL (top) and NIL (bottom) fabricated MPFAs. g–h) Comparison of CPER of LCP filters fabricated by NIL (black) and EBL (red): g) at 460–550 nm, and h) at 550–680 nm, respectively.

metasurface structures with reduced pixel sizes, e.g., to submicron with our demonstrated NIL capability or even smaller on more advanced systems, thus further improving the imaging sensor pixel density and resolution.

On the other hand, the surface topography resulting from the selectively fabricated Si metasurface (Figure S10, Supporting Information) strongly affected subsequent VCDG fabrication. Applying NIL on the Si metasurface as a conventional lithography tool would face a few serious challenges. First, as a contact-based lithographic technology, the NIL process typically prefers a flat substrate for high-resolution, low-defect pattern replication,[42] because existing nanostructures (e.g., ≈160 nm tall gratings in

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

selectively patterned areas here) could disrupt the resist flow, trap air bubbles and create defects. Further, using a much thicker NIL resist layer, for instance about twice the height of the Si gratings, although could mitigate the defect problem during NIL, would create non-uniform and substantial residual layers in some areas, e.g., the empty pixels without nanostructures. This, in turn, would lead to a much longer residual layer etching during pattern transfer, and could cause structural distortion, dimensional expansion, and/or defects. In fact, we attempted to replace EBL with NIL to lithographically pattern the VCDGs on SiO_2 spacer-coated Si metasurfaces for Cr liftoff and SiO_2 etching (Figure S11a–f, Supporting Information), similar to the EBL fabrication scheme (Figure 1f). Clearly, even though we utilized a pre-NIL polymer planarization process to help minimize NIL defects and designed a tri-layer UV resist stack to improve the yield of pattern transfer, the Cr patterns after liftoff suffered serious linewidth distortion, polymer residue contamination, and poor line roughness. To circumvent these problems, UV-NIL was instead employed as a 3D transfer-printing technology to produce uniform nanostructures in the resist as a VCDG scaffold, which readily functioned as a template to complete VCDG fabrication through an Al evaporation and simultaneously acted as a SiO_2-like dielectric spacer layer between the Si and VCDG metasurfaces. Therefore, this method eliminated complex, structure-damaging fabrication steps (such as etching, liftoff, etc.) to best preserve the printed nanostructure geometries. Compared to EBL-fabricated chips that displayed a wobbling surface (up to ≈80 nm modulation across ≈100 nm distance, and root mean square roughness ≈15.6 nm, from a 1 μm^2 flattened area without gratings, Figure 3d,e top), UV-NIL effectively planarized the substrate surface to have a much-reduced roughness (≈1.2 nm, Figure 3d,e bottom). Accordingly, the VCDGs overlaid on the Si metasurface had very small grating linewidth SDs of <4 nm from SEM imaging (Table S4, Supporting Information), comparable to that of VCDG structures fabricated on a flat substrate (≈2 nm, Table 2). Clearly, the in situ planarization, which was attributed to the effective resist filling owing to the low viscosity of the UV resist layer, allowed us to faithfully produce a nanograting scaffold from the NIL mold. This success demonstrated the feasibility of precise NIL nanopatterning over selectively patterned, significant protruding topography from underlying metasurfaces, which poses serious challenges in high-yield NIL fabrication.

We also performed optical spectroscopic measurements of the integrated multi-layer metasurfaces and compared the performance of EBL- and NIL-fabricated MPFA samples (Figure 3g,h). The transmission efficiencies from the NIL device were lower than the designed value, attributed to the fact that the VCDG mold after timed RIE had rounded trench edges in amorphous silica, which subsequently produced rounded shoulders in the VCDG scaffold and resulted in overhangs on the top Al gratings. Such structural modulation could therefore lower the transmission intensity (Figure S12, Supporting Information). The optical transmission proved sufficient in this work for polarimetric imaging and accurate Stokes parameter analysis, but can be improved in the future by optimizing the NIL mold fabrication process to improve the straightness of VCDG gratings and minimize the structure rounding at the grating foot. On the other hand, the maximum CPER of the NIL-fabricated MPFAs was ≈10 times and ≈4 times better at blue and red color wavelength ranges (≈20 and 80, respectively) than that of the EBL-fabricated device (≈2 and ≈20).[37] The improved CPER was attributed to the greatly enhanced LPER of the VCDGs over a broad visible wavelength range fabricated by NIL than that by EBL (Figure S13, Supporting Information), which was attributed to smoother VCDG grating lines and smaller optical losses. It was observed the peak wavelength of the max CPER was blue-shifted for the NIL-fabricated device, due to its thicker spacer layer (520 nm) than that of the EBL device (400 nm), consistent with simulation results (Figure S5, Supporting Information).

Further, we characterized the CPERs of the multilayered metasurfaces at different locations from two chips (Figure S14, Supporting Information). Different LCP and RCP filters from these two chips were shown to have similar CPER values at comparable wavelengths, demonstrating acceptable optical performance across different chips. We further performed FDTD simulations to better understand the impacts of key structural geometries on the CPER performance, including Si metasurface grating linewidth, Al VCDG duty cycle (i.e., the linewidth), and the spacer layer thickness. The simulation results showed that the maximal values and the wavelength dependence of CPERs are relatively insensitive to small variations in Si and Al gratings. In comparison, thickness variations of the spacer layer (i.e., NIL UV resist) would affect the optical coupling between the Si and Al metasurfaces, and therefore have a small but noticeable impact on the filter performance. Such variations are thought to result from nonuniform spin-coating and uneven NIL pressing, and could be minimized in future work by using more advanced manufacturing tools that provide better thickness control during film deposition and larger and more uniform pressure during NIL. In addition, it should be noted that the fabricated MPFA chips can be individually characterized to obtain their instrument matrix as detailed in the Experimental Section, and after the calibration, they can perform high-accuracy polarimetric imaging despite having slight performance variations.

3. Imaging Sensor Integration and Characterization

The integrated multi-layer MPFAs were diced (7.2 mm × 5.6 mm), optically aligned to the edges of a commercial CMOS sensor (IMX477) on a mask aligner and bonded with UV-curable polymer (**Figure** 4a,b, details in Experimental Section). This translational alignment error was on the micrometer scale and the rotational error was about 0.02, constrained by the lack of more accurate alignment marks (e.g., Moiré patterns) on the CMOS imaging sensors. To further minimize these alignment errors, the layouts of the CMOS imaging sensor and the metasurfaces may be co-designed with interferometric Moiré patterns, similar to what we demonstrated for high-accuracy alignment of multi-layer metasurface structures in the previous section. The bonded metasurface polarimetric imaging sensor (or Meta-PolarIm) was characterized to determine its instrument matrix A at different wavelength bands, i.e., blue (480–520 nm), green (530–570 nm), and red (580–620 nm), respectively (details to obtain the instrument matrix A in Experimental Section). Thus, the Stokes parameters of any unknown input polarization state S can be obtained using $S = A^{-1} \bullet I$, where I represents the intensity vector obtained by all eight pixels in each super-pixel of Meta-PolarIm. We measured the eight polarization states (Tables

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

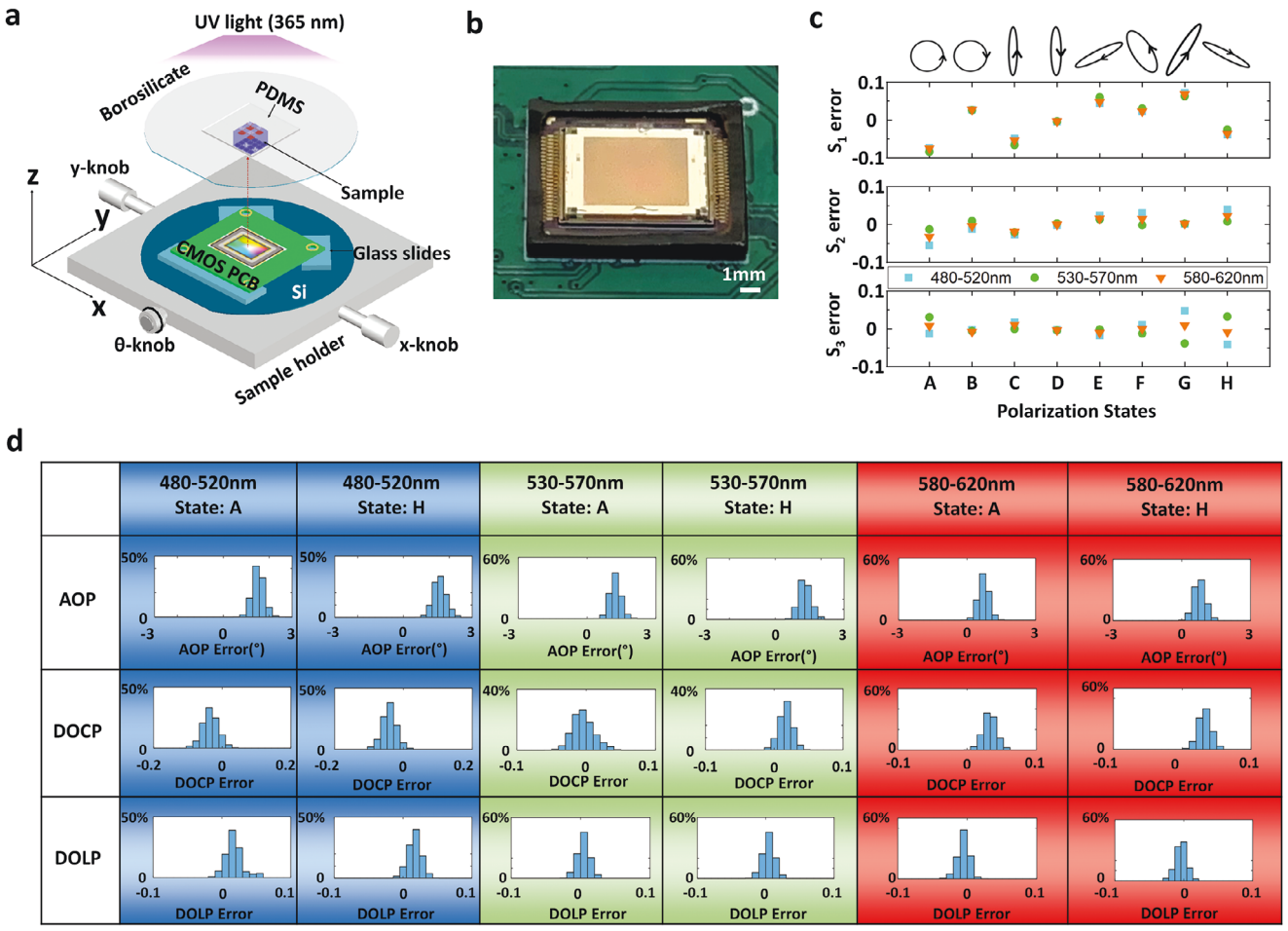


Figure 4. Multi-color full-Stokes polarization state detection using a metasurface polarimetric imaging sensor. a) Schematic of integrating MPFAs onto CMOS imaging sensor. A CMOS circuit board was first mounted onto a 3D rotation stage and leveled, and then the MPFA chip was aligned and bonded onto the board on a UV mask aligner. b) An optical image of the integrated Meta-PolarIm. c) Error analysis of multi-color, full-Stokes parameter detection of eight polarization states (A to H). d) Distributions of multi-color AOP, DOCP and DOLP detection errors of all metasurface pixels to analyze polarization states A and H. Here, the X-axes represent the errors and the Y-axes represent the corresponding percentage of pixels.

Table 4. Measurement errors of Stokes parameters and polarization states from eight polarized light inputs.

Color: Wavelengths [nm]	S_1	S_2	S_3	DOLP	DOCP	AOP
Blue: 480–520	4.13%	2.39%	1.93%	2.45%	1.93%	1.25
Green: 530–570	4.15%	1.4%	0.72%	2.37%	0.72%	1.20
Red: 580–620	4.45%	0.89%	1.59%	2.27%	1.59%	1.28

S4–S6, Supporting Information) with Meta-PolarIm (Figure 4c) to evaluate the polarization detection accuracy using a customized measurement setup (Figure S15, Supporting Information). The mean absolute errors (MAE) for Stokes parameters S_1, S_2, and S_3 were found to be <5% for all three wavelength bands (**Table 4**; Figures S16–S18 and Tables S5–S7, Supporting Information). We also performed statistical analysis for the errors of all pixels in the imaging sensor, including measurement errors for angle of polarization (AOP $=\frac{1}{2}\arctan\frac{S_2}{S_1}$), degree of circular polarization (DOCP $= S_3/S_0$) and degree of linear polarization (DOLP $=\sqrt{S_1^2+S_2^2}/S_0$) for the eight polarization states over the three wavelength bands (Figures S19–S21, Supporting Information). The results suggested that 90% of the polarimetric imaging pixels had reasonably small measurement errors for DOLP (<3%), AOP (<1.8) and DOCP (<2% for green and red, <6% for blue) (Figure 4d). Our results confirmed that this new NIL-based nanomanufacturing strategy was suitable for producing functional multi-layer metasurface devices with reasonably high performance and uniformity across a centimeter scale.

4. Polarization Imaging Application

The chip-integrated full-Stokes polarimetric imaging sensors have a broad range of applications. As proof-of-concept demonstrations, here we imaged several objects, including a plastic fork, a pair of 3D glasses, and a beetle (**Figure 5**, measurement setup illustrated in Figure S22, Supporting Information) to prove its functionality. The polarimetric images of the plastic fork (Figure 5a) and 3D glasses (Figure 5b) were obtained in

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

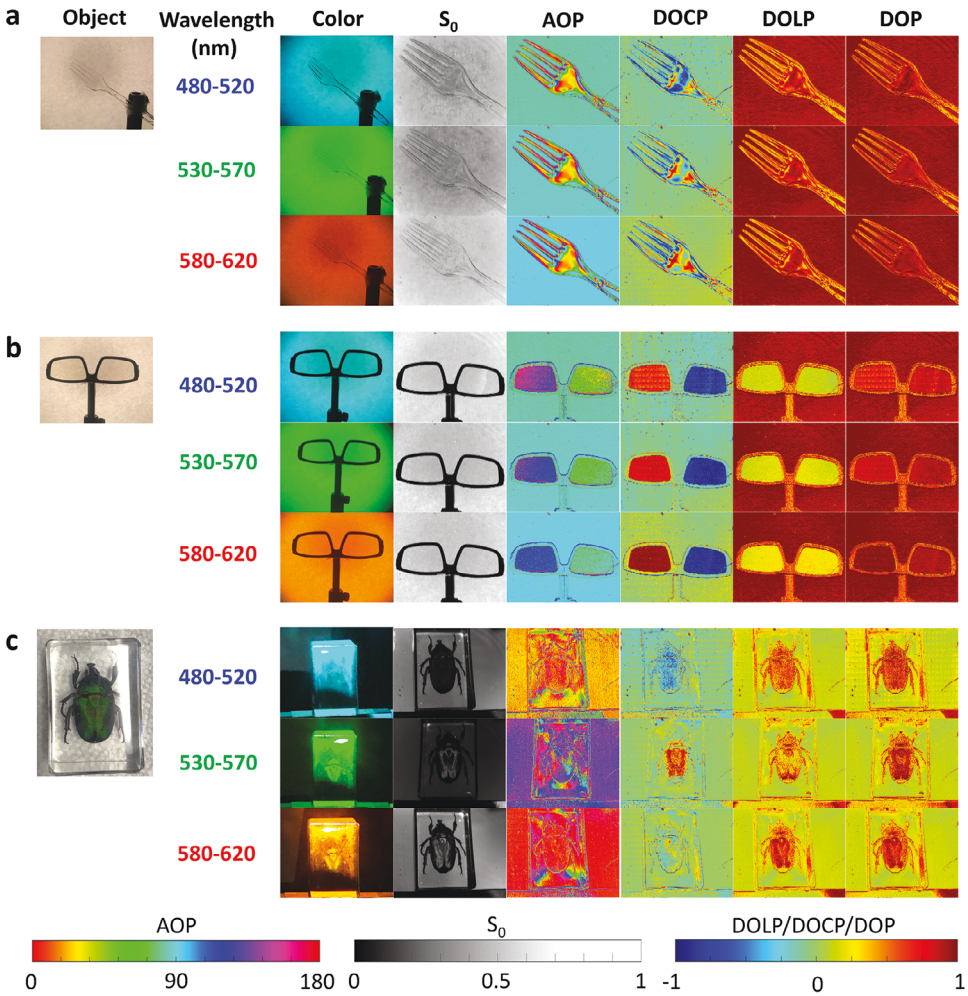


Figure 5. Multi-Color full-Stokes polarimetric images of exemplary objects. a,b) Transmission, color filtered, S_0, AOP, DOLP, DOCP, and DOP images of (a) a plastic fork, and (b) a pair of 3D glasses. The images were taken with the LP input as background. c) Reflection, color filtered, S_0, AOP, DOLP, DOCP, and DOP images of a Green June beetle. All the images were taken with an LP input light source and non-polarized white paper as background. Color channels were obtained by applying bandpass filters, i.e., 480 -520 nm for blue, 530–570 nm for green, and 580–620 nm for red.

transmission mode with ≈90° LP as the input light. These objects exhibited poor contrasts from the background in signal intensity (S_0) in all color bands; however, the AOP and DOCP images showed distinct contrasts. This was attributed to spatially varying optical birefringence (from local stress) in the plastic fork and the designed polarization response from the glasses. In addition, their DOCP images in the blue and red channels produced visually different polarization signals, indicating a wavelength-dependent polarization response. We also took images of a green June beetle sealed in resin in reflection mode (Figure 5c). The beetle elytra regions also presented a signature of wavelength dependence in DOCP images, showing right-handed CP signal (DOCP > 0) in the green channel, left-handed (DOCP<0) in the blue channel, but only low-contrast signals in the red channel. The above imaging results demonstrated the unique advantage of our metasurface-integrated Meta-Polarim to enhance imaging contrast by incorporating full-Stokes polarimetric signals in multi-wavelength channels, which is otherwise not available by conventional imaging sensors.

5. Conclusion

In summary, we propose and demonstrate a scalable manufacturing strategy for multilayer metasurfaces by synergistically co-designing multi-level NIL processes and metasurface structures. Uniquely, for the first time to our best knowledge, the nanometer-scale lithographic resolution and high-fidelity 3D pattern transfer capabilities of NIL were both explored to design and fabricate multilayer dielectric and metallic hybrid nanostructures in a single device. In particular, NIL was used as a lithography tool to create a first-layer Si metasurface, and then utilized as a transfer printing technique that preserved both the lateral and vertical geometries of the mold in the NIL resist as a 3D scaffold, which was converted into second-layer VCDG metasurface through a simple Al evaporation without defect-prone etching or liftoff steps. We demonstrated successful fabrication of dense nanostructures (period ≈200 nm and critical dimension <100 nm) in micro-sized arrays (4.65 × 4.65 μm^2 for VCDG and 7.75 × 7.75 μm^2 for Si metasurface) over ≈0.2 cm^2 area with uniform and accurate

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

dimension control (linewidth standard deviation <4 nm) and high interlayer alignment accuracy (translational error ≈200 nm, rotation error < 0.017 degrees). Compared to EBL, the NIL processes not only were much simpler and faster, but also greatly reduced the surface roughness (from ≈16 to ≈1 nm) and improved the CP extinction ratios to ≈20 and ≈80 at blue and red color wavelength ranges, or ≈10 and ≈4 times better. The NIL-fabricated MPFAs were bonded to a CMOS imager to create a metasurface polarimetric imaging sensor, i.e., Meta-PolarIm, for compact, single-shot, broadband polarimetric imaging in visible wavelengths, demonstrating a high polarization state measurement accuracy (<5%). These demonstrations proved this new, NIL-based, and simple fabrication method can outperform EBL in manufacturing throughput, cost, and device performance. This multilayer NIL-metasurface co-design approach can be adapted to the fabrication of many other metasurface structures, enabling on-chip integration of metasurface devices and their optic, electronic, optoelectronic, or quantum systems. By speeding up the prototyping process and enabling low-cost, large-scale production of such devices and systems, our design and manufacturing strategy can support future commercialization and broad deployment of metasurface devices in profound applications that are key to next-generation commercial electronics, national security, and sustainability.

6. Experimental Section

Materials: Poly(benzyl methacrylate) (≥ 99.0%), Propylene glycol monomethyl ether acetate (≥ 99.5%), Pentaerythritol tetra acrylate, Isobutyl methacrylate (≥ 97.0%), Anisole (≥ 99.7%), and trichloro (1*H*,1*H*,2*H*,2*H*-perfluorooctyl) silane, Octadecyl acrylate (≥ 97.0%), and 1*H*,1*H*,2*H*,2*H*-perfluoro-1-decanol (97%) were purchased from Sigma–Aldrich. BYK-310 and BYK-3570 were purchased from BYK Additives and Instruments. Omnirad 1173 and Omnirad TPO were purchased from IGM Resins. (Acryloxypropyl) methyl siloxane homopolymer was purchased from Gelest. Polymethyl methacrylate (PMMA, 950K A2 and 495K A3) was purchased from MicroChem. AMOPRIME was purchased from AMO GmbH. CN-292, SR-9003-B, and CN-975 were purchased from Satomer. AZ-1505 positive photoresist was purchased from MicroChemicals. Gel-box AD-22AS-00 was purchased from Gel-Pak. All chemicals were used as received without further purification.

Resist Preparation for NIL & CMOS Bonding Processes: The thermal NIL resist was prepared by diluting thermoplastic polymer (polybenzyl methacrylate, or PBMA) in Propylene glycol monomethyl ether acetate (PMA) as a solvent, with a small amount of surface additive (BYK-310) added to lower surface tension. The UV-NIL resist was prepared by mixing (Acryloxypropyl) methyl siloxane homopolymer with cross-linker (Pentaerythritol tetraacylated) photoinitiators (Omnirad 1173 and Omnirad TPO) and surface additive (BYK-3570) in Isobutyl methacrylate (IBMA). For the CMOS bonding process, another UV-curable polymer was prepared by mixing fast-reacting, low-viscosity, acrylate oligomers (e.g., SR-9003-B and CN-292), a surface additive (1*H*,1*H*,2*H*,2*H*-Perfluoro-1-decanol BYK-3570), and photoinitiators (Omnirad 1173 and Omnirad TPO) into IBMA solvent. All the solutions were stirred overnight at room temperature and filtered before use.

Mold Fabrication for Si Metasurface and VCDGs by EBL: The Si metasurface mold was fabricated by EBL (Figure S6, Supporting Information). A PMMA bi-layer was spin-coated (PS-80, Headway Research Inc.) on a cleaned Si substrate (1 mm thick, with 80 nm thermal SiO_2) and post-baked 5 min at 180° C. Then a 10 nm Cr layer was deposited on the PMMA as a discharging layer for EBL by thermal evaporator (Denton Bench Top Turbo, Denton Vacuum, LLC) at a deposition rate of 0.2 Å s^{-1}. Then EBL was carried out (ELS-7000, Elionix) with an acceleration voltage of 100 kV, a beam current of 1 nA, a field size of 300 µm with a minimum step size of 5 nm, and an exposure dose of 1200 µC cm^{-2}. After EBL, the Cr discharging layer was stripped and the patterns were developed in a 1:3 ratio (v/v) of methyl isobutyl ketone (MIBK)/isopropyl alcohol (IPA) solution for 2 min, rinsed in IPA, and dried with nitrogen. Then, a 10 nm Cr layer was deposited by using a thermal evaporator followed by an oxygen plasma descum (Tergeo plasma cleaner, 20 W, 10 sccm, 40 s) process. The sample was immersed in remover PG solution for 15 min at 80 °C for the lift-off process, rinsed with IPA and then DI water, and dried. The SiO_2 layer was etched by RIE (PlasmaTherm 790, CHF_3 = 40 sccm, O_2 = 3 sccm, 40 mTorr, 250 W) using Cr as a hard mask. Finally, the Cr hard mask was stripped by Cr etchant.

To fabricate NIL mold for the VCDGs, a thick fused silica wafer (6 mm) was chosen as the substrate (Figure S7, Supporting Information) to minimize mold bending during NIL. Then fused silica dicing, sample cleaning, EBL writing, development, Cr evaporation, and lift off were carried out following the same process mentioned above to produce the nanostructured Cr hard masks. The EBL exposure doses were adjusted for the designed structural dimensions. The Cr mask was used to etch 150 nm deep into fused silica by RIE using the same recipe as aforementioned. Differently, a mesa structure (roughly 1.5 cm^2, height = 2 µm) was intentionally fabricated in an additional RIE step to better accumulate pressure in the nanopatterned region. The mesa structure provided more uniformly imprinted structures using the imprinter. Both Si and fused silica molds were solvent and RCA-1 cleaned, and were treated using trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl) silane in a vacuum oven for 30 min at 100 °C to form self-assembled monolayers (SAMs) on the surface, which acted as an anti-sticking layer during the NIL process.[43]

Fabrication of Si Metasurface in a Tri-Layer Scheme: First, 130 nm α-Si was deposited on the pre-cleaned fused silica sample using plasma-enhanced CVD (PECVD) (Oxford Plasmalab 100, SiH_4 = 480 sccm, 1200 mTorr, 15 W, 350° C), followed by 60 nm SiO_2 deposition using the same tool (SiH_4 = 170 sccm, N_2O = 710 sccm, 1000 mTorr, 20 W, 350° C) without breaking chamber vacuum. After the substrate preparation, a tri-layer structure was employed for the thermal NIL process. Here thermal NIL was performed on a film stack made of a bottom polymethyl methacrylate (PMMA) layer, a mid-layer evaporated SiO_2 film, and a top-layer thermoplastic NIL resist. The polymers (PMMA and NIL resist) and SiO_2 layers in the film stack were selectively etched by a series of RIE with oxygen plasma or CHF_3 plasma, respectively, to transfer the NIL-patterned grating features. Lastly, Cr deposition, Cr mask liftoff, and RIE of SiO_2/Si films were performed to complete the fabrication of the Si metasurface layer. Specifically, a PMMA layer (950k A2, thickness of 90 nm) was spin-coated and post-baked for 5 min at 200 °C, followed by evaporation of ≈15 nm SiO_2 mid-layer (Kurt J. Lesker) at a deposition rate of 0.5 Å s^{-1}, and then spin-coating of thermal NIL resist and post-baking (5 min at 180 °C). The thermal NIL was carried out using a nanoimprinter (THU400, Zhenjiang Lehua Electronic Technology Co. Ltd.) at a nominal temperature reading of 55 °C and pressure of 750 KPa for 15 min in vacuum. Then the residual layer was RIE etched by oxygen plasma (O_2 = 10 sccm, 10 mTorr, 100 W), where the SiO_2 mid-layer acted as the etch-stop layer to enable sufficient over-etching time for uniform removal of the residual layer. The nanopatterns in the resist were transferred to SiO_2 mid-layer by another RIE etching (CHF_3 = 25 sccm, O_2 = 1 sccm, 10 mTorr, 100 W), and the PMMA bottom layer was RIE etched by oxygen plasma (O_2 = 10 sccm, 10 mTorr, 30 W). The high etching selectivity between SiO_2 and PMMA was beneficial for reliable patterning in a relatively thick PMMA layer, and helped form a mushroom-like structure in the SiO_2/PMMA stack to minimize the accumulation of metal on the sidewall of PMMA, which facilitated high-yield lift-off process and minimized feature distortion. The fabricated sample was immersed in remover PG solution for 15 min at 80 °C for lift-off, and later rinsed with IPA and DI water, followed by 10 nm Cr layer deposition by thermal evaporation. The 60 nm SiO_2 hard mask layer was etched by RIE (CHF_3 = 40 sccm, O_2 = 3 sccm, 40 mTorr, 250 W) using Cr as a hard mask, and Cr was stripped by chromium etchant. Finally,

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

the 130 nm α-Si film was etched using inductively coupled plasma (ICP) RIE (PlasmaTherm Apex ICP, Cl_2 = 100 sccm, Ar = 5 sccm, 10 mTorr, 250 W) using SiO_2 as a hard mask to complete Si metasurface fabrication. The SiO_2 hard mask layer was left without intentional removal, but its thickness was taken into account of the whole spacer layer thickness calculation.

Fabrication of VCDGs Using UV-NIL: The VCDGs were fabricated in a significantly simpler fabrication process. First, adhesion promoter (AMOPRIME) was spin-coated on pre-cleaned fused silica chips (some with Si metasurface structures for device integration, and some others without Si metasurface but used as process monitors) and post-baked 10 min at 115 °C on a hot plate. The prepared UV-NIL resist was spin-coated on the substrate, followed by UV-NIL using the fabricated fused silica VCDG mold on mask aligner (MJB4, Suss MicroTec). Three different fringes were visualized on the mask aligner TV monitor for the ease of alignment. Once the alignment was verified, 1.5 s UV exposure was used to cross-link the resist, which after curing turned to be a polymer similar to SiO_x in the optical index (UV-NIR spectroscopic ellipsometry, J.A. Woollam, M-2000) (Figure S8, Supporting Information). The UV resist had a low viscosity to easily fill during NIL, desired for high-fidelity pattern transfer at relatively low pressure.[44] After UV-NIL, the printed resist scaffold was treated using a mild oxygen plasma process (O_2 = 10 sccm, 10 mTorr, 30 W) to activate the hydroxyl groups on the surface. A layer of Cr (2 nm) was evaporated, and then Al was deposited at 2.5 Å s^{-1} to form the VCDG gratings. A high vacuum level (1 to 3×10^{-7} Torr) was useful to obtaining smoother surface morphology of VCDG (Figure S9, Supporting Information) by decreasing residual gases in the chamber and reducing contaminants. Finally, a 200 nm SiO_2 layer was deposited as an encapsulation layer to avoid further oxidation of the Al surface by using a radio-frequency (RF) sputtering system (Kurt J. Lesker) at a deposition rate of 0.5 Å s^{-1}.

Vertical Alignment and Integration of VCDGs on Si Metasurface: Here, two sets of gratings with slightly different periods (e.g., P_1 of 4 µm on the substrate and from Si metasurface mold, and P_2 of 4.2 µm on the VCDG mold) acted as the Moiré marks. The two gratings would produce periodic stripes under illumination, with the period P_{fringe} calculated as $P_{fringe} = P_1 \cdot P_2/(P_2 - P_1) = 84$ µm, when the substrate and mold were brought close to each other, e.g., with a small gap <10 µm. To minimize the alignment error, four groups of alignment markers (AM_1, AM_2, AM_3, and AM_4, respectively) were placed next to the NIL-patterned area, in other words separated by 7.2 mm horizontally and 5.6 mm vertically from each other. Noticeably, the process differs from previous studies that required metal deposition,[40,41] because the large optical index difference from α-Si metasurface (n = 3.58 at 632 nm) to the substrate SiO_2 (n = 1.49 at 632 nm) provided distinguishable contrast and eliminated the needs of metallic coating.

CMOS Bonding Process: The integrated multilayer metasurface chip was diced and bonded onto the customized CMOS sensor as follows. Here AZ-1505 photoresist (PR) was spin-coated on both sides of the fabricated sample and post-baked for 1 min at 90 °C as a protection layer during chip dicing, then the sample was diced into 7.2 mm × 5.6 mm rectangular shape using a dicing saw (DAD320, DISCO Corporation). Afterward, the sample was immersed in acetone to remove PR, rinsed in IPA, and dried with nitrogen blow. A thin PDMS film of ≈1 mm was detached from a commercially available Gel-box, and attached to a 4-inch borosilicate wafer as an intermediate host layer for the diced chip. A customized CMOS sensor on a printed circuit board (PCB) was mounted by Kapton tape onto a customized support, which was formed by taping stacked glass slides on a 4-inch Si wafer to avoid damaging the protruding electrical components on the backside of the PCB and to maintain the surface evenness during the bonding process. Then the UV-curable polymer was spin-coated on the CMOS imager, and the CMOS PCB was loaded into the mask aligner (MJB4, Suss MicroTec). After precise alignment the CMOS PCB was moved up in the z-direction and made contact with the metasurface chip, initiating polymer flow. Then the polymer was cross-linked under UV exposure (365 nm, 350 W) for 10 min to ensure appropriate bonding strength.

Structural and Material Characterization: The linewidth dimension and surface morphology of the α-Si metasurface and the Al VCDGs were inspected by scanning electron microscopy (SEM, Hitachi S-4700 FESEM) with an acceleration voltage of 15 keV and current of 10 µA. A thin layer of Au/Pd was sputtered (Cressington sputter coater 108) on the α-Si metasurface sample to enhance imaging resolution prior to SEM measurements. Optical properties (refractive index n, extinction coefficient k) of deposited α-Si and SiO_2 and cured UV resist films were measured by UV-NIR spectroscopic ellipsometry (J.A. Woollam, M-2000). Olympus BX53 fluorescent microscope coupled Horiba iHR320 imaging spectrometer was utilized to record all the optical images of fabricated samples for the calculation of alignment accuracy. It was noted that the electron microscopy would not be able to effectively detect the α-Si metasurface buried deep under the thick spacer layer (≈500 nm) after the UV NIL effectively planarized the surface topography. To standardize alignment error measurement, the optical images were converted to 8-bit black and white images and processed by setting a color threshold. The transmittance spectra were measured by the same tool, and then LPER and CPER were calculated.

Metasurface Design and Simulation: The finite-difference time-domain (FDTD) simulations were carried out to calculate transmission efficiency, as well as LPER and CPER of the metal-dielectric hybrid chiral metasurface. All the simulations were conducted with empirically measured optical indexes of each material. The mesh sizes were set as 5 nm. Periodic boundary conditions and perfectly matched layers were used within a unit cell along the in-plane direction. To calculate LPER of two orthogonal polarizations, a plane wave was applied as the source with its electric field pointing along the grating width and length directions, respectively. To represent RCP/LCP light input, two orthogonally linearly polarized plane waves with the same amplitude but 90° phase difference were used as the source. In initial simulations, ideal VCDG gratings without edge rounding were considered (Figures S1–S5, Supporting Information). Later, the non-ideal structural rounding effect and non-straight α-Si grating sidewalls (assumed six degrees off normal surface) were considered in the simulations, based on experimental characterizations.

Reference Polarization State Value Calculation: Stokes parameters of 8 reference polarization states input were theoretically calculated based on the linear retardance, transmission efficiency, and bandwidth of the optical elements, including color filters, linear polarizer, and super achromatic quarter-wave plate. First, transmission efficiency and linear retardance dispersion data of SAQWP05M-700 (Thorlabs) were obtained from Thorlabs website. Stokes parameter of light transmitted through the linear polarizer (with angle of θ_1) and quarter waveplate (with fast axis along angle θ_2) were modeled using the Mueller matrix of a linear attenuator and a linear retarder:

$$M_{LP} = \frac{1}{2} \times \begin{bmatrix} q+r & (q-r)\,cos2\theta_1 & (q-r)\,sin2\theta_1 & 0 \\ (q-r)\,cos2\theta_1 & (q+r)\,cos^2 2\theta_1 + \sqrt{qr}sin^2 2\theta_1 & \left(q+r-2\sqrt{qr}\right) sin2\theta_1 cos2\theta_1 & 0 \\ (q-r)\,sin2\theta_1 & \left(q+r-2\sqrt{qr}\right) sin2\theta_1 cos2\theta_1 & (q+r)\,sin^2 2\theta_1 + \sqrt{qr}cos^2 2\theta_1 & 0 \\ 0 & 0 & 0 & 2\sqrt{qr} \end{bmatrix} \quad (1)$$

here, θ_1 represented the transmission axis of the linear polarizer, q and r represented the maximum and minimum transmission efficiency of the linear polarizer and were extracted from data provided by the Thorlabs

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

website. LPER was expressed as LPER = q/r.

$$M_{retarder} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & cos^2 2\theta_2 + sin^2 2\theta_2 cos\,\delta & sin2\theta_2 cos2\theta_2\,(1-cos\,\delta) & -sin2\theta_2 sin\,\delta \\ 0 & sin2\theta_2 cos2\theta_2\,(1-cos\,\delta) & sin^2 2\theta_2 + cos^2 2\theta_2 cos\,\delta & cos2\theta_2 sin\,\delta \\ 0 & sin2\theta_2 sin\,\delta & -cos2\theta_2 sin\,\delta & cos\,\delta \end{bmatrix} \quad (2)$$

here, θ_2 represented the angle fast axis of the retarder, and δ represented retardance, as extracted from data provided by the Thorlabs website.

$$S_{in}^{\lambda} = M_{retarder} \cdot M_{LP} \cdot \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3)$$

It is noteworthy that both δ and fast axis angle θ_2 are wavelength-dependent. Final Stokes parameters were averaged after S_{in} was obtained at each wavelength accounting for wavelength dependency of δ and θ_2 using the equation:

$$S_{in} = \frac{\sum_{i=1}^{n} S_{in,i}^{\lambda}}{n} \quad (4)$$

Device Instrument Matrix Calibration Process at Red, Green, and Blue Colors: For an arbitrary input polarization state S_λ at a given input wavelength λ(nm), the captured intensity of a super-pixel as a vector I was written as the equation below:

$$I = \begin{bmatrix} s_0^{0G\_out} \\ s_0^{90G\_out} \\ s_0^{135G\_out} \\ s_0^{45G\_out} \\ s_0^{LCP\_RB} \\ s_0^{RCP\_RB} \\ s_0^{LCP\_G} \\ s_0^{RCP\_G} \end{bmatrix} = \begin{bmatrix} m_{11}^{0G} & m_{12}^{0G} & m_{13}^{0G} & m_{14}^{0G} \\ m_{11}^{90G} & m_{12}^{90G} & m_{13}^{90G} & m_{14}^{90G} \\ m_{11}^{135G} & m_{12}^{135G} & m_{13}^{135G} & m_{14}^{135G} \\ m_{11}^{45G} & m_{12}^{45G} & m_{13}^{45G} & m_{14}^{45G} \\ m_{11}^{LCP\_RB} & m_{12}^{LCP\_RB} & m_{13}^{LCP\_RB} & m_{14}^{LCP\_RB} \\ m_{11}^{RCP\_RB} & m_{12}^{RCP\_RB} & m_{13}^{RCP\_RB} & m_{14}^{RCP\_RB} \\ m_{11}^{LCP\_G} & m_{12}^{LCP\_G} & m_{13}^{LCP\_G} & m_{14}^{LCP\_G} \\ m_{11}^{RCP\_G} & m_{12}^{RCP\_G} & m_{13}^{RCP\_G} & m_{14}^{RCP\_G} \end{bmatrix} \times \begin{bmatrix} S_0 \\ S_1 \\ S_2 \\ S_3 \end{bmatrix}$$

$$= A_\lambda \times S_\lambda \quad (5)$$

where matrix A_λ was the wavelength-dependent instrument matrix[45] of the metasurface filter array. S_λ was inversely calculated by solving Equation 5:

$$S_\lambda = {A_\lambda}^{-1} \times I \quad (6)$$

To obtain A_λ at red, green, and blue color ranges, three color filters (FBH450-40, FBH550-40, FBH600-40) were used with a bandwidth of 40 nm to select targeted wavelength range. For each color, ten pre-known polarization states $S_{\lambda,4\times10}$ were measured by the device to form an intensity matrix $I_{cam,6\times10}$, and the instrument matrix A_λ was obtained using the following equation:

$$A_\lambda = I_{cam,6\times10} \times {S_{\lambda,4\times10}^{T}}^{-1} \quad (7)$$

here, the rank of $S_{\lambda,4\times10}^{T}$ should be 4 to make sure $S_{\lambda,4\times10}^{T}$ is invertible.

Statistical Analysis of Structural Linewidths: As shown in Figure 2, the linewidths of Si and Al metasurface gratings of all filter array designs were inspected at five different, randomly selected locations within the nanopatterned MPFA area (5.2 by 4 mm) across the sample (7.2 mm × 5.6 mm after dicing), i.e., at the center of the chip ①, center right ②, center left ③, center top ④ and center bottom ⑤. The distances were ≈4 mm between locations ② and ③ and 3 mm between ④ and ⑤. At each location, SEM images were taken at ≈50000 magnifications, and the widths of 10 to 15 lines for each filter array design were measured by ImageJ. The linewidths were averaged in Excel to obtain the mean value linewidth μ of each filter array design at each of the five positions, and then the mean and standard deviations of the measured linewidths across the wafer were calculated as $\mu = \frac{1}{5}\sum_{i=1}^{5} w_i$ and $SDs = \sqrt{\frac{1}{5}\sum_{i=1}^{5}(w_i - \mu)^2}$. The analyzed linewidths values were given as mean in each location but as mean ± SD for each filter array design across the sample in Table 2.

Stokes Parameter Analysis: A moving window spatial scanning discussed (Figure 1b) was first applied during the calibration process to increase the imaging resolution of the polarimetric imaging sensor to 671 by 509 super-pixels, each containing eight polarization filters for full Stokes parameter analysis. First, the measurement results S_i^j were obtained at normal incidence under multi-color inputs and averaged from all pixels: $S_i^j = \frac{1}{o\times p}\sum^{o,p} S_i^j/S_0^j$. Here i = 1, 2, 3 indicated the Stokes parameters, j = 1,2... 8 referred to the eight polarization states used for analysis, o = 671, p = 509, S_0^j was the input light intensity measured by each super-pixel, and S_i^j/S_0^j denoted the normalized Stokes parameters measured by each super-pixel. The measurement errors ΔS_i^j were then calculated by subtracting the measurement data S_i^j from the theoretically obtained reference values $S_{R_i}^{\ j}$, following $\Delta S_i^j = S_i^j - S_{R_i}^{\ j}$ (i = 1, 2, 3, j = 1,2... 8).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

S.C. and J. Z. contributed equally to this work. This project was supported by the U. S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) under the Solar Energy Technologies Office (SETO) Award number DE-EE0008999. S.C. and C.W. acknowledge partial support by the National Science Foundation under grant no. 1847324 and 1947753. Y. Y and J. Z acknowledge the support in part by the State of Arizona through the Science and Technology Centers of the Impact Arizona (formerly known as New Economy Initiative). The authors acknowledge Roland Himmelhuber and the Micro/Nano fabrication center at University of Arizona for training on their EBL tool in fabrication process. Some of the device fabrication and characterization steps were carried out in the NanoFab and Eyring Materials Center (EMC) at Arizona State University. Access to the NanoFab and/or EMC was supported, in part, by NSF grant no. ECCS-1542160.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

moiré alignment, multilayer metasurfaces, nanoimprint lithography, polarimetric imaging, scalable nanomanufacturing

© 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Received: March 20, 2024
Revised: May 28, 2024
Published online:

[1] A. C. Overvig, S. Shrestha, S. C. Malek, M. Lu, A. Stein, C. Zheng, N. Yu, *Light: Sci. Appl.* **2019**, *8*, 92.
[2] M. Liu, W. Zhu, P. Huo, L. Feng, M. Song, C. Zhang, L. Chen, H. J. Lezec, Y. Lu, A. Agrawal, T. Xu, *Light: Sci. Appl.* **2021**, *10*, 107.
[3] M. Mehmood, S. Mei, S. Hussain, K. Huang, S. Siew, L. Zhang, T. Zhang, X. Ling, H. Liu, J. Teng, *Adv. Mater.* **2016**, *28*, 2533.
[4] S. Yuan, X. Qiu, C. Cui, L. Zhu, Y. Wang, Y. Li, J. Song, Q. Huang, J. Xia, *ACS Nano* **2017**, *11*, 10704.
[5] N. A. Rubin, G. D'Aversa, P. Chevalier, Z. Shi, W. T. Chen, F. Capasso, *Science* **2019**, *365*, eaax1839.
[6] H. Ren, X. Fang, J. Jang, J. Bürger, J. Rho, S. A. Maier, *Nat. Nanotechnol.* **2020**, *15*, 948.
[7] Z. Yang, Z. Wang, Y. Wang, X. Feng, M. Zhao, Z. Wan, L. Zhu, J. Liu, Y. Huang, J. Xia, *Nat. Commun.* **2018**, *9*, 4607.
[8] F. Qin, L. Ding, L. Zhang, F. Monticone, C. C. Chum, J. Deng, S. Mei, Y. Li, J. Teng, M. Hong, *Sci. Adv.* **2016**, *2*, 1501168.
[9] B. Zeng, Z. Huang, A. Singh, Y. Yao, A. K. Azad, A. D. Mohite, A. J. Taylor, D. R. Smith, H.-T. Chen, *Light: Sci. Appl.* **2018**, *7*, 51.
[10] H.-T. Chen, A. J. Taylor, N. Yu, *Rep. Prog. Phys.* **2016**, *79*, 076401.
[11] V.-C. Su, C. H. Chu, G. Sun, D. P. Tsai, *Opt. Express* **2018**, *26*, 13148.
[12] G. Yoon, I. Kim, J. Rho, *Microelectron. Eng.* **2016**, *163*, 7.
[13] J.-S. Park, S. Zhang, A. She, W. T. Chen, P. Lin, K. M. Yousef, J.-X. Cheng, F. Capasso, *Nano Lett.* **2019**, *19*, 8673.
[14] S. Y. Chou, presented at IEEE/LEOS International Conference on Optical MEMS and Their Applications Conference, IEEE, Piscataway, NJ **2006**.
[15] S. Y. Chou, P. R. Krauss, P. Renstrom, *J Vac Sci Technol B Microelectron Nanometer Struct Process Meas Phenom* **1996**, *14*, 4129.
[16] J. Kim, J. Seong, W. Kim, G.-Y. Lee, S. Kim, H. Kim, S.-W. Moon, D. K. Oh, Y. Yang, J. Park, *Nat. Mater.* **2023**, *22*, 474.
[17] I. Kim, W.-S. Kim, K. Kim, M. A. Ansari, M. Q. Mehmood, T. Badloe, Y. Kim, J. Gwak, H. Lee, Y.-K. Kim, J. Rho, *Sci. Adv.* **2021**, *7*, eabe9943.
[18] Z. Yu, P. Deshpande, W. Wu, J. Wang, S. Y. Chou, *Appl. Phys. Lett.* **2000**, *77*, 927.
[19] S.-W. Ahn, K.-D. Lee, J.-S. Kim, S. H. Kim, J.-D. Park, S.-H. Lee, P.-W. Yoon, *Nanotechnology* **2005**, *16*, 1874.
[20] Z. Yu, H. Gao, W. Wu, H. Ge, S. Y. Chou, *J Vac Sci Technol B Microelectron Nanometer Struct Process Meas Phenom* **2003**, *21*, 2874.
[21] M. G. Kang, M. S. Kim, J. Kim, L. J. Guo, *Adv. Mater.* **2008**, *20*, 4408.
[22] W.-D. Li, S. Y. Chou, *Opt. Express* **2010**, *18*, 931.
[23] C. Wang, Q. Zhang, Y. Song, S. Y. Chou, *ACS Nano* **2014**, *8*, 2618.
[24] H. Liu, H. Yang, Y. Li, B. Song, Y. Wang, Z. Liu, L. Peng, H. Lim, J. Yoon, W. Wu, *Adv. Opt. Mater.* **2019**, *7*, 1801639.
[25] M. F. S. Shahidan, J. Song, T. D. James, A. Roberts, *Nanoscale Adv.* **2020**, *2*, 2177.
[26] T. D. James, P. Mulvaney, A. Roberts, *Nano Lett.* **2016**, *16*, 3817.
[27] S.-W. Lee, K.-S. Lee, J. Ahn, J.-J. Lee, M.-G. Kim, Y.-B. Shin, *ACS Nano* **2011**, *5*, 897.
[28] A. Cattoni, P. Ghenuche, A.-M. Haghiri-Gosnet, D. Decanini, J. Chen, J.-L. Pelouard, S. Collin, *Nano Lett.* **2011**, *11*, 3557.
[29] G. Yoon, K. Kim, D. Huh, H. Lee, J. Rho, *Nat. Commun.* **2020**, *11*, 2268.
[30] W.-J. Joo, J. Kyoung, M. Esfandyarpour, S.-H. Lee, H. Koo, S. Song, Y.-N. Kwon, S. H. Song, J. C. Bae, A. Jo, *Science* **2020**, *370*, 459.
[31] V. J. Einck, M. Torfeh, A. McClung, D. E. Jung, M. Mansouree, A. Arbabi, J. J. Watkins, *ACS Photonics* **2021**, *8*, 2400.
[32] S. V. Makarov, V. Milichko, E. V. Ushakova, M. Omelyanovich, A. Cerdan Pasaran, R. Haroldson, B. Balachandran, H. Wang, W. Hu, Y. S. Kivshar, *ACS Photonics* **2017**, *4*, 728.
[33] Y. Yao, H. Liu, Y. Wang, Y. Li, B. Song, R. P. Wang, M. L. Povinelli, W. Wu, *Opt. Express* **2016**, *24*, 15362.
[34] M. K. Chen, J. C. Zhang, C. W. Leung, L. Sun, Y. Fan, Y. Liang, J. Yao, X. Liu, J. Yuan, Y. Xu, *Nanophotonics* **2023**, *12*, 2479.
[35] X. Lai, Q. Ren, F. Vogelbacher, W. E. Sha, X. Hou, X. Yao, Y. Song, M. Li, *Adv. Mater.* **2022**, *34*, 2107243.
[36] V. Nagal, T. Li, J. B. Khurgin, D. H. Gracias, *ACS Appl. Nano Mater.* **2020**, *3*, 7029.
[37] J. Zuo, J. Bai, S. Choi, A. Basiri, X. Chen, C. Wang, Y. Yao, *Light: Sci. Appl.* **2023**, *12*, 218.
[38] A. Lebib, Y. Chen, F. Carcenac, E. Cambril, L. Manin, L. Couraud, H. Launois, *Microelectron. Eng.* **2000**, *53*, 175.
[39] C. Wang, K. J. Morton, Z. Fu, W.-D. Li, S. Y. Chou, *Nanotechnology* **2011**, *22*, 445301.
[40] M. Mühlberger, I. Bergmair, W. Schwinger, M. Gmainer, R. Schöftner, T. Glinsner, C. Hasenfuß, K. Hingerl, M. Vogler, H. Schmidt, E. B. Kley, *Microelectron. Eng.* **2007**, *84*, 925.
[41] N. Li, W. Wu, S. Y. Chou, *Nano Lett.* **2006**, *6*, 2626.
[42] L. J. Guo, *Adv. Mater.* **2007**, *19*, 495.
[43] G.-Y. Jung, Z. Li, W. Wu, Y. Chen, D. L. Olynick, S.-Y. Wang, W. M. Tong, R. S. Williams, *Langmuir* **2005**, *21*, 1158.
[44] M. D. Austin, H. Ge, W. Wu, M. Li, Z. Yu, D. Wasserman, S. Lyon, S. Y. Chou, *Appl. Phys. Lett.* **2004**, *84*, 5299.
[45] R. Azzam, *JOSA A* **1990**, *7*, 87.

 © 2024 Wiley-VCH GmbH

16163028, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/adfm.202404852 by Chao Wang - Arizona State University Acq , Wiley Online Library on [17/06/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License