

A Merged Backside Series/Parallel Hybrid Piezoelectric-Resonator-Based DC-DC Converter

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Abstract—This study introduces a merged backside series/parallel hybrid piezoelectric resonator-based (BSPPR) DC-DC converter that improves the performance of conventional piezoelectric-resonator-based (baseline PR) converters at large step-down ratios. The proposed converter incorporates a 2:1 series-parallel switched capacitor (SC) network to the output of the baseline PR converter, enabling a more efficient step-down conversion while placing the piezoelectric resonator (PR) on the high voltage side, which leads to reduced PR resonant current and PR vibration losses (I^2R losses). Moreover, due to the merged hybrid converter concept, the operational principle remains unchanged, preserving all the benefits of the baseline PR converter, including zero-voltage-switching (ZVS) and soft charging. A prototype of the BSPPR converter, employing disk-shaped lead zirconate titanate (PZT) PRs, is constructed and achieves a peak efficiency of 95.8%.

Index Terms—piezoelectric resonator, hybrid converter, switched capacitor

I. INTRODUCTION

Piezoelectric resonators (PRs) have gained significant attention as a magnetics replacement in DC-DC converters due to the promising high efficiency and power density of prior work [1]–[5]. Amongst various PR-based DC-DC converters, the step-down PR (baseline PR) converter, depicted in Fig. 1(a), garnered the most interest for its excellent peak efficiency where the PR component is represented by a Butterworth-Van Dyke (BVD) model with mechanical vibration equivalents (R , L , and C) and the junction capacitor (C_P) [6]. By operating PRs in the inductive resonant region, the baseline PR converter realizes zero-voltage switching (ZVS) and soft-charging of the PR's junction capacitor, minimizing the overall losses. Unfortunately, the baseline PR exhibits peak efficiency at a 0.5 voltage conversion ratio (VCR), defined as (V_o/V_{in}), with efficiency declining exponentially as the VCR decreases. The efficiency degradation arises from the increased circulating charge at a low VCR. This characteristic restricts the usage of PR-based converters in modern electronic applications with conversion ratios at or below 0.2.

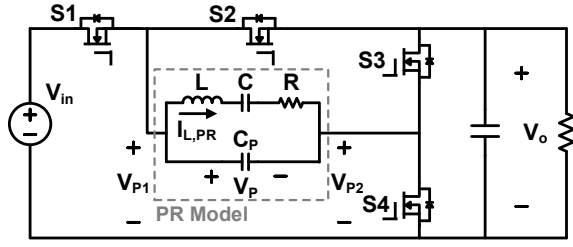
To address the efficiency issue, various hybrid PR-based converters have been reported [7], [8] in a similar manner to hybrid inductive buck converters. Both the Frontside Series/Parallel PR-based converter (FSPPR), Fig. 1(b), and Merged Switched Capacitor PR-based converter (MSCPR),

Fig. 1(c), leverage the advantages of switched capacitors to reduce the equivalent input voltage of PRs, thereby minimizing the PR resonant current and improving efficiency at low VCRs. However, such converters position the PR on the output side (low-voltage/high-current side), requiring the PR to process a large output current. As a result, significant PR vibration losses (I^2R losses) arise, constraining the achievable efficiency and output capability, which is limited by the maximum allowable current of PRs.

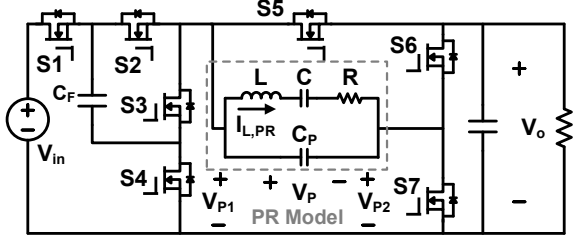
In response, this paper proposes a merged Backside Series/Parallel PR-based (BSPPR) converter. Unlike prior art, the proposed approach employs a switched capacitor network located on the backside (i.e., output side) of the converter, which thus places the PR on the high-voltage/low-current side. This configuration effectively reduces the PR resonant current as well as PR vibration losses, and shifts the optimal operating point to a lower VCR (from 0.5 to 0.25) while preserving all benefits of the baseline PR converter, such as ZVS for all switches. Furthermore, owing to the hybrid converter concept, similar to a hybrid Buck converter, the operation principle remains unchanged from the baseline PR converter, allowing for the direct application of the control logistics reported in [9], [10]. In contrast, both FSPPR and MSCPR converters only achieve ZVS on specific switches, and the MSCPR converter alters the operation principle from the baseline PR with a more complex driving strategy. A physical prototype of the proposed BSPPR is constructed, and measurement results are contrasted with baseline and FSPPR converters.

II. PROPOSED BACKSIDE SERIES/PARALLEL PIEZOELECTRIC-RESONATOR-BASED CONVERTER

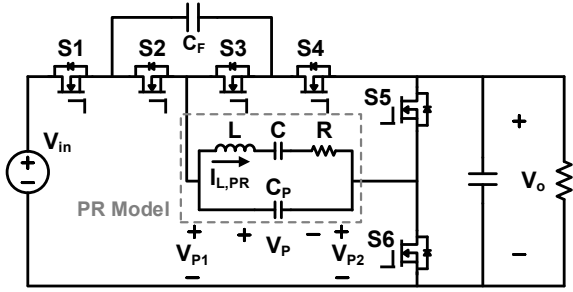
The Backside Series/Parallel PR-based (BSPPR) converter is shown in Fig. 2. Following the PR-based stage, a SC network is merged into the baseline PR converter, incorporating the output half-bridge structure of the baseline PR converter, switches S3-6, and additional switches S7,8 along with a flying capacitor, C_F . This configuration forms a 2:1 series/parallel SC network to the output, where C_F is controlled by driving signals D3 and D4 that position it either in series or parallel with the output. Notably, due to its series/parallel arrangement with the output, C_F is inherently self-balanced to the output voltage, V_o , effectively reducing the control complexity.



(a) Baseline PR-based converter



(b) Frontside Series/Parallel PR-based converter (FSPPR)



(c) Merged Switched Capacitor PR-based converter (MSCPR)

Fig. 1. Different PR-based Converter

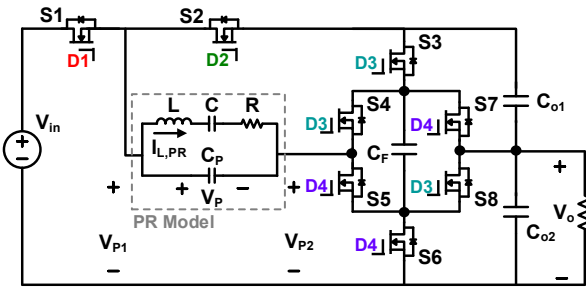


Fig. 2. Backside Series/Parallel PR-based (BSPPR) converter

Furthermore, this configuration allows the PR to operate at the high voltage/low current side for a given output power level, thereby reducing the PR resonant current and I^2R losses within the PR. Lastly, as C_F is balanced to V_o , ZVS turn-on for S7 and S8 is enabled, further reducing the overall losses.

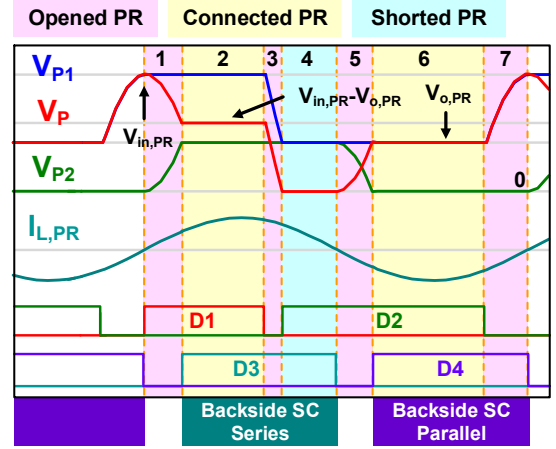


Fig. 3. Operation waveforms of Backside Series/Parallel PR-based (BSPPR) converter

A. Operation Principle

The operation waveforms and phases are illustrated in Fig. 3 and 4 where $V_{in,PR}$ and $V_{o,PR}$ represent the equivalent input/output voltage for PR stage. Here, $V_{in,PR}$ is the input voltage, V_{in} while $V_{o,PR}$ is twice the output voltage, $2V_o$ in the BSPPR converter. There are 7 individual phases in an operation cycle, where the PR can be arranged in one of three states: (1) opened PR, (2) connected PR, and (3) shorted PR states.

At the beginning, no current loop is formed by the switches in phase 1, leading to an open PR state. In this phase, the inductive PR current, $I_{L,PR}$, discharges C_P , where V_{P2} is correspondingly increased. As V_{P2} equals $V_{o,PR}$, the body diodes of S3 and S4 become forward-biased. This allows ZVS turn-on of S3, S4, and S8, entering phase 2 and making C_F in series with the load. During phase 2, the PR is linked to both the input and output, transferring energy to the output while storing energy within the PR. The phase ends as S1 deactivates, transitioning to phase 3, an open PR state, where $I_{L,PR}$ discharges C_P until $V_{P1} = V_{o,PR}$, assuring ZVS turn-on for S2. Then, phase 4 initiates, creating a shorted loop to ensure the current continuity and this free-wheeling phase terminates when the polarity of $I_{L,PR}$ reverses, after which switches S3, S4, and S8 are opened. This puts the PR back to an open PR state, phase 5, where $I_{L,PR}$ charges C_P , discharging V_{P2} until it becomes zero where body diodes of S5 and S6 are conducted with ZVS turn-on enabled for S5-S7. This consequently puts the C_F in parallel with the load, and the PR is connected to the output and ground, entering the connected PR state, where the PR starts to release energy to the load. Phase 7 begins as S2 turns off, opening the PR. In this phase, $I_{L,PR}$ charges C_P until V_{P1} reaches $V_{in,PR}$, ensuring ZVS turn-on for S1.

B. Voltage Conversion Ratio

As illustrated in Fig. 3, the PR must follow the conversion of charge (Coc) and conversion of energy (CoE) principles in the steady state to keep charge and energy balanced [3].

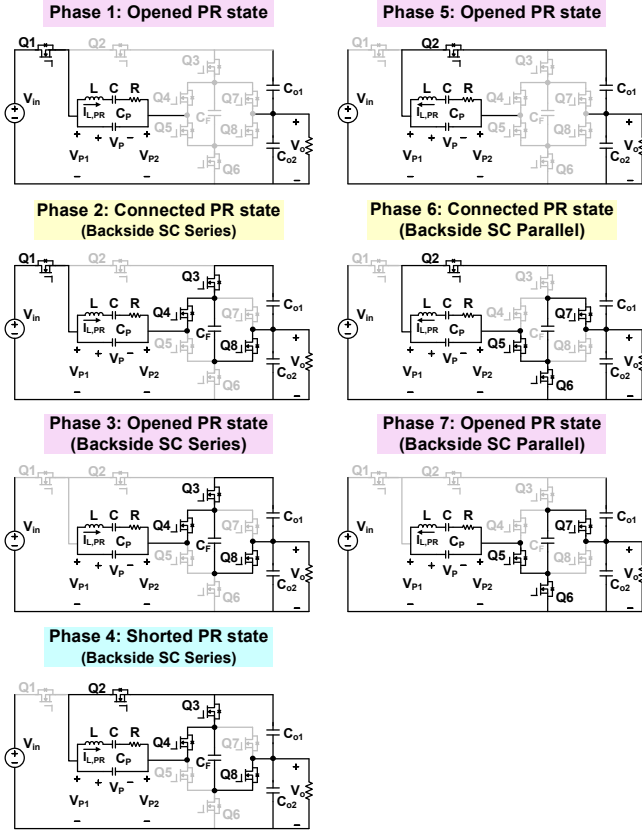


Fig. 4. Operation phases of Backside Series/Parallel PR-based (BSPPR) converter

Hence, the CoC of PR mechanical capacitor, C , and junction capacitor, C_P and be expressed as (1) and (2) where q_n is the charge in phase n .

$$q_1 + q_2 + q_3 + q_4 + q_5 + q_6 + q_7 = 0. \quad (1)$$

$$q_1 + q_3 + q_5 + q_7 = 0. \quad (2)$$

On the other hand, the CoE of the PR can be written as:

$$\begin{aligned} E_2 + E_4 + E_6 &= V_2 q_2 + V_4 q_4 + V_6 q_6 \\ &= (V_{in,PR} - V_{o,PR}) q_2 + (0) q_4 + (V_{o,PR}) q_6 = 0. \end{aligned} \quad (3)$$

Here, $V_{in,PR}$ and $V_{o,PR}$ are the equivalent input/output voltage viewed by the PR. In the BSPPR converter, $V_{in,PR}$ equals V_{in} and $V_{o,PR}$ equals $2V_o$.

By substituting (1) and (2) into (3), the voltage conversion ratio can be found as:

$$0 \leq \frac{V_o}{V_{in}} = \frac{1}{2} \frac{q_2}{2q_2 + q_4} \leq \frac{1}{4}. \quad (4)$$

According to (4), it can be found that the VCR is regulated by the ratio of phases 2 (connected state) and 4 (shorted state), which can also be translated into the ratio of the input-connected time (phase 2) and the circulating time (phase 4). Therefore, an extended phase 2 interval implies a prolonged input-connected time leading to an increased VCR, and conversely, a shortened phase 2 interval leads to a reduced VCR.

C. PR Utilization Factor

The PR utilization factor is defined by the charge transfer utilization as a ratio of the charges delivered to the output, Q_{out} , to the total connected/shorted state charges including charges delivered to the output, Q_{out} , and the charges circulating inside the circuit in the shorted state, Q_{cir} [3]. Thus, the PR utilization factor can be written as:

$$K = \frac{Q_{out}}{Q_{out} + Q_{cir}} = \frac{|q_2| + |q_6|}{|q_2| + |q_4| + |q_6|}. \quad (5)$$

By inserting (1), (2) and (3) into (5), K is expressed as:

$$0.5 \leq K = \frac{V_{in}}{2(V_{in} - 2V_o)} \leq 1. \quad (6)$$

Based on (4) and (6), it can be observed that the BSPPR converter reaches its maximum K of 1 at 0.25 VCR; on the other hand, the baseline PR converter presents a K of 0.67 at the same conversion ratio indicating a higher portion of circulating interval in the baseline PR converter, and consequently, a lower efficiency.

D. PR Resonant Current Amplitude

The amplitude of PR resonant current, $I_{L,PR(PK)}$, can be found by the charges in connected and shorted states, and charges used to achieve ZVS as defined in [3], which can be derived as:

$$I_{L,PR(pk)} = \pi \left(\frac{P_o}{4KV_o} + f_{sw} C_P V_{in} \right). \quad (7)$$

The resonant current, $I_{L,PR(PK)}$, is directly correlated to the output current. However, in (7), the output-related term is written as $P_o/(4KV_o)$, contrasting with the baseline PR, FSPPR, and MSCPR converters as $P_o/(2KV_o)$. This implies that the PR resonant current in the BSPPR converter can be smaller than in others at the same output condition, leading to reduced $I^2 R$ losses in the PR. The difference in resonant current arises because the PR is relocated to the input side (high voltage/low current side) rather than being directly linked to the output (low voltage/high current side).

III. TOPOLOGY COMPARISONS

To better understand the performance of the proposed topology, three other PR-based converters: Baseline PR, FSPPR, and MSCPR, as shown in Fig. 1, are selected for performance comparison. Various aspects are discussed in this section including VCR, K , $I_{L,PR(PK)}$, and PR efficiency.

A. Voltage Conversion Ratio and PR Utilization Factor

The voltage conversion range for each PR-based converter is illustrated in Table I. Here it can be seen that the hybrid PR-based converters exhibit slightly smaller voltage conversion ranges compared to the baseline PR converter, attributed to the presence of the hybrid SC mechanism.

Table II and Fig. 5 show K and its dynamic relationship with VCR across various PR-based converters. As shown, the MSCPR, even with the introduction of hybrid conversion,

TABLE I
VOLTAGE CONVERSION RANGE OF DIFFERENT PR-BASED CONVERTERS

Topology	VCR		
Baseline PR	0		1/2
FSPPR	0	$\leq \frac{V_o}{V_{in}} \leq$	1/4
BSPPR	0		1/4
MSCPR	0		1/3

TABLE II
PR UTILIZATION FACTOR, EQUIVALENT PR INPUT/OUTPUT VOLTAGE, AND PEAK-TO-PEAK PR VOLTAGE

Topology	K	$V_{in,PR}$	$V_{o,PR}$	$V_{p(p-p)}$
Baseline PR	$\frac{V_{in}}{2(V_{in}-V_o)}$	V_{in}	V_o	V_{in}
FSPPR	$\frac{V_{in}}{2(V_{in}-2V_o)}$	$V_{in}/2$	V_o	$V_{in}/2$
BSPPR	$\frac{V_{in}}{2(V_{in}-2V_o)}$	V_{in}	$2V_o$	V_{in}
MSCPR	$\frac{V_{in}}{2(V_{in}-V_o)}$	$\frac{(V_{in}+V_o)}{2}$	V_o	$\frac{(V_{in}+V_o)}{2}$

exhibits the same utilization as the baseline PR converter due to its asymmetrical energy delivery between cycles [8]. In contrast, both the FSPPR and BSPPR converters show superior utilization under specific input/output voltage conditions compared to the baseline PR converter indicating more efficient usage of charges for power delivery and thereby enhancing overall efficiency.

B. PR Resonant Current and PR Efficiency

The generalized PR resonant current amplitude can be expressed as (8), where the PR utilization factor, K , equivalent PR output voltage, $V_{o,PR}$, and peak-to-peak PR voltage, $V_{p(p-p)}$, are shown in Table II.

$$I_{L,PR(pk)} = \pi \left(\frac{P_o}{2KV_{o,PR}} + f_{sw}C_P V_{p(p-p)} \right), \quad (8)$$

By investigating (8) along with Table II, it can be found that, compared to the baseline converter, the hybrid PR-based

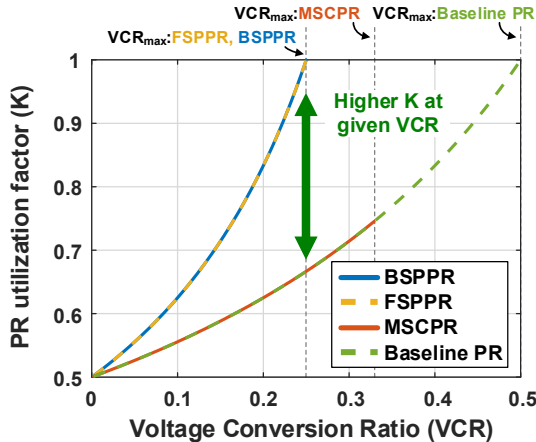
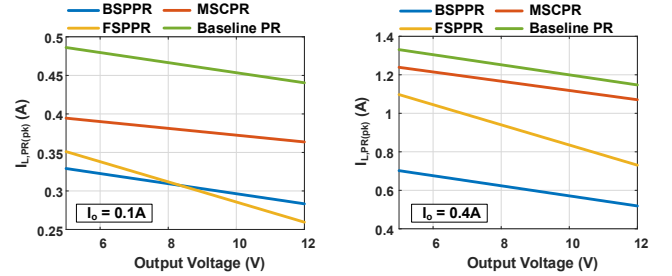


Fig. 5. PR utilization factor versus VCR of different PR-based converter



(a) $V_{in} = 48V$, $I_o = 0.1A$

(b) $V_{in} = 48V$, $I_o = 0.4A$

Fig. 6. Amplitude of PR resonant current at 48V input

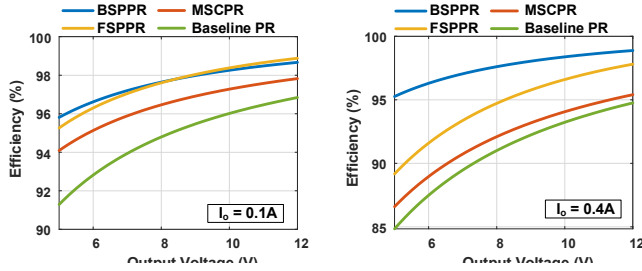
converters generally have a smaller PR resonant current due to the merged SC:

- The MSCPR converter lowers $I_{L,PR(pk)}$ by adjusting $V_{p(p-p)}$ from V_{in} to $(V_{in} + V_o)/2$.
- The FSPPR reduces $I_{L,PR(pk)}$ by setting $V_{p(p-p)}$ to $V_{in}/2$ while increasing K value.
- The BSPPR decreases $I_{L,PR(pk)}$ by increasing both $V_{o,PR}$ and K values

The PR resonant current amplitudes at 48V input voltage and various output conditions are depicted in Fig. 6. It is noticeable that the hybrid PR-based converters have a smaller PR resonant current, aligning with the previous analysis. Particularly, both FSPPR and BSPPR demonstrate even smaller $I_{L,PR(pk)}$ than the MSCPR converter, owing to better K , which implies reduced circulating charges resulting in reduced $I_{L,PR(pk)}$.

In the comparison of the FSPPR and BSPPR converters, the amplitude difference arises from the different strategies adopted in $I_{L,PR(pk)}$ reduction, which can be translated into the output term ($P_o/(2KV_{o,PR})$) and C_P soft-charging term ($f_{sw}C_P V_{p(p-p)}$) reductions in (8). Similar to the distribution of conduction/switching losses, at light load, the C_P soft-charging term predominates $I_{L,PR(pk)}$. On the other hand, as output current increases, the output term begins to dominate $I_{L,PR(pk)}$. Since the FSPPR converter reduces $I_{L,PR(pk)}$ by both $V_{p(p-p)}$ and K , $I_{L,PR(pk)}$ of the FSPPR converter is smaller at light loads and high VCR cases, as shown in Fig. 6(a), compared to the BSPPR converter, which reduces $I_{L,PR(pk)}$ via $V_{o,PR}$ and K . On the other hand, as the output power/current increases, the advantage of the BSPPR, which relocates the PR to the high voltage/low current side, becomes more prominent, presenting a smaller $I_{L,PR(pk)}$ as shown in Fig. 6(b). Given the same PR devices applied, the reduced $I_{L,PR(pk)}$ in the BSPPR converter indicates the ability to operate at a higher output current than others.

There are several sources of loss contributing to PR losses, such as dielectric, piezoelectric, and elastic losses. However, as reported in [11], dielectric and piezoelectric losses are significantly smaller than elastic losses (mechanical losses) and are considered negligible. Hence, the PR loss and efficiency can be simplified as (9) and (10) where R is the mechanical resistance in the BVD model.



Reconfigurable PR-based Power Stage and its auxiliary components

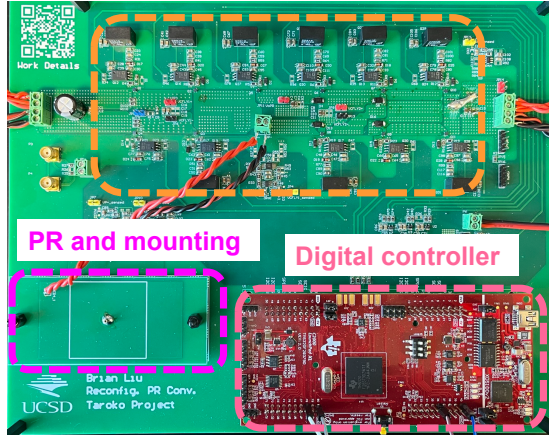


Fig. 8. The BSPPR converter prototype with reconfigurability as the FSPPR and baseline PR converter

$$P_{loss,PR} = \frac{1}{2} I_{L,PR(pk)}^2 R. \quad (9)$$

$$\eta_{PR} = \frac{P_o}{P_o + P_{loss,PR}}. \quad (10)$$

With (10) and (8), the PR efficiency at 48V input voltage and various output conditions are depicted in Fig. 7. Given that the PR efficiency is directly linked to $I_{L,PR(pk)}$, the BSPPR converter demonstrates superior PR efficiency compared to the baseline PR converter due to its reduced $I_{L,PR(pk)}$, especially in higher output current and lower output voltage scenarios.

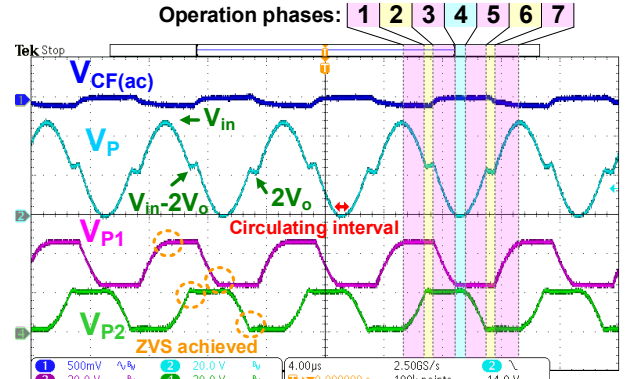
IV. IMPLEMENTATIONS AND EXPERIMENT RESULTS

The proposed BSPPR converter prototype, depicted in Fig. 8, is built alongside configurations to run the circuit as the FSPPR and baseline PR converters, with a PIC181 disk-shaped PR. The parameters of the implementation are shown in Table III. In this design, the sandwich PR mounting approach is employed.

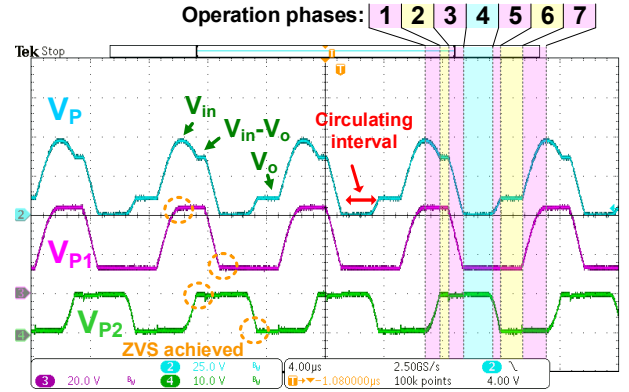
The steady-state operation waveforms of both the BSPPR, and baseline PR converters are shown in Fig. 9 at 48/10V, 0.1A conditions. Based on the waveforms, both converters achieve ZVS but, notably, the BSPPR exhibits shorter PR circulating intervals, implying better PR utilization and efficiency.

TABLE III
EXPERIMENTAL PARTS AND PARAMETERS

Parts/Parameters	Values	implementation
Switches (S1-S8)	80V, 10A, 20mΩ	EPC2214
Digital Controller	150MHz	TMS320F28379D
Piezoelectric Resonator	20/0.2mm (Dia./Thick.)	PIC 181 materials
Input voltage range V_{in}	36-60 V	-
Output voltage range V_o	4-12 V	-
Output current range I_o	0.05-0.3 A	-
flying capacitor C_F	10 μ F	MLCC (0603)
Resonant frequency f_r	≈ 113 kHz	Piezo resonator
Anti-resonant frequency f_r	≈ 129 kHz	Piezo resonator
Quality factor Q	≈ 696	Piezo resonator
FSPPR flying capacitor C_{FF}	4.7 μ F	MLCC (0805)



(a) BSPPR converter @ $V_{in}/V_o = 48/10V$, $I_o = 0.1A$

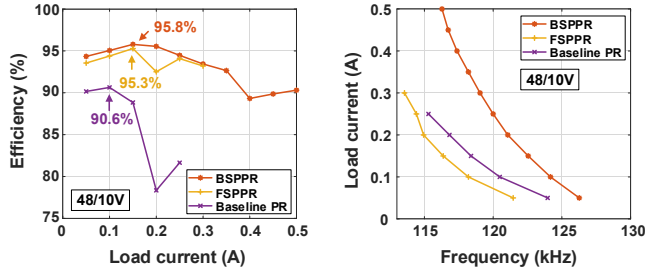


(b) Baseline PR converter @ $V_{in}/V_o = 48/10V$, $I_o = 0.1A$

Fig. 9. Steady-state operation waveforms

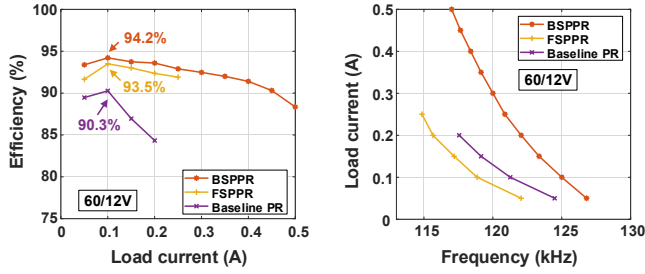
Moreover, V_{P2} of the BSPPR converter swings between 0 to $2V_o$ indicating an operation at an equivalent PR output voltage of $2V_o$, and consequently, implying a lower $I_{L,PR}$ (high voltage/low current side).

The measured efficiency comparisons of the BSPPR, FSPPR, and baseline PR converters at the identical input/output conditions are shown in Fig. 10(a), and 10(c). Here, the BSPPR converter achieves a peak efficiency of 95.8% while extending its operable load range because of a reduced $I_{L,PR(pk)}$ as discussed in section III. Moreover, the BSPPR converter presents enhanced efficiency performance compared to the FSPPR and baseline PR converters across all test



(a) Efficiency at 48/10V

(b) Frequency variation at 48/10V



(c) Efficiency at 60/12V

(d) Frequency variation at 60/12V

Fig. 10. Efficiency, and frequency variation curves of PR-based converters
TABLE IV
COMPARISON TABLE

	Baseline PR [3]	FSPPR [7]	BSPPR (This work)
Active footprint	5.8 mm ³ (4x GaN)	10.2 mm ³ (7x GaN)	11.7 mm³ (8x GaN)
Passive footprint	62.8 mm ³ (PR only)	65.2 mm ³ (PR, 1x 0805 Cap.)	65.4 mm³ (PR, 2x 0603 Cap.)
$P_{o(max)}$	2.5 W	3 W	6 W
Power density	36.4 W/cm ³	39.8 W/cm ³	77.8 W/cm³
Peak efficiency	92.1%	95.3%	95.8%

points. Note that the efficiency measurement concludes when the PR exhibits unstable behaviors, including low-frequency oscillations and voltage drops over time.

The frequency variations at the identical input/output conditions are depicted in Fig. 10(b), and 10(d). In general, the frequency approaches resonant frequency as the load increases, and at the same load condition, the operational frequency tends to decrease with a reduction in input voltage. Here, the BSPPR operates at a slightly higher frequency owing to a higher equivalent PR output voltage, suggesting a better usage of the operable frequency range.

The comparison table is presented in Table IV, delineating the volumetric footprints of active and passive power processing components and corresponding performance. As shown, situating the PR on the input side endows the BSPPR converter with enhanced output capabilities and high peak efficiency. Notably, the footprint of MLCC capacitors is small compared

to the PR. Moreover, the strategic positioning of the SC network at the BSPPR converter's output side, operating at lower voltages, enables the utilization of compact 0603 MLCCs; in contrast, the FSPPR demands high-voltage capacitors for SC operations, necessitating the use of larger 0805 MLCCs. The combined advantages of the small footprint and low-voltage operation with MLCCs in the BSPPR converter result in marginal footprint augmentation while maximizing output capabilities. Note that power density is calculated as the peak output power divided by the sum of the footprints.

V. CONCLUSION

This study introduces a hybrid Backside Series/Parallel PR-based converter, designed to enhance the performance of a baseline PR converter, particularly when high step-down conversion ratios are required. The behavior of the proposed converter is analyzed and benchmarked against prior arts. Incorporating a hybrid approach similar to the hybrid buck converter and strategically placing the PR on the input side (high voltage/low current side) enable the BSPPR converter to operate at low VCR ($VCR < 0.2$) with expanded output capability and minimize the PR vibration losses, which correspondingly maximizes the overall efficiency. Finally, the BSPPR prototype demonstrates a peak efficiency of 95.8% alongside a power density of 77.8 W/cm³.

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