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Ohmic contact structures on β-Ga_2O_3 with n+ β-Ga_2O_3 pulsed laser deposition layers

Special Collection: Honoring Dr. Gary McGuire's Research and Leadership as Editor of the Journal of Vacuum Science & Technology for Three Decades

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ABSTRACT

Thin (40–150 nm), highly doped n+ (10^{19}–10^{20} cm^{-3}) Ga_2O_3 layers deposited using pulsed laser deposition (PLD) were incorporated into Ti/Au ohmic contacts on (001) and (010) β-Ga_2O_3 substrates with carrier concentrations between 2.5 and 5.1×10^{18} cm^{-3}. Specific contact resistivity values were calculated for contact structures both without and with a PLD layer having different thicknesses up to 150 nm. With the exception of a 40 nm PLD layer on the (001) substrate, the specific contact resistivity values decreased with increasing PLD layer thickness: up to 8× on (001) Ga_2O_3 and up to 16× on (010) Ga_2O_3 compared with samples without a PLD layer. The lowest average specific contact resistivities were achieved with 150 nm PLD layers: 3.48×10^{-5} $\Omega\,cm^2$ on (001) Ga_2O_3 and 4.79×10^{-5} $\Omega\,cm^2$ on (010) Ga_2O_3. Cross-sectional transmission electron microscopy images revealed differences in the microstructure and morphology of the PLD layers on the different substrate orientations. This study describes a low-temperature process that could be used to reduce the contact resistance in Ga_2O_3 devices.

I. INTRODUCTION

Beta-gallium oxide (β-Ga_2O_3) is a wide bandgap ($E_G \sim 4.8$ eV) semiconductor that has attracted growing interest due to the availability of bulk crystals and a variety of shallow *n*-type dopants (Sn, Si, and Ge)[1] covering a broad doping range. It is considered a promising candidate for next-generation power electronics,[2,3] in part due to the fact that it has a higher theoretical breakdown field and power figure-of-merit than either GaN or SiC.[4]

For power devices, it is necessary to minimize the ohmic contact resistance, which contributes to the on-resistance of the device and increases the conduction losses in the circuit. Reducing the contact resistance is often achieved by doping the semiconductor surface heavily to decrease the depletion width, making it thin enough to allow carriers to the tunnel.[5]

The standard metallization for Ga_2O_3 ohmic contacts consists of annealed Ti/Au.[6–9] Various processes have been reported to reduce the contact resistance of Ti/Au contacts to Ga_2O_3 (Table I). Values range from $\sim 10^{-3}$ to $\sim 10^{-7}$ $\Omega\,cm^2$ and depend on doping concentration and the type of process. Many processes incorporate a highly doped (n+), 100–180 nm-thick Ga_2O_3 layer produced using Si-ion implantation with high-temperature (925–975 °C) activation anneal.[1–4] Several of the aforementioned processes also included reactive ion etching using BCl_3/Ar.[10–13] A specific contact resistance of 4.6×10^{-6} $\Omega\,cm^2$ was achieved using Si-ion

TABLE I. Specific contact resistivity of Ti/Au ohmic contacts on β-Ga_2O_3. UID stands for unintentionally doped.

Metallization	Substrate orientation/ doping concentration (cm^{-3})	Epitaxial layer/doping concentration (cm^{-3})	n^+ processing conditions	n^+ thickness	Doping of n + region (cm^{-3})	ρ_c(Ω cm^2)	Reference
Ti/Au (20/80 nm)	(001) 10^{18}	…	…	…	…	5×10^{-4}	35
Ti/Au/Ni (20/150/ 50 nm)	(010) Fe-doped β-Ga_2O_3	UID β-Ga_2O_3 buffer layer	MOVPE Si-doped Ga_2O_3 films, 600 °C	170 nm	3.23×10^{20}	1.62×10^{-7}	19
Ti/Au/Ni (20/100/ 30 nm)	(010) Fe-doped β-Ga_2O_3	MOVPE β-Ga_2O_3 1.5×10^{17}	SF_6/Ar RIE + Si delta doped then MOVPE regrow, 600 °C	100 nm	1.4×10^{20}	8.3×10^{-7}	10
Ti(50 nm)/Au (30 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	MBE β-Ga_2O_3 10^{17}	Si-implantation, 950 °C activation for 30-min in N_2,	150 nm	5×10^{19}	4.6×10^{-6}	14
Ti (20 nm)/Au (230 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	MBE Sn-doped β-Ga_2O_3 7×10^{17}	Si-implantation, 925 °C activation for 30-min in N_2, and BCl_3/Ar RIE	150 nm	5×10^{19}	8.1×10^{-6}	11
Ti/Au (20/80 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	UID β-Ga_2O_3 buffer layer 10^{17} and MBE Si-doped β-Ga_2O_3 1.8×10^{18}	…	…	…	3.29×10^{-3}	12
Ti/Au (20/80 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	UID β-Ga_2O_3 buffer layer 10^{17} and MBE Si-doped β-Ga_2O_3 1.8×10^{18}	Si-implantation, 950 °C activation for 30-min in N_2, and BCl_3/Ar RIE	180 nm	3×10^{19}	1.51×10^{-4}	12
Ti/Au (20/80 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	UID β-Ga_2O_3 buffer layer 10^{17} and MBE Si-doped β-Ga_2O_3 1.8×10^{18}	Si-implantation, 975 °C for 30-min in N_2 + 975 °C activation for 30-min in N_2, and BCl_3/Ar RIE	180 nm	3×10^{19}	3.93×10^{-5}	12
Ti/Au (20/230 nm)	(010) Fe-doped β-Ga_2O_3 semi-insulating	MBE UID β-Ga_2O_3 buffer layer	Si-implantation, 950 °C activation for 30-min in N_2	150 nm	5×10^{19}	7.5×10^{-6}	13

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implantation (implant dosage = 5×10^{19} cm^{-2}) and a postimplant anneal at 950 °C.[14] In a separate study, contacts on the (010) orientation without implantation were pseudo-ohmic with a specific contact resistivity of $\rho_C \sim 10^{-3}$ Ω cm^2; Si-ion implantation and RIE treatment (MBE)[15,16] and metal organic vapor phase epitaxy (MOVPE) have also been used to create highly doped Ga_2O_3 layers for ohmic contacts.[10,17,18] Low-resistance (8.3×10^{-7} Ω cm^2) ohmic contacts were achieved on a Si-doped β-Ga_2O_3 (1.4×10^{20} cm^{-3}) regrown MOVPE layer.[10] The ~100 nm-thick n+-Ga_2O_3 growth step was preceded by a heavy Si delta doping at the etched Ga_2O_3 surface in the contact region. The lowest specific contact resistance (1.62×10^{-7} Ω cm^2) was achieved on heavily doped (3.23×10^{20} cm^{-3}) MOVPE layers.[19]

In this study, we investigated the use of thin (~40–150 nm), highly doped (n+) Ga_2O_3 layers deposited using pulsed laser deposition (PLD) as an approach to reduce the contact resistance of Ti/Au ohmic contacts on (001) and (010) β-Ga_2O_3 substrates. PLD has been demonstrated to readily produce highly conductive β-Ga_2O_3 films.[20–24] The use of PLD could simplify processing and avoid the high temperatures (900–1000 °C) associated with Si-ion implantation.[11–14]

II. EXPERIMENT

A. β-Ga_2O_3 samples

Single-crystalline, Sn-doped (*n*-type) β-Ga_2O_3 wafers produced by the edge-defined film-growth (EFG) method were purchased from Novel Crystal Technology, Japan. Two orientations with slightly different doping concentrations were used: (001) with $N_D = 5.10 \times 10^{18}$ cm^{-3} and (010) with $N_D = 4.80 \times 10^{18}$ cm^{-3} or $N_D = 2.50 \times 10^{18}$ cm^{-3}. A commercial pulsed laser deposition system with a KrF excimer laser, located at the Air Force Research Laboratory, was used to deposit n+ layers from a Ga_2O_3–1 wt. % SiO_2 target. The base pressure of the PLD chamber was 2.66×10^{-6} Pa, and deposition was performed in Ar at 13.3 Pa. The substrate temperature was 550 °C, and the laser was operated at a pulse rate of 10 Hz with an energy density of 3 J cm^{-2} measured at the target. The thicknesses of the PLD layers were 40, 80, and 150 ± 10 nm, based on a growth rate of 96 nm/h.[20]

B. Device fabrication

The substrates were ultrasonicated in acetone, isopropyl alcohol, and de-ionized (DI) water for 10 min each and blown dry in nitrogen after each step.[6] Ti/Au (20 nm/80 nm) ohmic contact metal stacks were deposited onto the Ga_2O_3 substrates (with or without PLD layers) via electron-beam evaporation using a Kurt Lesker PVD 75 deposition system having a base pressure of ~3.3×10^{-5} Pa. Circular transfer length method (CTLM) patterns for measuring contact resistance were fabricated using photolithography as described below. First, a negative resist was used to pattern the CTLM mask, followed by UV exposure and development to expose the desired areas. CTLM structures comprised contact spacings, d = 10, 20, 30, 40, 50, and 60 μm, and the inner circle radius was fixed at 100 μm [Fig. 1(b)]. The contacts were etched using a Commonwealth Scientific Ion Mill (base pressure = ~10^{-5} Pa) with Ar ions at 30 A and 450 V. It is noted that the ion milling step can

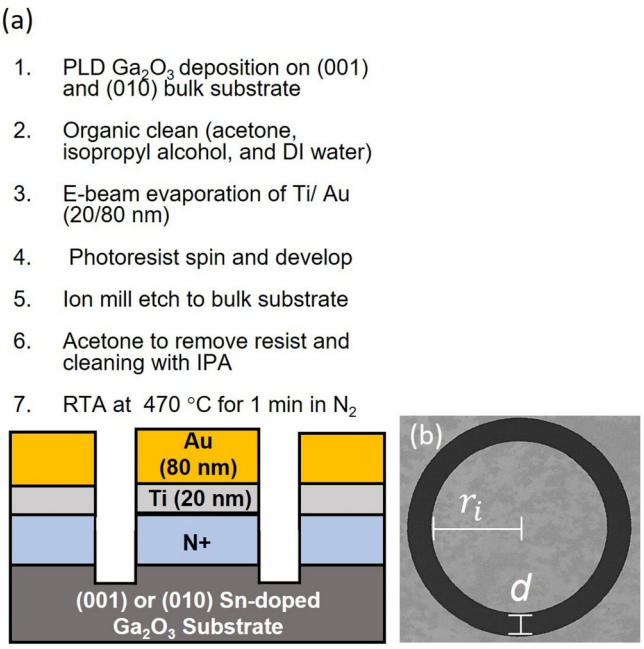

FIG. 1. (a) Device fabrication process flow and schematic illustration of the structure in the cross section. (b) Optical image of a patterned contact: inner radius, r_i = 100 μm, and contact spacing, d = 20 μm.

produce damage to the contact sidewalls and to the Ga_2O_3 surface area between the contacts but does not damage the Ga_2O_3 surface directly underneath the contacts since these regions are covered and, therefore, not exposed to the ions. To ensure that the Au/Ti/PLD layers were completely etched, each device was overetched 25–33 ± 4 nm (no PLD, 40, and 80 nm samples) and 40–45 ± 5 nm (150 nm samples) into the substrate, as determined from multiple measurements for each sample using a KLA Tencor P-15 profilometer. To complete the ohmic contact processing, the samples were subjected to a rapid thermal anneal (RTA) at 470 °C for 1 min in N_2.[8] A schematic illustration of the fabrication steps and resulting cross-sectional structure is given in Fig. 1.

C. Electrical characterization

I–V characteristics of the fabricated CTLM devices were collected with an Agilent 4155C semiconductor parameter analyzer with a Signatone S-1160-4 N probe station. A voltage ranging from −1 to 1 V was applied between a probe placed on the inner metal circle and one on the outer metal area. Five to eight sets of CTLM structures were measured for each sample, and the specific contact resistivity value was taken from the average of these sets.

Hall measurements were conducted at room temperature using a Nanometrics HL5500 Hall System with a magnetic field strength of 0.5 T. Ti/Al/Ni/Au (20/100/50/50 nm) ohmic contacts were deposited via electron-beam deposition in a van der Pauw pattern followed by an RTA at 470 °C for 1 min in N_2. Ohmic contacts were placed on bare (001) and (010) Sn-doped β-Ga_2O_3

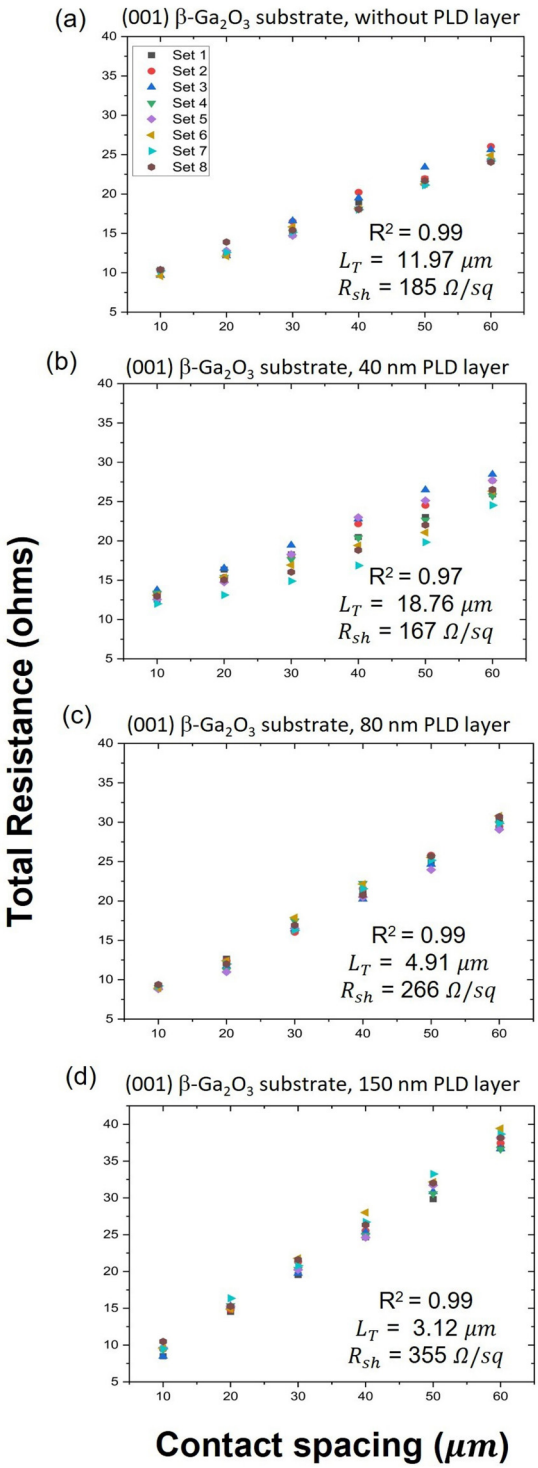

FIG. 2. Total resistance vs contact spacing plots for Ti/Au contacts on (001) β-Ga_2O_3 substrates (a) without a PLD layer and with an n + Ga_2O_3 PLD layer having a deposited thickness of (b) 40, (c) 80, and (d) 150 nm.

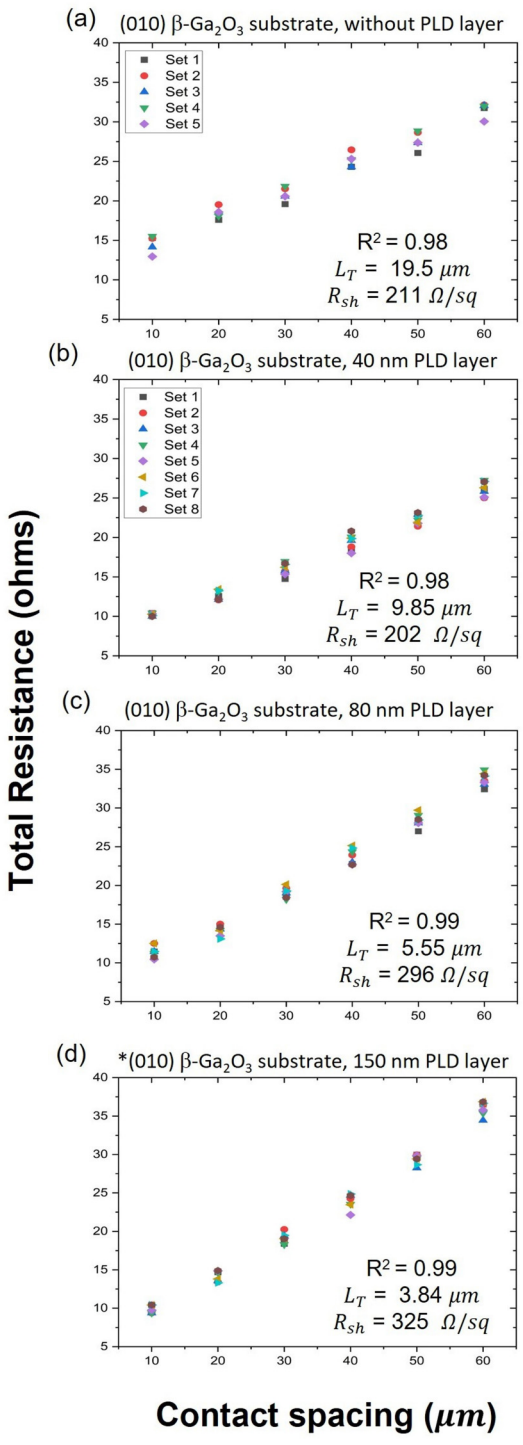

FIG. 3. Total resistance vs contact spacing plots for Ti/Au contacts on (010) β-Ga_2O_3 substrates (a) without a PLD layer, and with an n + Ga_2O_3 PLD layer having a deposited thickness of (b) 40, (c) 80, and (d) 150 nm. *Substrate from different wafer batch (see Table II).

TABLE II. Summary of results from Hall and CTLM measurements. *Indicates different wafer batch.

Hall measurement			CTLM specific contact resistivity(Ω cm^2)			
Substrate orientation	Substrate carrier concentration (cm^{-3})	PLD layer carrier concentration (cm^{-3})	No PLD	40 nm Si-doped PLD	80 nm Si-doped PLD	150 nm Si-doped PLD
(001)	5.10×10^{18}	2.60×10^{19}	2.64×10^{-4}	5.88×10^{-4}	6.41×10^{-5}	3.48×10^{-5}
(010)	4.80×10^{18}	2.00×10^{20}	8.03×10^{-4}	1.96×10^{-4}	9.11×10^{-5}	…
*(010)	2.50×10^{18}	2.80×10^{20}	…	…	…	4.79×10^{-5}

substrates to obtain the carrier concentration of each substrate and on (001) and (010) Fe-doped β-Ga_2O_3 substrates coated with Si-doped β-Ga_2O_3 PLD layers to obtain the carrier concentrations of the PLD layers.

D. TEM sample prep and characterization

Selected samples were prepared for characterization using transmission electron microscopy (TEM). The samples were capped with platinum to prevent damage during the sample preparation process. Liftout and thinning were achieved using a FEI Helios 650 Nanolab focused ion beam (FIB) instrument. After liftout, the samples were attached to a Cu TEM grid and thinned to ~65 nm. Scanning transmission electron microscopy (STEM), high-angle annular dark field (HAADF) imaging, and energy-dispersive x-ray (EDX) analysis were conducted using a Themis 200 TEM. High resolution TEM (HRTEM) images were obtained using a Tecnai F20 TEM.

III. RESULTS AND DISCUSSION

The I–V curves for contacts on all samples were linear. These measurements confirmed that the contacts were ohmic. I–V measurements of individual sets of CTLM patterns were used to calculate the specific contact resistance values for each sample. First, the total resistance R_t (Ω) was determined by measuring the voltage drop while passing a known current through the inner and outer metal pads with a separation d. The CTLM patterns used here consist of circular contacts with 100 μm radius, separated from the surrounding metal by gaps, $d = 10$, 20, 30, 40, 50, and 60 μm. According to the CTLM theory,[26] the measured resistance, R_t, should vary linearly with the contact spacing, d. This relationship can be expressed as

$$R_t = \frac{R_{sh}}{2\pi r_i}(d + 2L_t)C, \tag{1}$$

where R_{sh} represents the sheet resistance, r_i is the inner radius, and L_T is the transfer length. C is a unitless geometrical correction factor given by

$$C = \frac{r_i}{d}\ln\left(1 + \frac{d}{r_i}\right). \tag{2}$$

For contacts on semiconductor layers that are thicker than the contact spacing d, the current flows primarily in the topmost layer of the semiconductor. The thickness of this layer and its effective sheet resistance were calculated for a similar contact structure and similar doping concentration in the Ga_2O_3 substrate to be ~40 μm and ~5 Ω/sq, respectively.[25] For these conditions, the CTLM equations should be valid for specific contact resistivity values > 10^{-6} Ω cm^2.[26]

Plots of total resistance vs contact spacing for five to eight sets of CTLM patterns for each PLD layer thickness are shown in Figs. 2 and 3 for the (001) and (010) substrates, respectively. For ease of data interpretation, the y axis in Figs. 2 and 3 corresponds to the measured total resistance divided by the correction factor, calculated individually for each value of d, i.e., $R_T(d)/C(d)$. In general, the

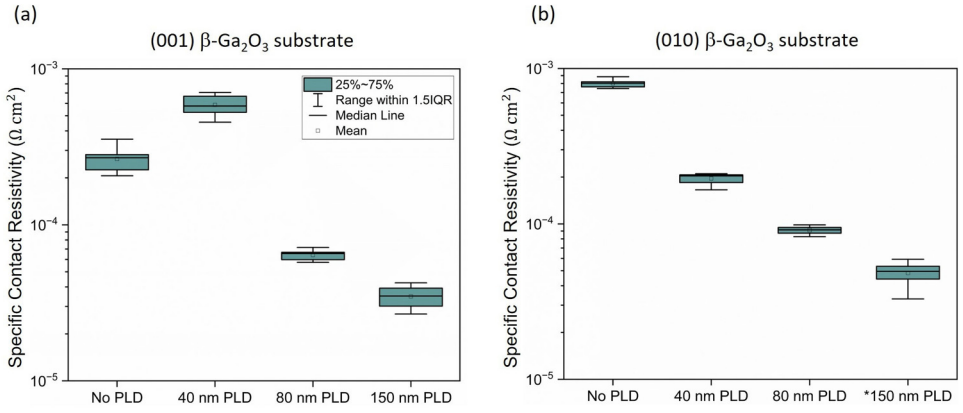

FIG. 4. Specific contact resistivity values for Ti/Au contacts on (a) (001) and (b) (010) β-Ga_2O_3 substrates for different thicknesses of n + β-Ga_2O_3 PLD layers; calculated from data plotted in Figs. 2 and 3, respectively. *Substrate from different wafer batch (see Table II).

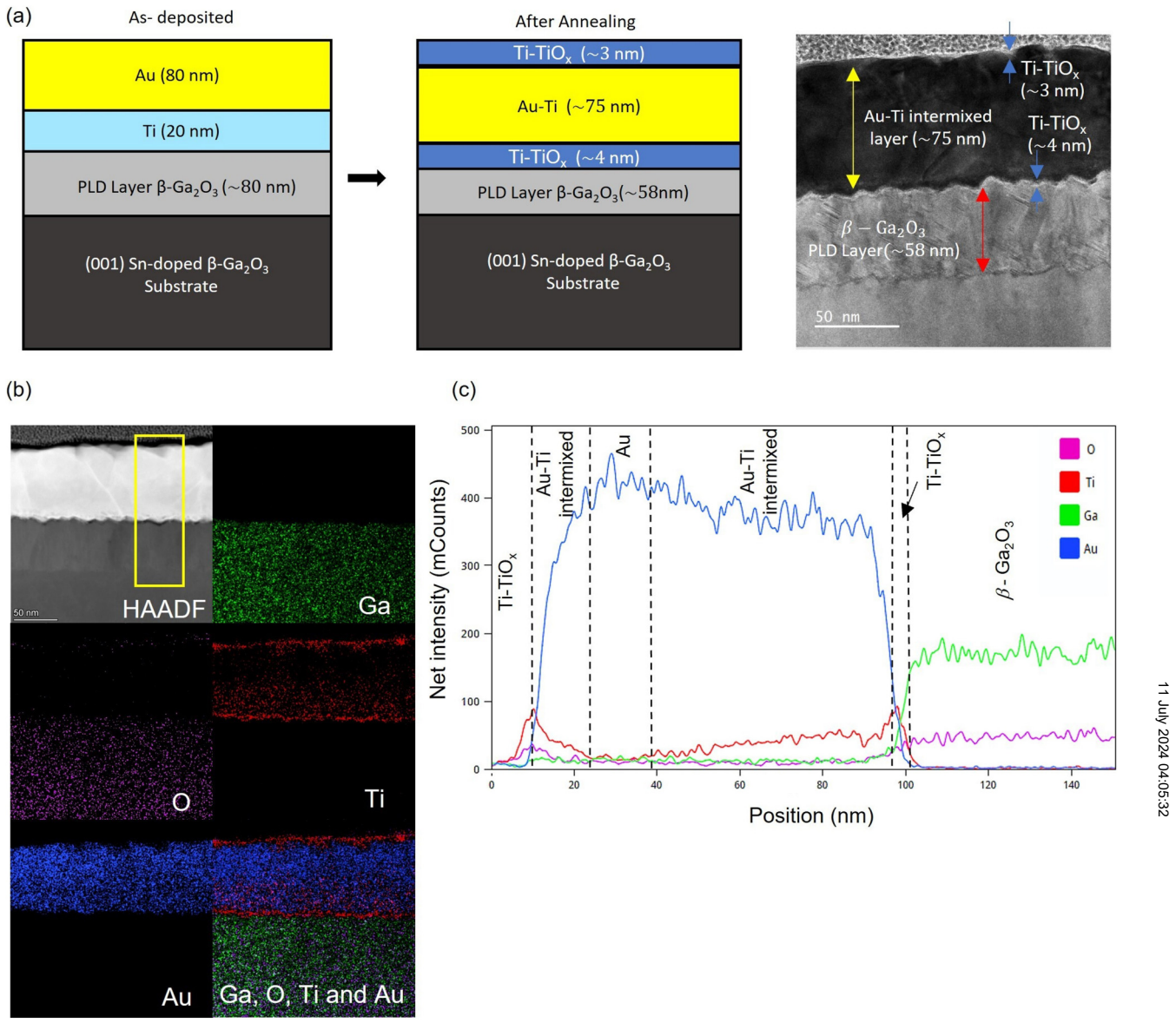

FIG. 5. (a) Schematic illustrations and TEM image of Ti/Au on the (001) β-Ga_2O_3 substrate (zone axis: [0$\bar{1}$0]) with an n + Ga_2O_3 PLD layer (deposited thickness = 80 nm) (zone axis: [010]), after annealing at 470 °C in N_2 for 1 min. (b) EDX elemental maps of Ga (green), O (purple), Ti (red), and Au (blue); and (c) EDX areal profiles across the interface [yellow box in Fig. 5(b)]. Six distinct layers are marked. From bottom to top, these are β-Ga_2O_3, Ti − TiO_x, Au–Ti intermixed, Au, Au–Ti intermixed, and another layer of Ti − TiO_x.

resistance increased with increasing d, as expected. From these plots, parameters such as L_T and R_{sh} can be extracted.[27,28] Modest increases in calculated sheet resistance were observed with increasing n+ PLD thickness; this result could be associated with higher roughness between the contacts due to higher over-etching to ensure that the thicker PLD layers were completely removed. Other factors, such as increased current crowding at contact edges, as transfer length decreases, might also contribute to changes in the calculated sheet resistance underneath and between the contacts. The specific contact resistivity, ρ_c, can be expressed as

$$\rho_c = R_{sh} \cdot L_t^2. \tag{3}$$

The quality of the linear fit is measured by the Pearson product (regression coefficient, R^2). In the ideal situation, the Pearson product equals unity ($R^2 = 1$). R-squared values for these

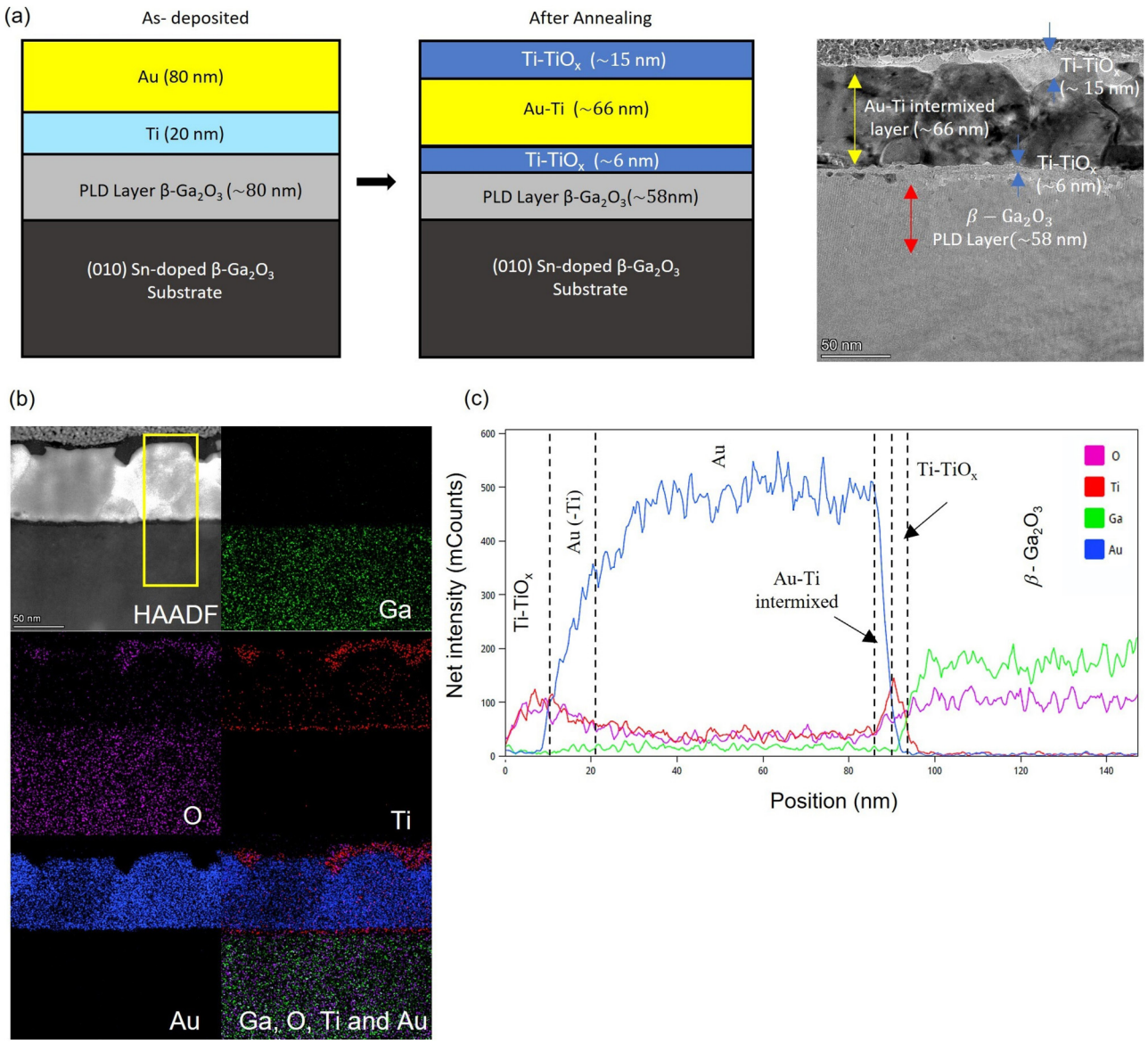

FIG. 6. (a) Schematic illustrations and TEM image of Ti/Au on the (010) β-Ga_2O_3 substrate (zone axis: [001]) with an n + Ga_2O_3 PLD layer (deposited thickness = 80 nm) (zone axis: [001]), after annealing at 470 °C in N_2 for 1 min. (b) EDX elemental maps of Ga (green), O (purple), Ti (red), and Au (blue); and (c) EDX areal profiles across the interface [yellow box in Fig. 6(b)]. Six distinct layers are observed. From bottom to top, these are β-Ga_2O_3, Ti − TiO_x, Au–Ti intermixed, Au, Au–Ti intermixed, and another layer of Ti − TiO_x.

data are typically, $R^2 = 0.99$. However, in some cases, there was significant scatter, e.g., 40 nm PLD layer on the (001) substrate.

Table II and Fig. 4 show the specific contact resistivity values calculated from the data shown in Figs. 2 and 3. The average specific contact resistivities for contacts without a PLD layer were 2.64×10^{-4} and $8.03 \times 10^{-4}\,\Omega\,cm^2$, on the (001) and (010) substrates, respectively. The different values can be attributed to the anisotropic properties of different β-Ga_2O_3 surfaces and to the slightly higher doping concentration in the (001) substrate. Different thermal, optical, and electrical properties along different β-Ga_2O_3 crystal directions have been reported.[29–32]

β-Ga_2O_3 has two strong cleavage planes of (100) and (001) with low surface energies potentially susceptible to the growth of off-axis planes. Substrate orientations for the epitaxial growth of β-Ga_2O_3 films with high electrical quality are typically (010) or (100) with miscuts. Homoepitaxial growth on (001) by MBE

revealed an additional ($\bar{4}01$) reflection by x-ray diffraction and depositions in this work by PLD on (001) also indicated a minor ($\bar{4}01$) contribution.[33] The additional planes could possibly generate point defects in the lattice causing Ga vacancies, which are dominant acceptors. Lower carrier concentrations in films deposited on (001) substrates are, thus, attributed to elevated acceptor levels.

For the (010) substrate, the contact resistance values decreased as the PLD layer thickness increased. The lowest average value of $4.79 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ on the (010) substrate was achieved for a PLD layer thickness of 150 nm. For the (001) substrate, the contact resistivity initially increased for contacts with a 40 nm PLD layer. This increase could be associated with the nonuniformity of the thin PLD layer (e.g., in terms of thickness, doping, and/or stoichiometry); as discussed above, the TEM results indicate that the PLD layers grow differently on different surface orientations. However, the contact resistivity decreased for (001) contacts with thicker (80 and 150 nm) PLD layers. The (001) substrate with the 150 nm PLD layer had the lowest average value of specific contact resistivity: $\rho_c = 3.48 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$. The lowest contact resistance values for both (010) and (001) substrates were achieved for contact structures that comprised PLD layers having a deposited thickness of 150 nm, which is in the range of thicknesses of reported n+ layers used to reduce the contact resistance in Ga_2O_3 ohmic contacts (see Table I). However, further investigation is required to precisely determine the optimal thickness of the n+ PLD layer.

We note here that the contact resistivity values were typically lower for the (001) substrate than the (010) substrate even though the carrier concentration was approximately an order of magnitude lower in the PLD layers grown on the (001) substrates. This is further evidence that the PLD layers in the gaps between contacts were completely etched during the ion milling step, indicating that the n+ PLD layers provide a low-resistance tunneling barrier for current transport into the β-Ga_2O_3 substrate.

Contact structures were characterized in the cross section using TEM to investigate the microstructure, morphology, and chemical compositions. The thickness of the as-deposited PLD layers in the samples selected for analysis was 80 nm. HAADF STEM images of annealed contact structures on (001) and (010) β-Ga_2O_3 substrates are shown in Figs. 5(a) and 6(a), respectively. It is apparent from the images that, after annealing, the thickness of the PLD layers was reduced by ~20 nm. The PLD film grown on the (001) substrate appears to comprise multiple grains, whereas the film grown on the (010) substrate appears epitaxial such that the interface between the substrate and film is difficult to discern. Additional TEM images and FFT diffraction patterns are included in the supplementary material.[34] The layers on both substrates, however, appear continuous and without voids. According to EDX analysis [Figs. 5(b), 5(c), 6(b), and 6(c)], a similar layered structure is present on both substrates after annealing. From bottom to top, the layers can be described as Ti – TiO, intermixed Au–Ti, Au, intermixed Au–Ti, and another layer of Ti – TiO_x.

IV. CONCLUSIONS

The results of this study show that thin n+ Ga_2O_3 PLD layers can be used to reduce the contact resistance of Ti/Au ohmic contacts on (001) and (010) β-Ga_2O_3 substrates. The specific contact resistance was reduced by up to 8× and 16× on (001) and (010) substrates, respectively. The results provide a point of reference for the further optimization of highly doped Ga_2O_3 PLD layers to minimize the contact resistance in Ga_2O_3 devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Elizabeth V. Favela: Conceptualization (equal); Data curation (equal); Formal analysis (lead); Investigation (equal); Methodology (equal); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Hyung Min Jeon:** Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Kevin D. Leedy:** Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (equal); Writing – review & editing (equal). **Kun Zhang:** Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Writing – review & editing (equal). **Szu-Wei Tung:** Investigation (equal); Writing – review & editing (equal). **Francelia Sanchez Escobar:** Investigation (equal); Validation (equal); Writing – review & editing (equal). **C. V. Ramana:** Funding acquisition (equal); Supervision (equal); Writing – review & editing (equal). **Lisa M. Porter:** Conceptualization (equal); Funding acquisition (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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