Research Experiences for Teachers on Chip Design

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***Abstract*—This paper presents the first Research Experience for Teachers (RET) site in the United States on integrated circuit (IC) design and education for high school and community college teachers. Motivated by the enormous upcoming semiconductor workforce demand spurred by investments from the CHIPS and Science Act, we offered a six-week paid RET program for ten teachers in Oklahoma to learn about semiconductors and chip design. Teachers were also required to translate their experience into new curriculum modules. Our training leveraged the web-based Silicon Layout Wizard (Siliwiz), Wowki template, and the Tiny Tapeout flow, all running in a browser using the open-source Skywater 130 nm CMOS process. We also provided curriculum design training so teachers could teach the new materials more effectively. Among the ten participants, six successfully submitted their GDS files for fabrication. Four presented at the 2023 ASEE virtual poster sessions. Evaluation data indicated the challenges teachers initially faced and the enthusiasm they sustained throughout the RET program.**

***Index Terms*—semiconductor workforce development, teacher training, STEM education, integrated circuits, CMOS**

I. Introduction

Semiconductor workforce development is becoming one of the STEM education priorities in the United States [1]. A skilled and diverse pipeline of workers is critical to building a sustainable domestic semiconductor industry and to achieve the CHIPS Act economic and national security goals [2]. The CHIPS Act has already sparked more than $200 Billion in private and public investments in US semiconductor production [3]. The challenge now becomes how to train enough students to meet this demand quickly.

Since 2022, many universities, such as Purdue, Ohio State, and Arizona State University, have introduced programs to address the semiconductor talent shortages [4]. However, university education alone may not solve this problem. Figure 1 shows the semiconductor occupational profile based on [5]. Engineering occupations, which college graduates with BS, MS, or PhD degrees will likely pursue, consist of only 24% of the total jobs available. Production occupations, on the other hand, represent 39%. If we seek to fill all vacant jobs, high school and community college students should be key [4], and we must create a pathway for non-college graduates to participate in the semiconductor ecosystem.

However, many high schools do not have any material related to semiconductors or microelectronics. A study in 2010 [6] showed that despite transistors being invented in the 1940s, high school physics curricula did not have any materials on solid-state electronics. Hence, students remain uninformed about the principles of semiconductors or the exciting career opportunities the chips industry offers.

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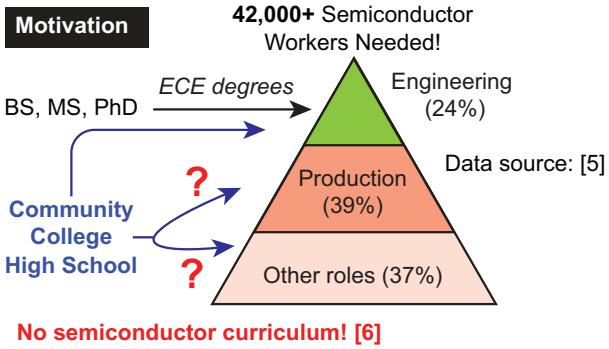

Fig. 1. Motivation for our RET program: The lack of teachers and curriculum

Motivated by the workforce needs and the vacancy in pre-college semiconductor education, this paper proposed a Research Experience for Teachers (RET) program to train K-14 teachers on semiconductor basics. Teacher training is a critical prerequisite (though insufficient) toward introducing high school and non-college graduates into the semiconductor workforce. The contributions of our paper include:

1) We present the first RET program in the US focused on chip designs and K-14 semiconductor education.
2) Our training was done in a web browser without access to a Linux server or proprietary software. Thus, it can be more accessible to high school teachers and students.
3) We provided dedicated curriculum design training so teachers could teach the new materials more effectively.

The rest of the paper is organized as follows. Section II describes our participants and recruitment. Section III details our training contents and methods. Section IV explains our curriculum design training. Section V presents teacher evaluation and feedback. Finally, Section VI concludes this paper.

II. Participants and Recruitment

Recruitment is critical for any RET program to succeed. We learned from past NSF RET program recruitment strategies [7]–[9] and leveraged existing relationships between local schools and our institution. Our target population was any STEM teachers teaching in high schools or community colleges (Grades 9-14) in Oklahoma. We chose them because their students are more mature, close to college education, and are ready to join the workforce upon graduation.

We recruited from all schools with particular emphasis on teachers serving high minority students, rural areas, and high percentage of students eligible for free or reduced (F/R) lunch programs [10] to ensure diversity and inclusiveness. Table I shows our 2023 trainee profiles and their schools' demographics. Their teaching subjects include math, chemistry, computer science, robotics, and general STEM.

TABLE I
2023 RET PARTICIPANTS' STATISTICS

No.	School Name	Minority Students	F/R	Rural
5	Dove HS	83% Hispanic	85%	No
2	Cushing HS	15% Native	66%	Yes
1	Kingfisher HS	21% Hispanic	45%	Yes
1	OSSM HS	state-wide recruit	residential	
1	NOC	community college	transfer students	

III. TECHNICAL TRAINING AND METHODS

Table II shows our six-week RET program schedule. Two features set us apart from other NSF RET programs [7]–[9]: (1) Dedicated curriculum and pedagogy training (Week 1 and 6). (2) A more compressed technical program (4 weeks instead of 6). Hence, we had to design our training to maximize effectiveness under time constraints.

TABLE II
SIX-WEEK TRAINING SCHEDULE

Week	Topics & Activities
1	Introduction, Lab Tours, Curriculum Basics
2	Siliwiz and Wowki: Digital Design Guide (SKY130)
3	Analog/digital project breakout, Mid-term presentations
4	Analog: SPICE simulator, Digital: Wowki
5	Analog: ADALM, Digital: Tiny Tapeout, ASEE conference
6	Curriculum Peer-to-Peer Feedback, Final Poster Session

A. Introduction: (Week 1)

Week One introduced the semiconductor fundamentals and laid a foundation for meaningful research. We provided two half-days of conventional lectures to meet these goals. The first part of the lecture provided an overview of the semiconductor industry in the US with an emphasis on their applications, growth potential, and need for a skilled workforce. Afterward, all three areas of semiconductors, namely materials, devices, and integrated circuits, were introduced. The second-day lecture covered the integrated circuits design and fabrication process with real-world examples and visual aids.

We also offered guided lab tours by faculty members researching various chip design fields. The faculty mentor of an analog IC lab demonstrated a dynamic-bias CMOS comparator they fabricated to reproduce the work in [11]. In an RFIC research lab, teachers examined unpackaged integrated circuits through a microscope and operated basic IC testing equipment such as a probe station.

B. CMOS Process and PDK: (Week 2)

Week Two training centered around the basics of a CMOS process and the Google/Skywater 130 nm open process design kits (PDK) [12], [13]. A common challenge in semiconductor education is the limited access to PDKs [14]. In our training, we chose Siliwiz [15], a web-based platform to learn and interact with SKY130 PDK. As such, teachers did not need to log into a Linux server or install proprietary software like Cadence. Siliwiz allowed teachers to draw rectangles and arbitrary shapes to represent n-wells, p diffusion, and metal layers 1 to 3 in a web browser. The SKY130 design rules (DRC) would automatically apply, and even a SPICE netlist could be generated automatically based on the dimension of the transistor drawn. Teachers then clicked a button to simulate their drawn circuit in the browser and plotted the waveforms for different nodes. Figure 2 shows a snapshot of a CMOS inverter drawn in Siliwiz. The simulation waveform could be zoomed in and out through the interactive tool bars.

C. The Digital Project: (Week 3 to 5)

Starting in Week 3, teachers chose to work on an analog or digital project. In the digital project, teachers would implement a logical function of choice and turn their designs from ideas to manufacturable GDS files.

Wowki template: The digital design took place in a web browser using a Wowki template. Wowki is a web-based simulator often used for Arduino and other virtual hardware simulations [16]. Our training partner developed a Wowki digital design template with interactive Input/Outputs (I/O) such as switches, LED lights, and a seven-element display. Teachers could drag and drop pre-built logic gates (i.e., NAND, NOR) and D flip-flops onto the canvas and connect them to implement their logical functions. The Wowki template also had built-in simulation capabilities with animations.

Tiny Tapeout: Once teachers were satisfied with their logical designs in Wowki, they could submit them using a GitHub action system for fabrication in Skywater open source 130 nm process. Each teacher created their own GitHub account. Then, they forked the submission template and edited the relevant fields (e.g., Wowki ID, designer name, functional and test descriptions) in the submission template. Once they clicked submit, the GitHub action system would automatically grab their Wowki design, check for DRC, and generate a GDS file ready to be fabricated. If there were errors, the GitHub action system would prompt the teachers to fix them and resubmit their designs.

Outcome: Six out of seven teachers successfully submitted their design to one of the Skywater Multi-Wafer Project shuttles in September 2023. Figure 3 shows an even-number counter created by one of our teachers. The Wowki design used 2 AND, 4 OR, 1 XOR, and 4 D Flip-flops. The function of the circuit was to show the next even number (0, 2, 4, 6, 8) on the 7-segment LED display each time the push-button switch was pressed. The GDS file was auto-generated by the GitHub action system. The 3D viewer could highlight each standard cell's location within the final layout.

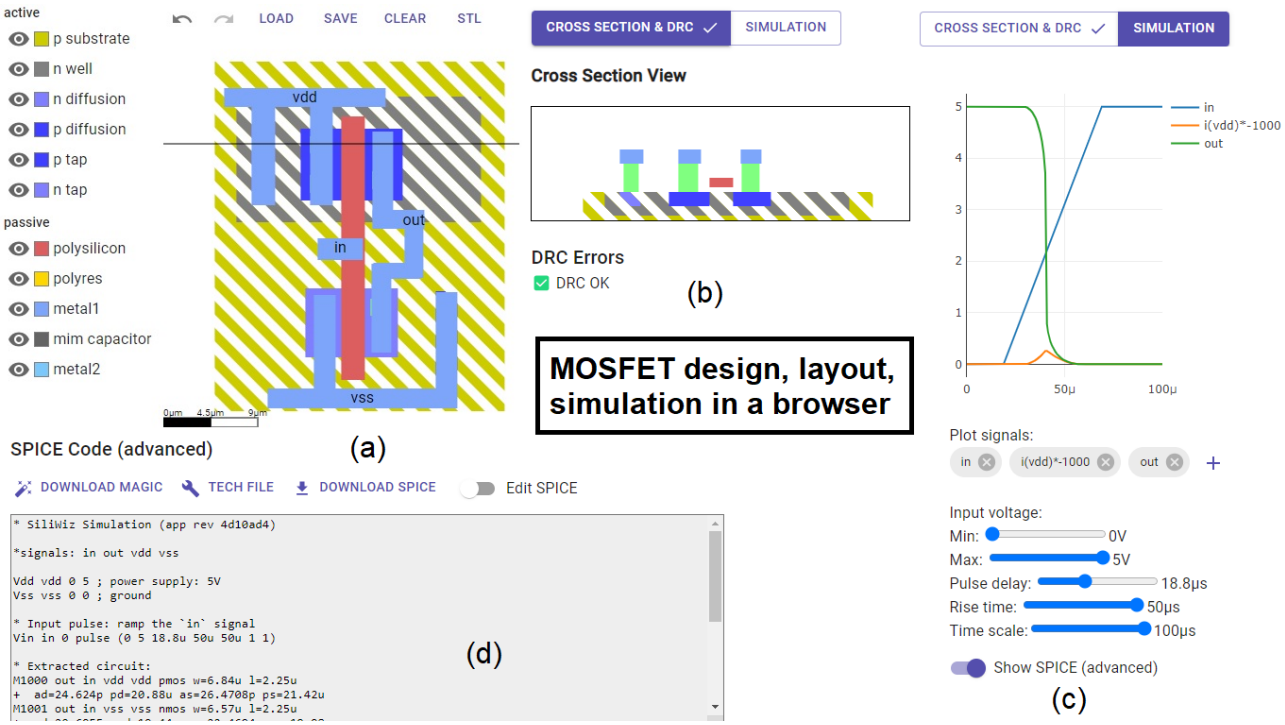

Fig. 2. Siliwiz [15]: CMOS transistor design and simulation in a web browser. (a) SKY130 layer drawing from scratch, (b) autogenerated SPICE netlist from layout, (c) cross-section view of layout and DRC results, (d) interactive waveform viewing from the SPICE transient simulation

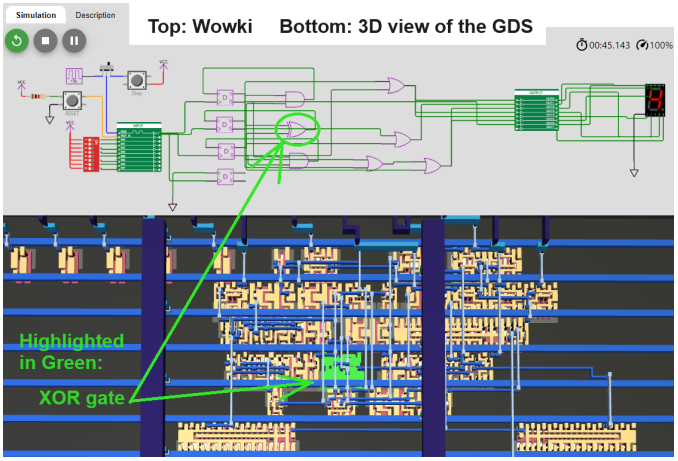

Fig. 3. A even-number counter design in Wowki and its GDS file (3D view) created by one of our teachers

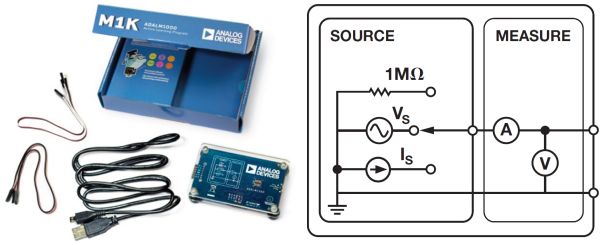

Fig. 4. ADALM1000 evaluation board and its block diagram [22].

D. The Analog Project: (Week 3 to 5)

The goal of the analog project was for teachers to learn and be able to explain to their students two things: (1) What is analog? Why do we need analog in an increasingly digital world? (2) How to learn analog by yourself?

To answer (1), we gave an hour lecture based on [17] that focused on the differences between analog and digital. To answer (2), we introduced SPICE ("Simulation Program with Integrated Circuit Emphasis"), a general-purpose, open-source analog electronic circuit simulator [18]. In the summer of 2023, we based our training on LTspice [19], which contained chip macro models for simulations. This feature was handy for some RET teachers when they guided their students to design printed circuit boards (PCB) for robotic competitions [20]. During the training, we asked teachers to reproduce the circuits and simulations in the schematic editor, the waveform viewer, and AC analysis tutorials [19]. However, we know that other SPICE versions (e.g., NGSPICE [21]) are more amiable to transistor designs, particularly in Skywater PDKs. We plan to include them in our future training.

ADALM1000 is a pocket-sized evaluation board to introduce the concepts of voltage, current, and impedance [22]. The board hosts two high-precision analog channels, each capable of generating or measuring analog signals at up to 100 kilosamples per second (kSPS), as seen in Figure 4. We taught teachers how to read the hardware manual [23], schematics, board layout, and integrated circuit (IC) datasheets. This know-how was essential for teachers to advise their students.

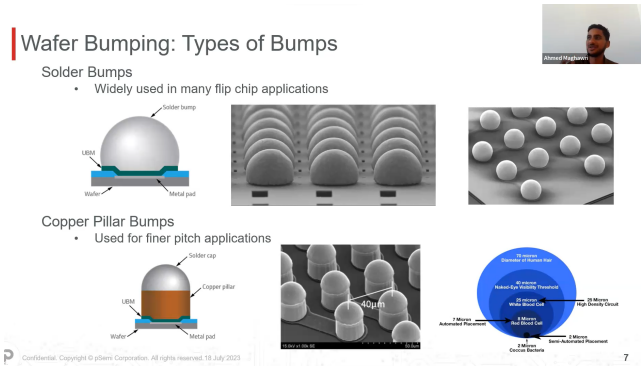

Fig. 5. Zoom Talk by a pSemi engineering on IC Packaging

E. Industry Talks

For teachers to better understand the big picture of the semiconductor industry and the different jobs and skills required, we partnered with pSemi, a high-performance RF CMOS IC company and arranged a dozen Zoom talks for our participants. Fig. 5 shows a screenshot during a talk on IC packaging. As teachers' knowledge grew, they responded more favorably toward the content. As one teacher commented:

"*Just how much we've all learned about the semiconductor manufacturing process as several guest speakers from pSemi outlined their roles in the process... and it all felt familiar. Five weeks ago, it was Martian-speaking.*"

IV. Curriculum Design Training

Description: During Week 1, teachers undertook two workshops on a tri-part framework for curriculum design: cultural relevance, concept-based understanding, and backward design. Cultural relevance emphasizes the need to understand students' linguistic, geographic, gender, racial, and generational, among other cultural, knowledge as assets that can be leveraged for curriculum and teaching [24]. Concept-based understanding prioritizes inquiry-based learning and application and transferability of knowledge versus rote memorization of information or discrete skill acquisition. The backward design provides an accessible structure for planning assessment and learning activities in ways that center conceptual understanding and student inquiry [25].

Throughout Weeks 2-5, teachers prioritized chip design learning and research experience while engaging in regular weekly reflection on the development of their curriculum ideas. In Week 6, teachers focused specifically on curriculum design and were mentored to discuss and reflect more deeply on their student communities' social, academic, and cultural contexts. They had opportunities to support one another to creatively navigate the challenges they faced in curricular innovation (e.g., limited curricular autonomy, workload constraints). All participating teachers developed unit curricula through a scaffolded, iterative approach with peer and mentor feedback.

Outcome: All ten teachers finished their initial lesson plans by the end of the training. Four presented their research findings and lesson ideas in the 2023 ASEE NSF RET Virtual poster sessions [26]–[29]. Some new modules will be taught in high school as early as November 2023. We plan to follow up with classroom visits to observe and provide support.

V. Evaluation and Feedback

Method and Data Sources: This paper draws on constant comparative analysis of qualitative data [30] collected during the six-week period. Our data sources included participants' weekly written feedback, reflective midterm, cumulative research posters, participants' iterative curriculum design drafts and peer feedback, and RET mentors' midterm and cumulative reflections.

Data Analysis: Qualitative data was analyzed utilizing an ongoing constant comparative method within an interpretivist paradigm [31]. The coding of qualitative data occurred in stages. First, data underwent initial open coding, centering participants' meanings and perspectives. The second stage of analysis entailed in-depth focused coding, which is more "directed, selective, and conceptual" [31] and refines and clarifies codes, categories, and their significance.

Findings: While the complete data analysis is ongoing, we report here on two findings: (1) learning chip designs and translating them into understandable curricula were by no means easy for teachers. This can be seen from teachers' feedback in Table III. (2) Despite the challenges, teachers were enthusiastic about semiconductors and were eager to learn. This enthusiasm was also reflected in other data sources.

TABLE III
Teacher Feedback: Selected Quotes

Week	Teachers' Comments on Weekly Feedback Forms
1	"There are too many things we need to know." "How to apply to my class"; "How we will teach to students"
2	"This old brain is being tasked with some daunting knowledge but it's all so interesting, which provides plenty of motivation."
3	"The material is hard to understand but interesting to learn."
4	"How to close my knowledge gap to teach my students."
5	"How I'm going to sustain my level of enthusiasm?" "Will I be able to connect with real semiconductor industry employees for my students?"

VI. Conclusion

This paper presents the first RET program in the US focused on semiconductor education and chip design. By leveraging web-based Siliwiz, Wowki template, and the Tiny Tapeout flow, teachers could finish a tiny chip design from ideas to GDS files without logging in to a Linux server. We also provided dedicated curriculum design training to increase their teaching effectiveness.

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