

# Implementation of High-Performance and High-Yield Nanoscale Hafnium Zirconium Oxide based Ferroelectric Tunnel Junction Devices on 300mm Wafer Platform

Running title: Nanoscale Hafnium Zirconium Oxide based Ferroelectric Tunnel Junctions

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In this work, hafnium zirconium oxide (HZO)-based 100 nm x 100 nm ferroelectric tunnel junction (FTJ) devices were implemented on a 300 mm wafer platform, using a baseline 65 nm CMOS process technology. FTJs consisting of TiN/HZO/TiN were integrated in between metal 1 (M1) and via 1 (V1) layers. Cross-sectional transmission electron microscopy and energy dispersive x-ray spectroscopy analysis confirmed the targeted thickness and composition of the FTJ film stack, while grazing incidence, in-plane x-ray diffraction analysis demonstrated the presence of orthorhombic phase Pca2<sub>1</sub> responsible for ferroelectric polarization observed in HZO films. Current measurement, as a function

of voltage for both up and down polarization states, yielded a tunneling electroresistance (TER) ratio of 2.28. The device TER ratio and endurance behavior were further optimized by insertion of thin  $\text{Al}_2\text{O}_3$  tunnel barrier layer between the bottom electrode (TiN) and ferroelectric switching layer (HZO) by tuning the band offset between HZO and TiN, facilitating on-state tunneling conduction and creating an additional barrier layer in off-state current conduction path. Investigation of current transport mechanism showed that the current in these FTJ devices is dominated by direct tunneling (DT) at low electric field ( $E < 0.4 \text{ MV/cm}$ ) and by Fowler-Nordheim (F-N) tunneling at high electric field ( $E > 0.4 \text{ MV/cm}$ ). The modified FTJ device stack (TiN/  $\text{Al}_2\text{O}_3$ / HZO/ TiN) demonstrated an enhanced TER ratio of  $\sim 5$  (2.2X improvement) and endurance up to  $10^6$  switching cycles. Write voltage and pulse width dependent trade-off characteristics between TER ratio and maximum endurance cycles ( $N_c$ ) was established which enabled optimal balance of FTJ switching metrics. The FTJ memory cells also showed multi-level-cell (MLC) characteristics i.e. 2 bits/ cell storage capability. Based on full 300 mm wafer statistics, switching yield of  $>80\%$  was achieved for fabricated FTJ devices demonstrating robustness of fabrication and programming approach used for FTJ performance optimization. The realization of CMOS-compatible nanoscale FTJ devices on 300mm wafer platform demonstrates promising potential of high-volume large scale industrial implementation of FTJ devices for various non-volatile memory (NVM) applications.

## I. INTRODUCTION

Since CMOS technology reaching its fundamental scaling limits, some emerging non-volatile memory (NVM) concepts have made significant progress in recent years<sup>1-5</sup>. In contrast to volatile memories, which require constant power to retain its state; NVM devices allow for data retention when not powered<sup>6</sup>. Modern day technology imposes different requirements on memory devices e.g., high density data storage, low cost, fast read and write speeds, long data retention, low power consumption<sup>7,8</sup> etc. Various novel concepts, architectures, materials, operation principles are being explored in NVM technology to fulfill these requirements. One such promising non-volatile memory technology is the ferroelectric tunnel junction (FTJ). An FTJ is a two terminal non-volatile memory device with two metal electrodes sandwiching a thin ferroelectric layer allowing quantum mechanical tunneling through it<sup>9</sup>. The switchable polarization of the ferroelectric layer enables significant change in tunneling resistance of FTJ devices<sup>10</sup>. Unlike FRAM, FTJ has a non-destructive read-out process since the tunneling current is sensed and the polarization state in ferroelectric switching layer is retained<sup>11</sup>. In addition, FTJ devices offer significant advantage with regard to superior scaling capability since scaling in these devices is not limited by stored amount of polarization charge<sup>12</sup>. One of the key challenges in manufacturing high performance FTJ device is the trade-off between remanent polarization and sizeable quantum mechanical tunneling current magnitude. The ferroelectric switching layer should be thin enough to achieve sufficient tunneling on current, however, magnitude of remanent polarization in these thin films is small impacting tunneling electroresistance ratio (TER) negatively and creates a major hindrance in reliable FTJ device design<sup>12</sup>. Other challenges like low TER ratio, stress induced leakage current based endurance/ lifetime limitation<sup>13</sup>, retention degradation due to depolarization field<sup>14</sup>,

remain on pathway to large scale commercial adoption of FTJ technology in semiconductor memory industry.

Some studies in past few years have tried to address some of these FTJ challenges. Goh et al. observed almost zero TER with symmetric TiN/HZO/TiN FTJ stack and demonstrated much improved TER ratio ( $> 6$ ) by changing the bottom electrode to Ge<sup>15</sup>. Ryu et al. showed that using p-Si as bottom electrode over metal based electrodes could significantly improve FTJ TER ratio and they demonstrated a TER ratio of  $\sim 5$  for Ti/Au/Al<sub>2</sub>O<sub>3</sub>/HZO/p-Si based FTJ structure<sup>13</sup>. Max et al. achieved excellent TER ratio ( $\sim 10$ ) for 12 nm thick HZO based FTJ, but  $> 4$  V of programming voltage was used to reliably switch those FTJ devices<sup>16</sup>, making them non-ideal for low power NVM applications. All these studies mentioned above, focused on development of large size i.e.,  $\mu\text{m}$  scale FTJ cells. At nanoscale, loss of reliable control of ferroelectric properties is one of the major challenges in nanoscale implementations of FTJ which severely limits its potential to be considered as industrially viable non-volatile memory<sup>12</sup>. Investigating switching performance, reliability, and a statistically significant large-scale development of high performance/yield nanoscale FTJ devices is still missing in current research. With that goal, in this work, hafnium zirconium oxide (HZO)-based  $100 \times 100 \text{ nm}^2$  FTJ devices were implemented on a 300 mm wafer platform, using SUNY Polytechnic Institute's 65 nm CMOS process technology. Key insights into nanoscale FTJ switching dynamics and reliability are presented based on optimization of HZO based stack fabrication and programming approaches. Multi-level-cell (MLC) behavior for improved storage density and full wafer scale key switching metrics for fabricated FTJ devices are investigated.

## II. DEVICE FABRICATION

FTJ devices (with TiN/HZO/TiN stack) were integrated in between metal (M1) and Via 1 (V1) layers in CMOS back end of the line (BEOL) process flow. Figure 1 shows a simplified process flow for FTJ device integration on 300 mm wafer platform. Fabrication of the FTJ device stack started with a TiN bottom electrode (BE) layer patterned using a subtractive integration scheme on top of M1 metallization layer, Figure 1b. The via insulator layer  $\text{Si}_3\text{N}_4$  was then patterned around BE layer, Figure 1c and 1d. On top of the bottom electrode, a conformal thin layer of 5 nm  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  switching layer was deposited via atomic layer deposition (ALD) at a deposition temperature of 250 °C followed by a 5 nm TiN layer, deposited via ALD, Figure 1e. A final 50 nm TiN top electrode layer (TE) was then deposited using physical vapor deposition (PVD), Figure 1e. Afterwards a post-deposition 60 seconds  $\text{N}_2$  anneal at 450 °C was done to drive the HZO into the ferroelectric phase.

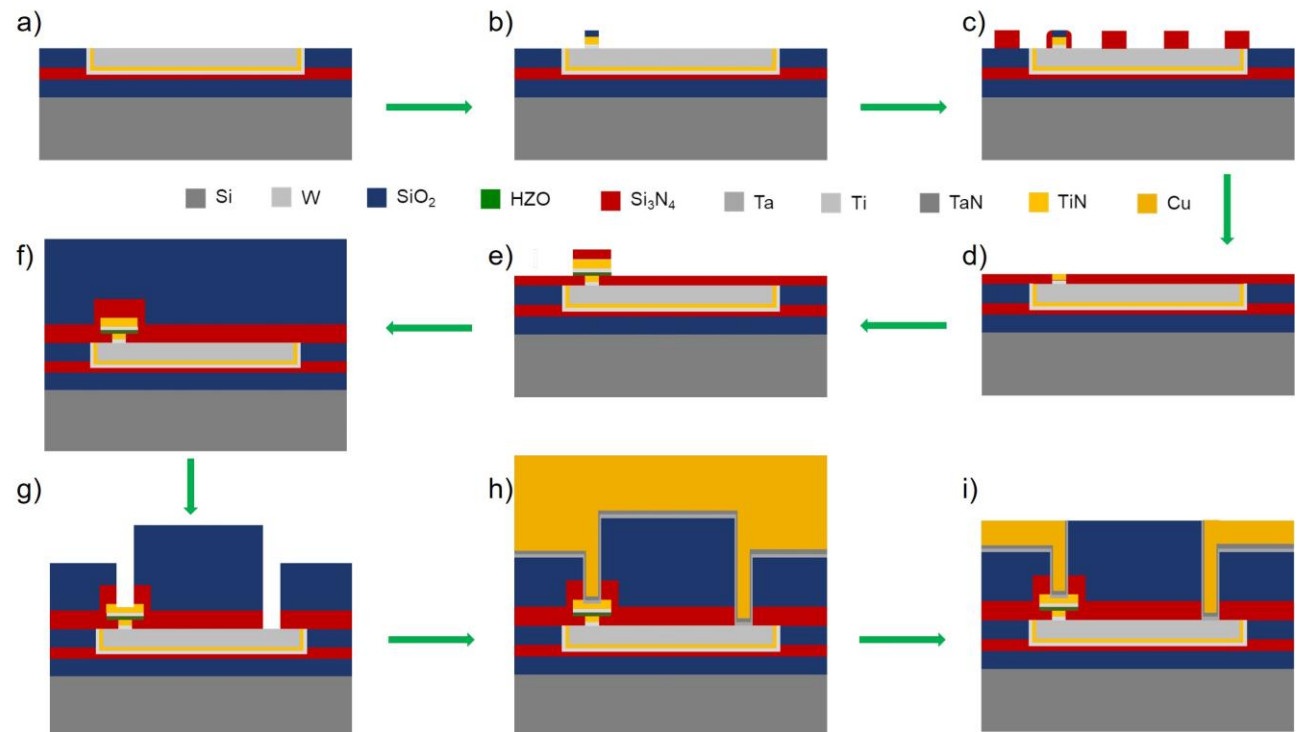


FIG. 1. Simplified process flow schematic for fabrication of HZO based 100 nm x 100 nm FTJ device development on 300 mm wafer platform.

The entire FTJ device stack was then lithographically patterned and etched using a custom-designed reactive ion etch (RIE) process. A  $\text{Si}_3\text{N}_4$  mask layer was deposited on top of TiN TE, Figure 1f, to protect the device top surface from subsequent V1/M2 patterning steps, Figure 1g. A standard state of the art dual-damascene Cu V1/M2 module and CMP, concludes the FTJ integration, Figure 1h and 1i. Cross-sectional transmission electron microscopy (TEM) imaging along with energy dispersive x-ray spectroscopy (EDS) analysis of the fabricated FTJ device stack confirmed the targeted thickness and composition of deposited films with low interface roughness (Figures 2a and 2b). The scaling of the BE is also observed at 100 nm with an overlay of the SL/TE.

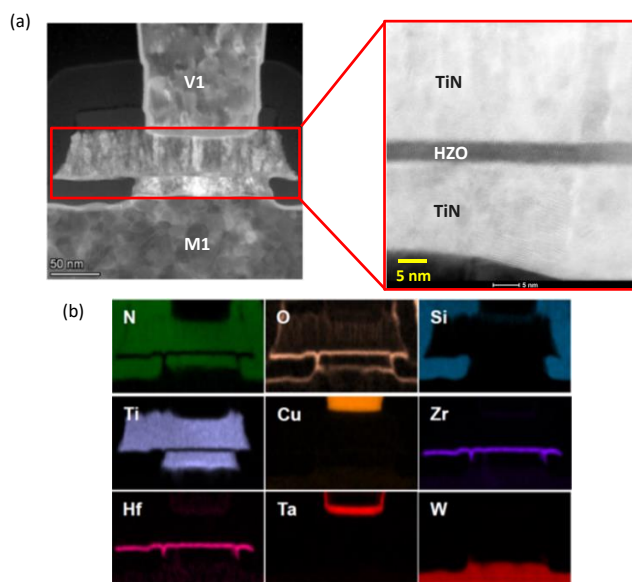


FIG. 2. a) TEM cross-sectional image of TiN/ HZO/ TiN FTJ stack integrated between M1 and V1 layers b) EDS compositional map showing various elements in FTJ stack. Hf and Zr are represented by purple and cyan, respectively.

### III. RESULTS AND DISCUSSION

Figure 3a shows electrical polarization hysteresis measurement of TiN/ Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub>/ TiN FTJ device stack. The device shows good ferroelectric response with extracted remanent polarization ( $P_r$ ) of  $\sim 15 \mu\text{C}/\text{cm}^2$  and coercive switching field of 2.25 MV/cm. The polarization hysteresis characteristics and remanent polarization were measured post 100 wake-up field cycles with 10 kHz frequency Positive-Up-Negative-Down (PUND) pulses. The observed ferroelectric behavior in HZO based FTJ devices is attributed to the presence of the non-centrosymmetric orthorhombic phase<sup>17</sup> as confirmed by grazing incidence X-ray diffraction measurements shown in Figure 3b. Other structural phases observed include monoclinic and tetragonal phase. The device was set in up or down polarization state with PUND positive or negative pulses, respectively with maximum pulse amplitude of 3.5 V. After programming the devices into a certain polarization state, an I-V sweep was performed. Figure 3c shows a typical I-V characteristics of a FTJ device. Observably, the maximum read voltage applied (0.75 V) was kept smaller than the coercive voltage ( $\sim 1$  V) to prevent change in programmed polarization state and corresponding switching state in FTJ device. The up-polarization state (programmed with positive pulses in PUND waveform) set the device in high conductance on- state, yielding an on-current density of  $0.08 \text{ A}/\text{cm}^2$  at a read voltage of 0.75 V. An off-current density of  $0.035 \text{ A}/\text{cm}^2$  was achieved due to down-polarization state (programmed with negative pulses in PUND waveform) of FTJ device, yielding a TER ratio of  $\sim 2.28$ . Figure 3d shows polarization endurance

measurements of the device upto  $10^3$  switching cycles in which the up and down remanent polarization states are programmed at write voltages of  $\pm 3.5$  V, respectively. The device

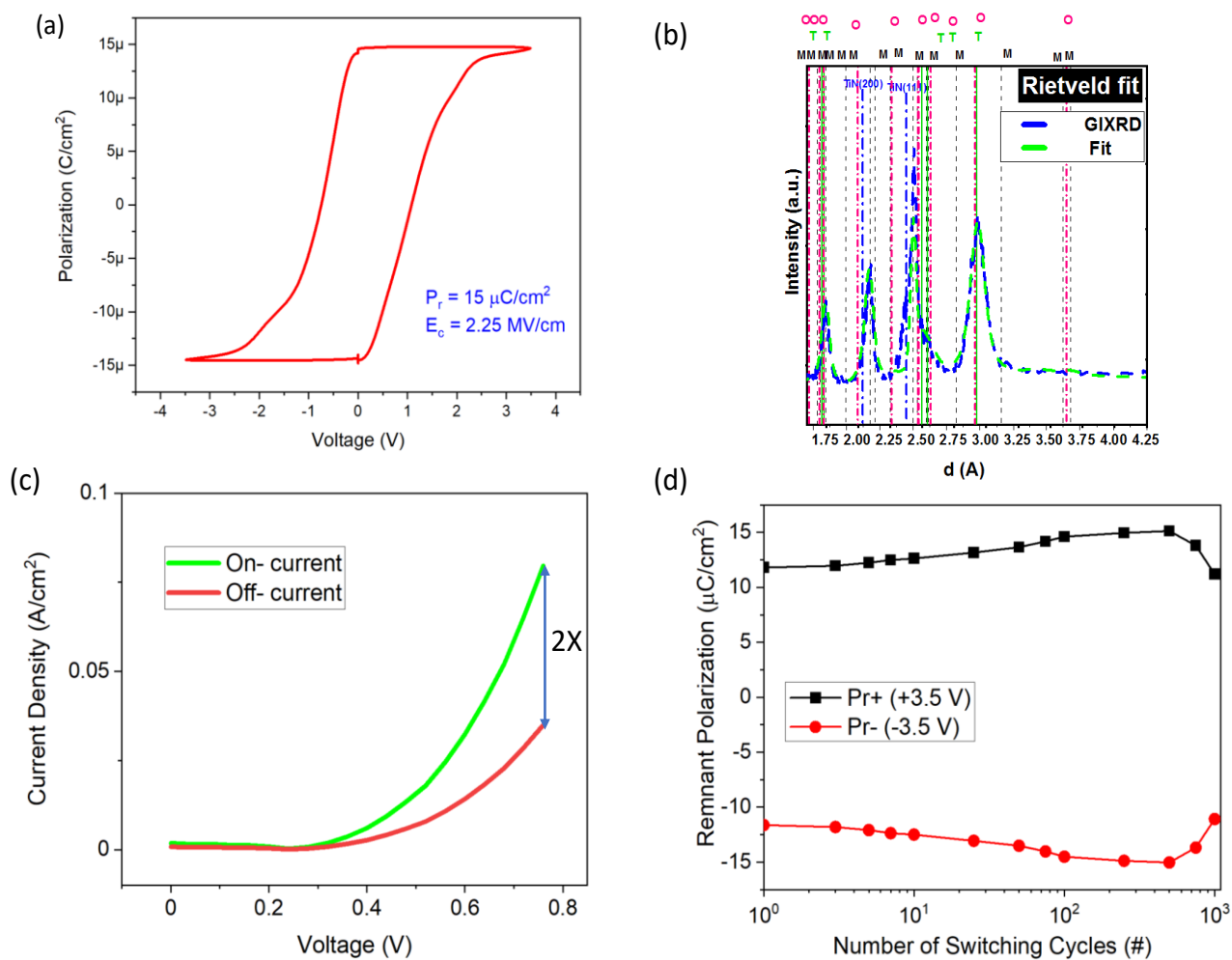


FIG. 3. TiN/ HZO/ TiN based FTJ performance: a) Polarization-Voltage (P-V) hysteresis b) grazing incidence XRD measurement results confirming presence of ferroelectric orthorhombic phase in HZO film. Reprinted with permission from Mukundan, Vineetha, et al., Applied Physics Letters 117, 262905 (2020), American Institute of Physics. c) current density-voltage curve for on and off-state of device; d) up and down remanent polarization with number of switching cycles at 3.5 V pulse amplitude.

exhibited a weak wake-up effect up to 500 switching cycles followed by polarization fatigue and eventual hard breakdown of devices.

The TER ratio for fabricated MIM TiN/ HZO/ TiN FTJ device was limited by off-state leakage current and not enough band tuning at HZO/TiN interface to facilitate high tunneling transmission coefficient<sup>18</sup>. To improve device performance, a modified FTJ stack was implemented in which we separated the ferroelectric switching layer and tunneling layer. A schematic of the modified FTJ stack is shown in Figure 4a, in which 2 nm thin Al<sub>2</sub>O<sub>3</sub> tunnel barrier layer was inserted between the bottom electrode TiN and ferroelectric switching layer HZO. Figure 4b shows the polarization hysteresis characteristics for the modified FTJ stack with Al<sub>2</sub>O<sub>3</sub> layer (black line) and a comparison with conventional FTJ stack without Al<sub>2</sub>O<sub>3</sub> layer (red line) is also shown. The thin Al<sub>2</sub>O<sub>3</sub> oxide layer results in an additional voltage drop across it, and hence, an increase in coercive voltage (~1.15 V) and a reduction in maximum achieved polarization (~12.5  $\mu\text{C}/\text{cm}^2$ ) can be observed for same pulse amplitude when compared with same for FTJ stack without Al<sub>2</sub>O<sub>3</sub> layer. An increase in coercive voltage also allows for an increase in read voltage which increases FTJ tunneling current.

The impact of the inserted tunnel barrier layer on FTJ performance can be better understood from the energy band diagram schematic in Figure 5a. With application of positive write pulse amplitude, the polarization in ferroelectric HZO layer is pointed towards Al<sub>2</sub>O<sub>3</sub> layer, i.e., up polarization state, resulting in downwards band bending in HZO. Subsequent positive read voltage also enables sufficient band bending in Al<sub>2</sub>O<sub>3</sub> layer creating a triangular potential profile which facilitates electron tunneling from bottom to

top electrode. Negative write pulse sets the device in down polarization state in which the polarization in ferroelectric layer is pointed towards the top electrode, and the upwards band tilt in HZO prevents large number of electrons to tunnel through the oxide layer. The  $\text{Al}_2\text{O}_3$  layer acts as an additional tunnel barrier layer in the off-state causing further reduction in tunnel transmission coefficient. Hence, significant tunneling conduction is expected for up-polarization state whereas, the down polarization state, programmed with negative write pulse should allow for a small tunneling current to flow in FTJ device. This impact of  $\text{Al}_2\text{O}_3$  tunnel layer is validated through measured current-voltage characteristics of FTJ device shown in Figure 5b where a significant increase ( $\sim 1.5$  times) in on current density and reduction in off-current density ( $\sim 1.45$  times) was observed when compared to conventional FTJ stack without  $\text{Al}_2\text{O}_3$  layer. At a read voltage of 0.75V, the up-polarization state in ferroelectric layer resulted in a device on current density of  $0.12 \text{ A/cm}^2$ . The corresponding off-current density due to down-polarization was extracted to be  $0.024 \text{ A/cm}^2$  yielding a TER ratio  $\sim 5$ . Hence, a 2.2X improvement in device TER ratio was achieved with  $\text{Al}_2\text{O}_3/\text{HZO}$  bilayer based FTJ structure.

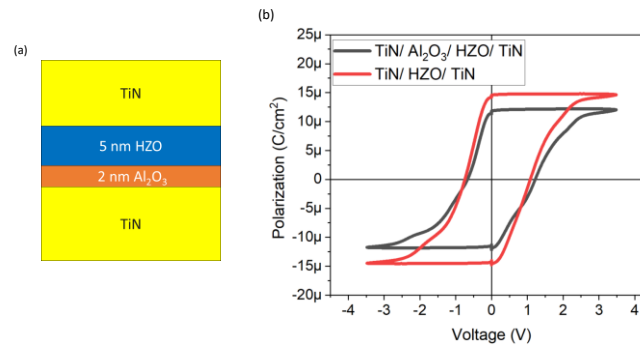


FIG. 4. a) Schematic of  $\text{TiN}/\text{Al}_2\text{O}_3/\text{HZO}/\text{TiN}$  based FTJ stack; b) Polarization-voltage (P-V) hysteresis loop for  $\text{Al}_2\text{O}_3$  based modified FTJ device and comparison with conventional  $\text{TiN}/\text{HZO}/\text{TiN}$  based FTJ structure.

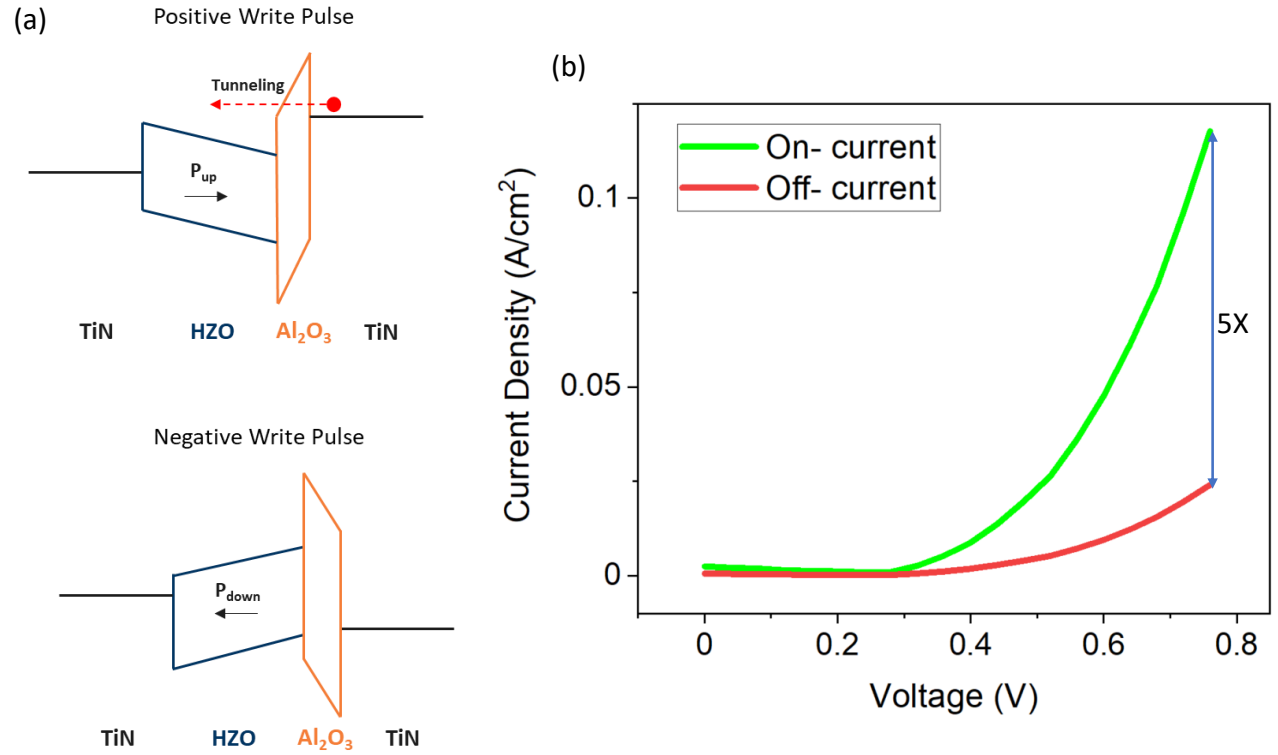


FIG. 5. a) Energy band diagram schematic of TiN/ Al<sub>2</sub>O<sub>3</sub>/ HZO/ TiN based FTJ device depicting how large tunneling current flows for up polarization state and current flow is inhibited for down polarization orientation; b) Current density (J)- voltage (V) characteristics for the FTJ device, an on/off ratio of ~5 is yielded at a read voltage of 0.75 V.

To demonstrate that the improvement in on-current density is due to enhancement in tunneling current, we investigated the conduction mechanism in TiN/ Al<sub>2</sub>O<sub>3</sub>/ HZO/ TiN FTJ device, shown in Figure 6. We observed that for low applied field ( $E < 0.4$  MV/cm), the plot of  $\ln(J/E^2)$  shows logarithmic variation with  $1/E$  (Figure 6a), which indicates that the device exhibits direct tunneling conduction. When the applied electric field exceeds a critical field, a transition from direct tunneling to Fowler-Nordheim (F-N) tunneling regime

occurs as shown in Figure 6b. This transition field was extracted to be  $\sim 0.4$  MV/cm beyond which  $\ln(J/E^2)$  decreases linearly with  $1/E$ , an indication of device operation switching in F-N tunneling conduction regime. The relationship between  $\ln(J/E^2)$  and  $1/E$  governing both tunnel conduction processes can be understood from following set of Eqs. (1)-(4)<sup>19</sup>:

Direct tunneling regime ( $E < 0.4$  MV/cm):

$$J \propto \frac{E^2}{E} e^{\left(-\frac{4\pi d \sqrt{2m^* \phi_B}}{h}\right)} \quad (1)$$

$$\ln\left(\frac{J}{E^2}\right) \propto \ln\left(\frac{1}{E}\right) \quad (2)$$

Fowler-Nordheim tunneling regime ( $E > 0.4$  MV/cm):

$$J \propto E^2 e^{\left(-\frac{8\pi \sqrt{2qm^* \phi_B^3}}{3hE}\right)} \quad (3)$$

$$\ln\left(\frac{J}{E^2}\right) \propto -\left(\frac{1}{E}\right) \quad (4)$$

Where  $J$  is the current density,  $E$  is applied electric field,  $m^*$  is the effective mass of electrons, and  $\phi_B$  is the junction barrier height. The schematic energy band diagrams for both direct and F-N tunneling conduction are illustrated in Figures 6c and 6d, respectively. Direct tunneling shows a linear relationship with applied field  $E$  and exponential dependence with insulator thickness  $d$  as shown in Eq. (1). Hence, this tunneling mechanism is dominant at thinner oxide films at low voltage<sup>20</sup>. On the other hand, F-N tunneling occurs when applied electric field is large enough to cause electron wave functions to tunnel through the triangular potential barrier profile in the insulator layer<sup>21</sup>, as shown in the Figure 6d energy band diagram. This is consistent with fabricated FTJ

current-voltage conduction mechanism characteristics shown in Figure 6b, in which FTJ devices exhibited F-N tunneling for  $E > 0.4$  MV/cm.  $R^2$  values of 0.995 and 0.998

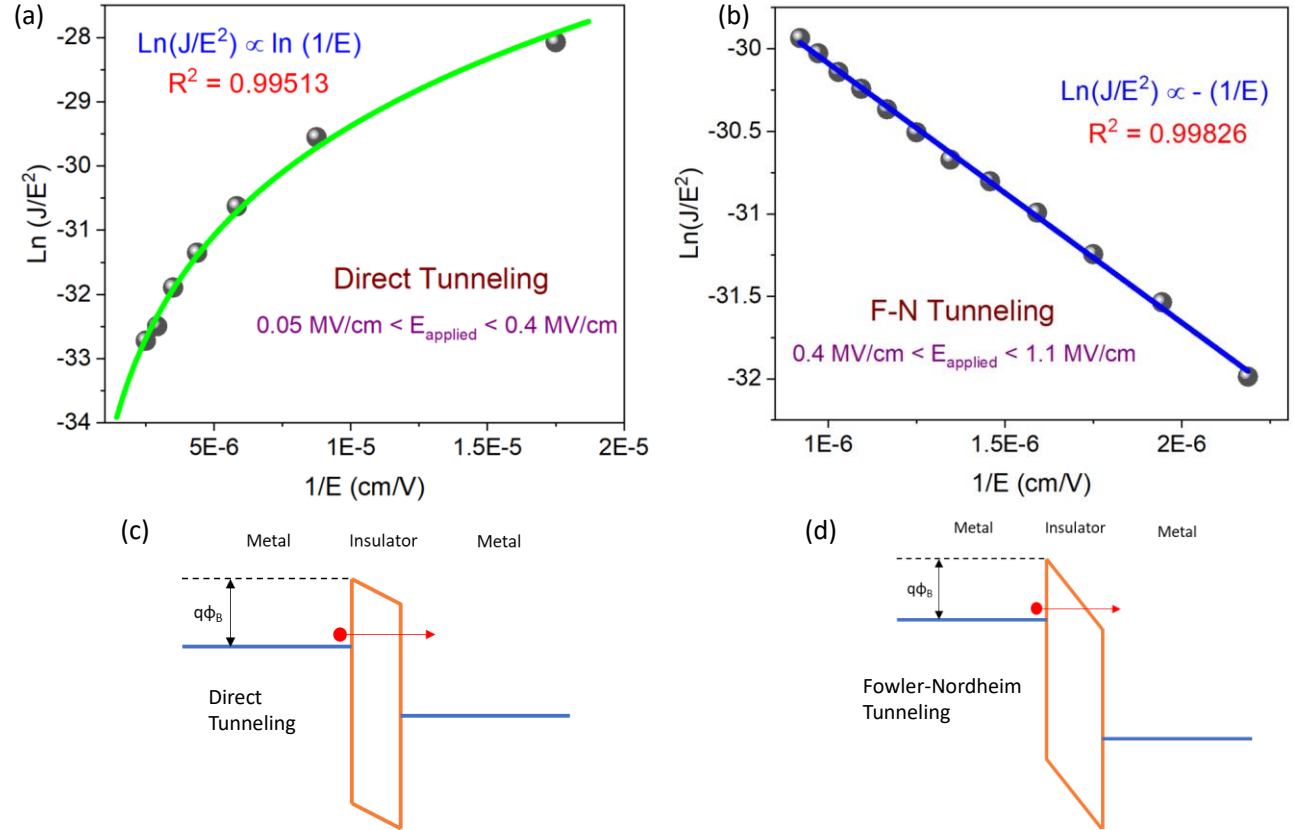


FIG. 6.  $\text{Al}_2\text{O}_3/\text{HZO}$  bilayer based FTJ device conduction mechanism analysis:  $\ln(J/E^2)$  vs  $1/E$  plot showing a) direct tunneling phenomenon for  $0.05 \text{ MV/cm} < E < 0.4 \text{ MV/cm}$  regime; b) Fowler-Nordheim tunneling for  $0.4 \text{ MV/cm} < E < 1.1 \text{ MV/cm}$  applied electric filed regime. Energy band diagram schematic depicting c) direct tunneling and d) Fowler-Nordheim tunneling process.

excellent goodness of fit for direct tunneling and F-N tunneling processes, respectively. The discussed conduction mechanism analysis validates that dominant on state current transport mechanisms for fabricated  $\text{TiN}/\text{Al}_2\text{O}_3/\text{HZO}/\text{TiN}$  FTJ devices are tunneling

conductions, i.e., direct tunneling at low electric field and F-N tunneling at high electric field.

Endurance and retention characteristics of these  $\text{Al}_2\text{O}_3/\text{HZO}$  based FTJ devices were studied to qualify reliability of our devices. Figure 7a shows the remanent polarization in ferroelectric film with number of switching cycles. The ferroelectric HZO film showed a significant wake-up effect up to  $\sim 5 \times 10^4$  switching cycles yielding a maximum remanent polarization value of  $\sim 13 \mu\text{C}/\text{cm}^2$  at 3.75 V pulse amplitude and 10 kHz pulse frequency. The observed wake-up effect with the  $\text{Al}_2\text{O}_3$  layer FTJ device is most likely due to homogeneous distribution of defects with continuous cycling in ferroelectric layer resulting in an increase in number of switchable domains & consequently, remanent polarization value<sup>22</sup>. With more field cycling, the devices showed fatigue behavior in which remanent polarization decreases with switching cycle, shown in Figure 7a. The polarization fatigue in the ferroelectric film could be attributed to eventual pinning of switching domains by generated defects in ferroelectric layer with continuous field cycling<sup>22,23</sup>. The FTJ current density evolution with endurance cycles was analyzed for both MIM stacks (with and without  $\text{Al}_2\text{O}_3$  layer), shown in Figure 7b. The bilayer FTJ stack showed significant improvement in device endurance behavior, with maximum endurance limit extending up to  $10^6$  switching cycles. The  $\text{Al}_2\text{O}_3$  layer facilitates tunneling for up polarization state and acts as a barrier layer in down polarization state, as explained in energy band diagram schematic in Figure 5a. Hence, an increase in on state current density and decrease in off state current density were observed with bilayer FTJ stack, denoted by black and red lines in Figure 7b, respectively. Increase in both on and off state current density with endurance

cycles is most likely due to overall increase in device leakage current originating from defects/trap states generation in ferroelectric layer<sup>13</sup>. In FTJ retention measurement, shown

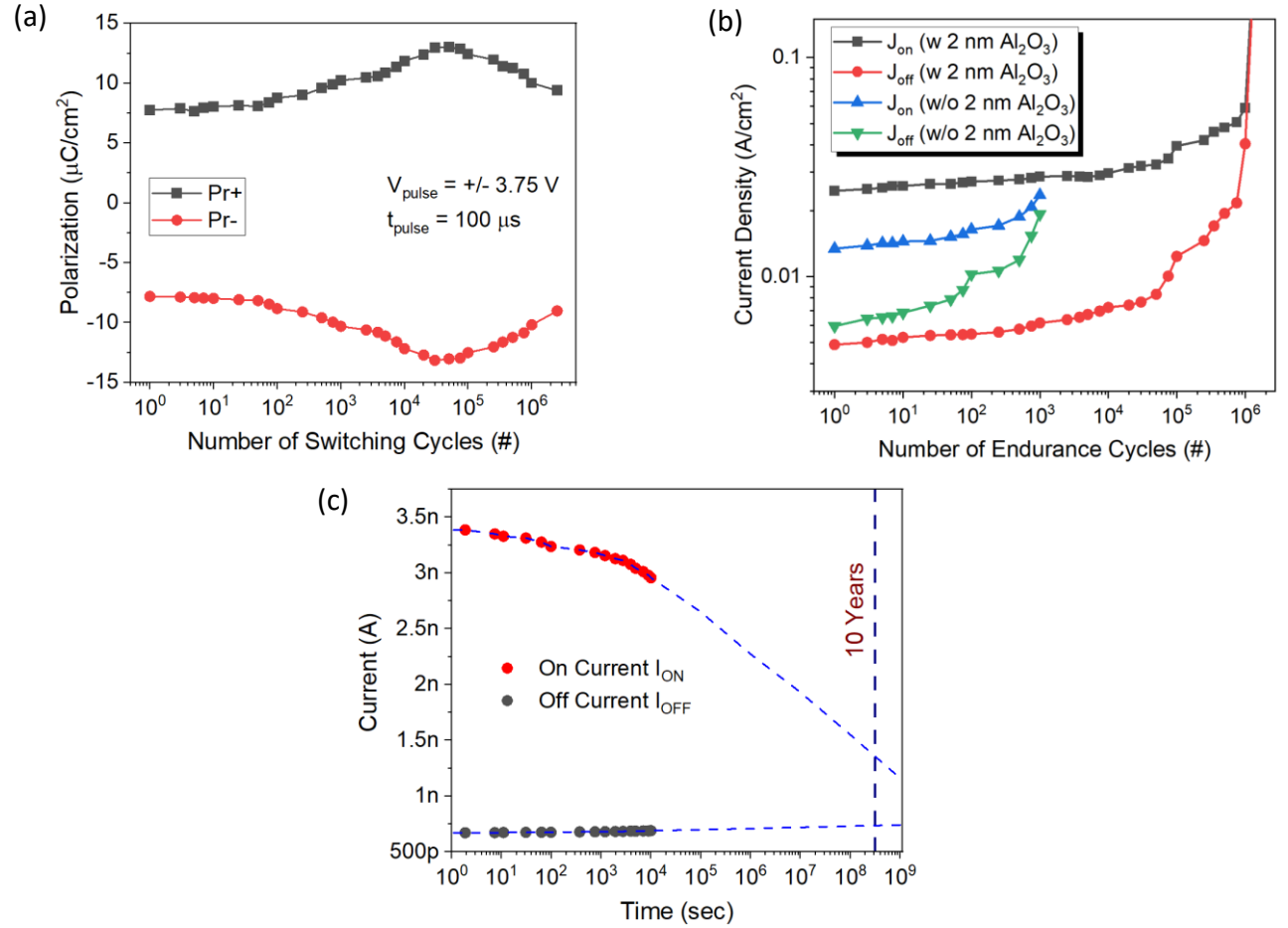


FIG. 7. a) Up and down remanent polarization with switching cycles at pulse amplitude of 3.75 V and frequency of 10 kHz b) Current density evolution comparison with endurance cycles for bilayer  $\text{Al}_2\text{O}_3/\text{HZO}$  based FTJ stack with single layer HZO based FTJ device c) Retention characteristics at room temperature for  $\text{Al}_2\text{O}_3/\text{HZO}$  based FTJ memory device.

in Figure 7c, a gradual drift in on-current was observed resulting in reduction of TER ratio with time. A residual TER ratio of  $\sim 2.1$  was extracted after extrapolation to 10 years in data

retention characteristics. The drift in current values could be attributed to depolarization field caused by incomplete charge compensation at  $\text{Al}_2\text{O}_3/\text{HZO}$  interface<sup>24</sup>.

In order to optimize FTJ devices with respect to both TER ratio and maximum endurance cycles ( $N_c$ ), we investigated their dependence on write pulse width and amplitude. Figure 8a shows FTJ TER ratio with pulse width (100 ns – 10 ms) for a wide range of write pulse amplitude (1 V – 4 V) values. An increase in write voltage amplitude/ pulse width enhances ferroelectric polarization in HZO layer resulting in an increase in TER ratio. The slope of TER increase reduces at higher write voltage amplitude/ pulse width (3V/100  $\mu\text{s}$ ) due to increase in off-state leakage current density. When the device was stressed at 4V amplitude with 1 ms pulse width, the large magnitude of leakage current through the device causes hard breakdown in oxide layer diminishing TER effect in ferroelectric tunnel junctions. Unlike TER, maximum endurance cycles  $N_c$  shows an inverse relationship with write pulse amplitude/time (Figure 8b). High voltage/time stress induces generation of interface and bulk defects in the dielectric increasing overall leakage current and consequently limiting FTJ endurance performance<sup>16</sup>. Maximum  $N_c$  of  $\sim 3 \times 10^6$  was observed for lowest applied write amplitude (2 V) and pulse width (100 ns) at the cost of low TER ratio. Hence, a clear trade-off between TER ratio and endurance limit could be observed in fabricated bilayer FTJ devices, enforcing the need of suitable programming parameters for optimal device

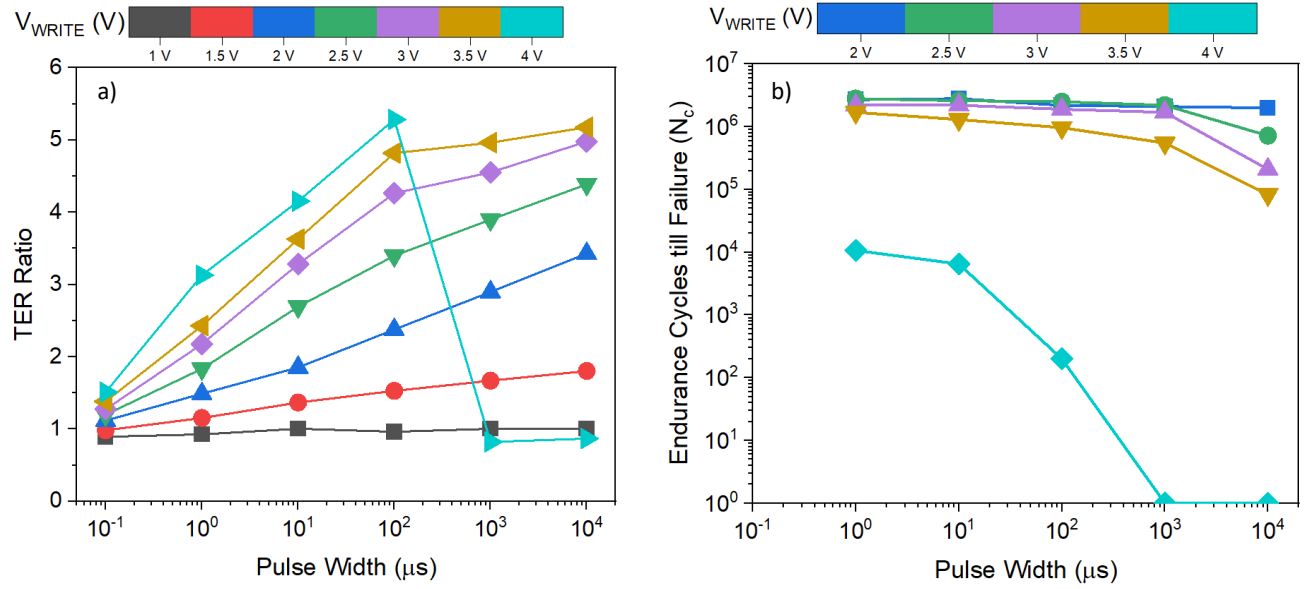


FIG. 8. a) Tunnel electroresistance (TER) ratio and b) maximum endurance cycles  $N_c$  with write pulse width for different write pulse amplitudes.

performance.

To improve storage density of ferroelectric tunnel junction memory, the FTJ devices were also investigated for multi-level-cell (MLC) functionality. The observed phenomena of increase in remanent polarization in ferroelectric layer and consequent increase in FTJ tunneling current with  $V_{\text{WRITE}}$  amplitude, was used to demonstrate MLC behavior in fabricated FTJ cells. Five different on-current levels were achieved through write voltage amplitude modulation from 1.5 V to 3.75 V, shown in Figure 9a. Figure 9b shows cumulative distribution of on current density values measured for different  $V_{\text{WRITE}}$  amplitudes. The MLC behavior in FTJ devices can be elucidated using a simplified model<sup>25</sup> in which total current density is made up of two different current components: contribution from up polarization ferroelectric domains and contribution from down polarization ferroelectric domains, represented by Eq. (5):

$$J_{Total} = S \cdot J_{up} + (1 - S) \cdot J_{down} \quad (5)$$

where  $S$  is fraction of ferroelectric domains switched with up polarization state. With increase in  $V_{WRITE}$ , the  $S$  value increases as more fraction of ferroelectric domains can be switched with up orientation and hence, increases total on current density. With intermediate write voltage amplitudes, multiple  $S$  values can be obtained, and consequently multiple on-current levels can be achieved. It can be observed from Figures 9a and 9b that the cycle-to-cycle variation in on current density is higher at lower  $V_{WRITE}$  amplitudes causing an overlap between on-current levels for  $V_{WRITE}$  of 1.5 V and 2 V. This is quantified in Figure 9c, where we plotted mean and relative spread ( $\sigma_J/J$ ) in on-current density values with different write voltage amplitudes. The mean on-current  $\mu_J$  decreases from 0.095 to 0.015 A/cm<sup>2</sup> (> 6X reduction) and relative cycle-to-cycle spread  $\sigma_J/J$  value increases from 0.03 to 0.3 (10X increase) when  $V_{WRITE}$  was decreased from 3.75 V to 1.5 V. The larger on-current variation at lower write voltage values could also be explained by understanding switching kinetics of ferroelectric domains. When  $V_{WRITE}$  is closer to coercive voltage, the polarization state switching of domains in ferroelectric films is known to be a stochastic and non-deterministic process<sup>26</sup>, in which some ferroelectric domains can switch with up orientation while other domains remain in down polarization state, hence introduces cycle-to-cycle stochasticity in FTJ metrics. This switching variation gets

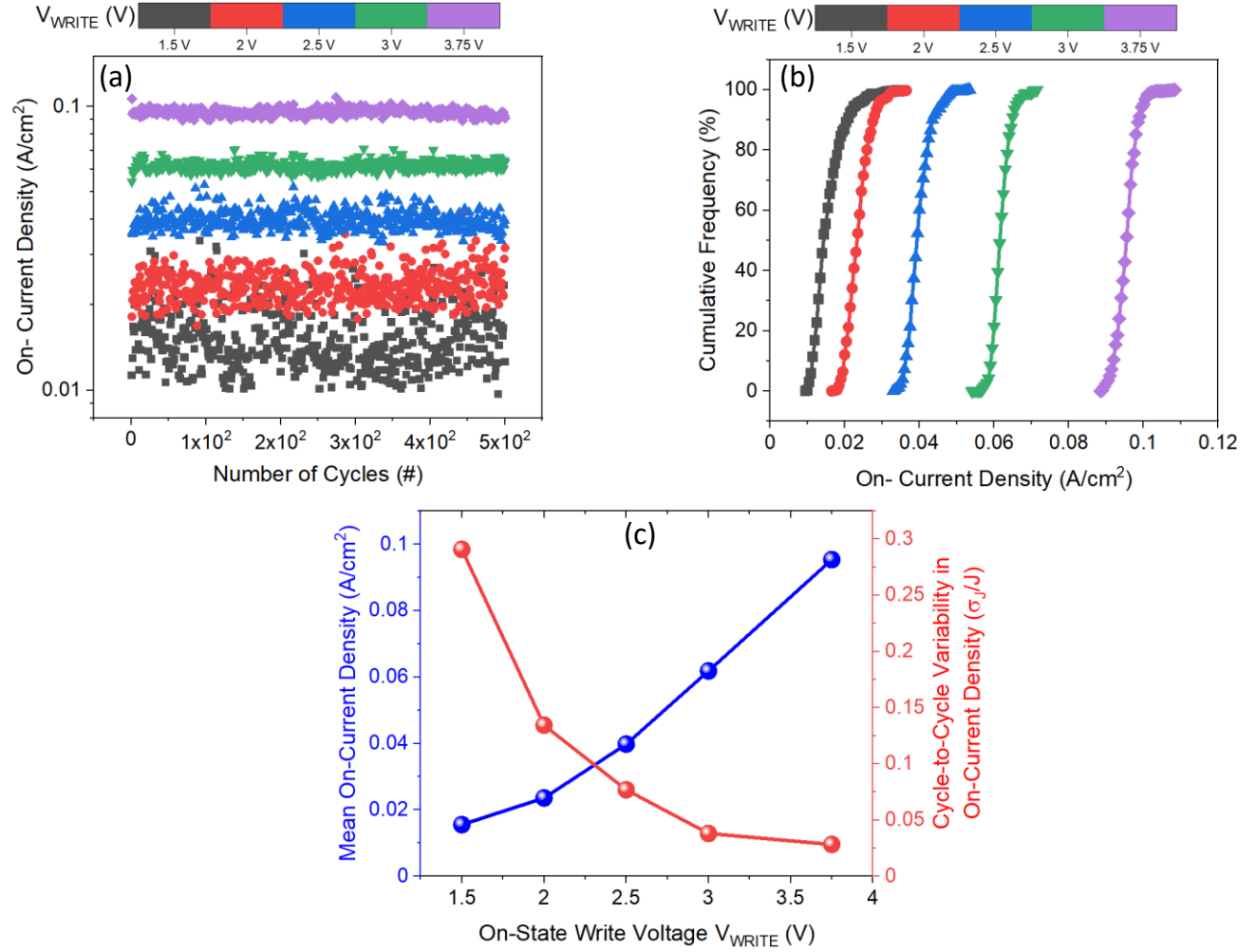


FIG. 9. Multi-level-cell functionality of fabricated FTJ devices: a) on current density with number of cycles for various write pulse amplitudes showing 5 distinct current levels b) corresponding cumulative distribution plots for on currents c) extracted mean and cycle-to-cycle variation in on current for those 5 distinct levels.

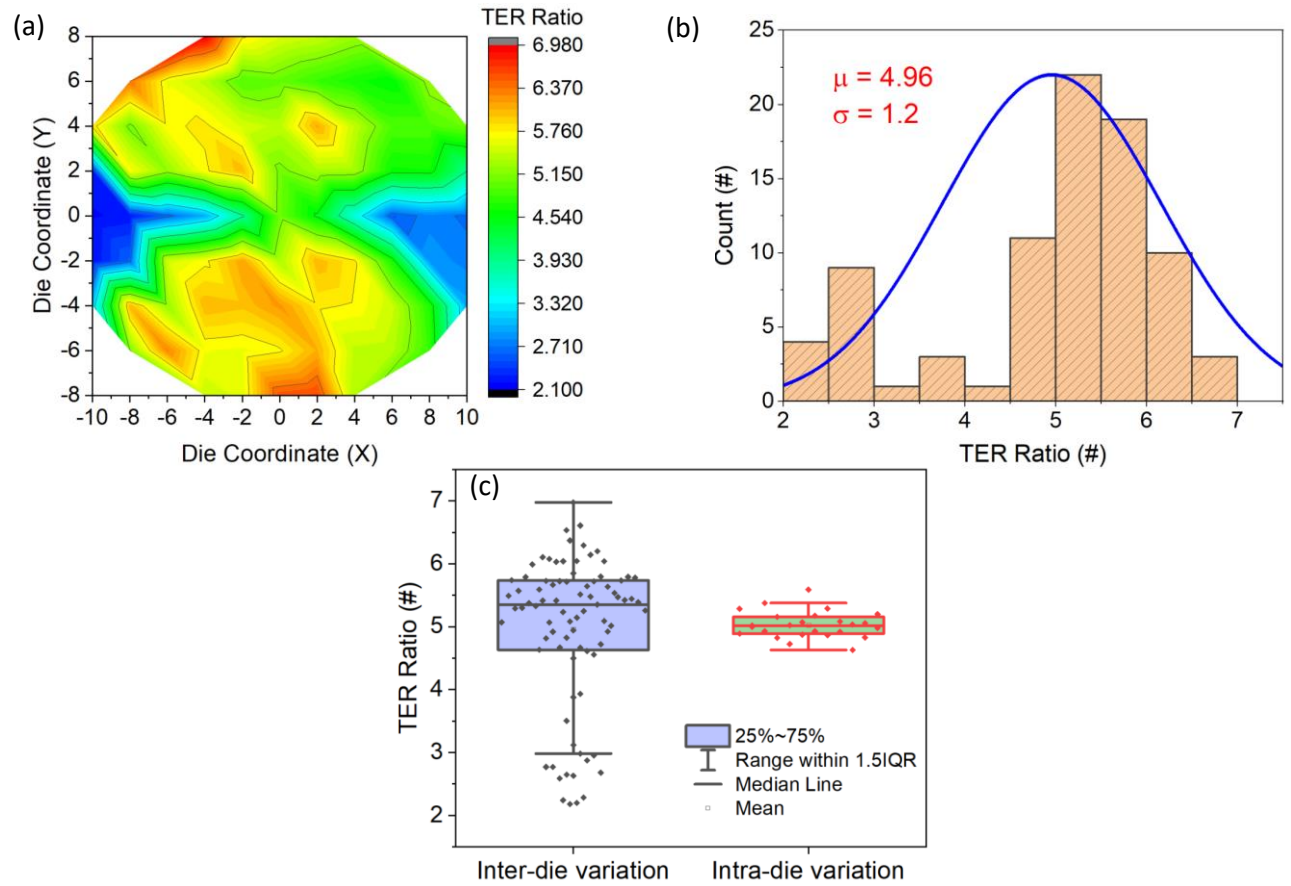


FIG. 10. Full 300 mm wafer scale statistics for total 415 tested FTJ devices: a) wafer map for FTJ TER ratio; b) corresponding normal distribution plot for TER ratio with mean and sigma values of 4.96 and 1.2, respectively; c) Intra-die and inter-die variations in FTJ TER ratio. The raw data is represented by dots around the boxes and the median and box plot is represented.

significantly reduced at higher pulse amplitudes when most of the ferroelectric domains have already switched into up polarization state.

For a comprehensive statistical analysis of device performance, we measured a total of 415 FTJ devices distributed across full 300 mm wafer and the wafer map for TER ratio

is plotted in Figure 10a. Excluding the edge regions where the TER is lowered by higher leakage current, FTJ devices showed an impressive 4.5 -6 TER ratio on center and

TABLE I. Performance metrics statistics of fabricated HZO based FTJ devices distributed across full wafer and center region ((-4, -4) to (4, 4) die coordinates).

| FTJ Performance Metric               | Center Region | Full Wafer |
|--------------------------------------|---------------|------------|
| TER Ratio                            | 5.38          | 4.96       |
| Switching Yield                      | 80.8%         | 76.2%      |
| Cycle-to-Cycle $\sigma_{\text{TER}}$ | 0.253         | 0.312      |
| Cell-to-Cell $\sigma_{\text{TER}}$   | 0.83          | 1.2        |

surrounding regions of the wafer. A full wafer distribution curve is shown in Figure 10b. The full wafer mean and standard deviation of measured TER ratios for 415 FTJ devices were found to be 4.96 and 1.2, respectively. We also investigated intra-die and inter-die variations in FTJ switching, plotted in Figure 10c. The raw data points for the box plots are shown by black and red dots. The intra-die variation is found to be much higher as compared to inter-die variation likely due to variation in HZO/  $\text{Al}_2\text{O}_3$  interface properties which significantly impacts the device TER ratio.

Table 1 tabulates statistics for FTJ performance metrics analyzed for center region and full wafer devices. The full wafer and center region analysis is carried over 415 and 125 FTJ devices, respectively. The TER ratio increases from full wafer mean value 4.96 to

5.38 for center region devices. We also demonstrate an impressive switching yield of >80% based on characterization of FTJ devices on center region of the wafer. The switching yield is defined by FTJ cells exhibiting a TER ratio  $> 2$ . In addition, the variability in FTJ switching was also investigated across full wafer. We report low cycle-to-cycle (0.25) and cell-to-cell variability (0.83) in FTJ TER ratio for center region devices. Expectedly, the TER variability increased in full wafer statistics when relatively higher leakage edge region devices were included in the statistics. Further studies are planned to explore the thickness and characteristics of the ferroelectric film and tunneling barrier, to optimize the TER, reduce variability, and achieve high endurance.

#### IV. SUMMARY AND CONCLUSIONS

We successfully implemented CMOS compatible Zr doped  $\text{HfO}_2$  based nanoscale (100 nm x 100 nm) ferroelectric tunnel junction devices on 300 mm wafer platform. We demonstrated that separating ferroelectric layer HZO and tunneling layer  $\text{Al}_2\text{O}_3$  could significantly improve FTJ performance over conventional TiN /HZO/ TiN based FTJ structure. The modified FTJ device stack (TiN/  $\text{Al}_2\text{O}_3$ / HZO/ TiN) demonstrated an excellent TER ratio of  $\sim 5$  and endurance up to  $10^6$  switching cycles. Investigation of current transport mechanism showed that the current in these FTJ devices is dominated by direct tunneling (DT) at low electric field ( $E < 0.4$  MV/cm) and by Fowler-Nordheim (F-N) tunneling at high electric field ( $E > 0.4$  MV/cm). Further improvement of TER and endurance will require enhancing the asymmetry of the tunneling barrier created for the two polarization orientations and optimization of film thickness for the ferroelectric and tunneling layers. Write voltage amplitude modulation based MLC operation yielded 4

distinct current levels resulting in improved storage density of FTJ devices. The FTJ devices were optimized with respect to write voltage amplitude and pulse width and low cycle-to-cycle & cell-to-cell variability along with impressive switching yield (~80%) were accomplished across full 300 mm wafer. The development of high performance and high yield CMOS-compatible nanoscale FTJ devices on 300mm wafer platform demonstrates promising potential of commercially viable industrial adoption of FTJ devices for various NVM based data storage and other embedded memory applications.

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## AUTHOR DECLARATIONS

### Conflicts of Interest

The authors have no conflicts to disclose.

## DATA AVAILABILITY

Data from this manuscript is available by request from the corresponding author (Nathaniel Cady).

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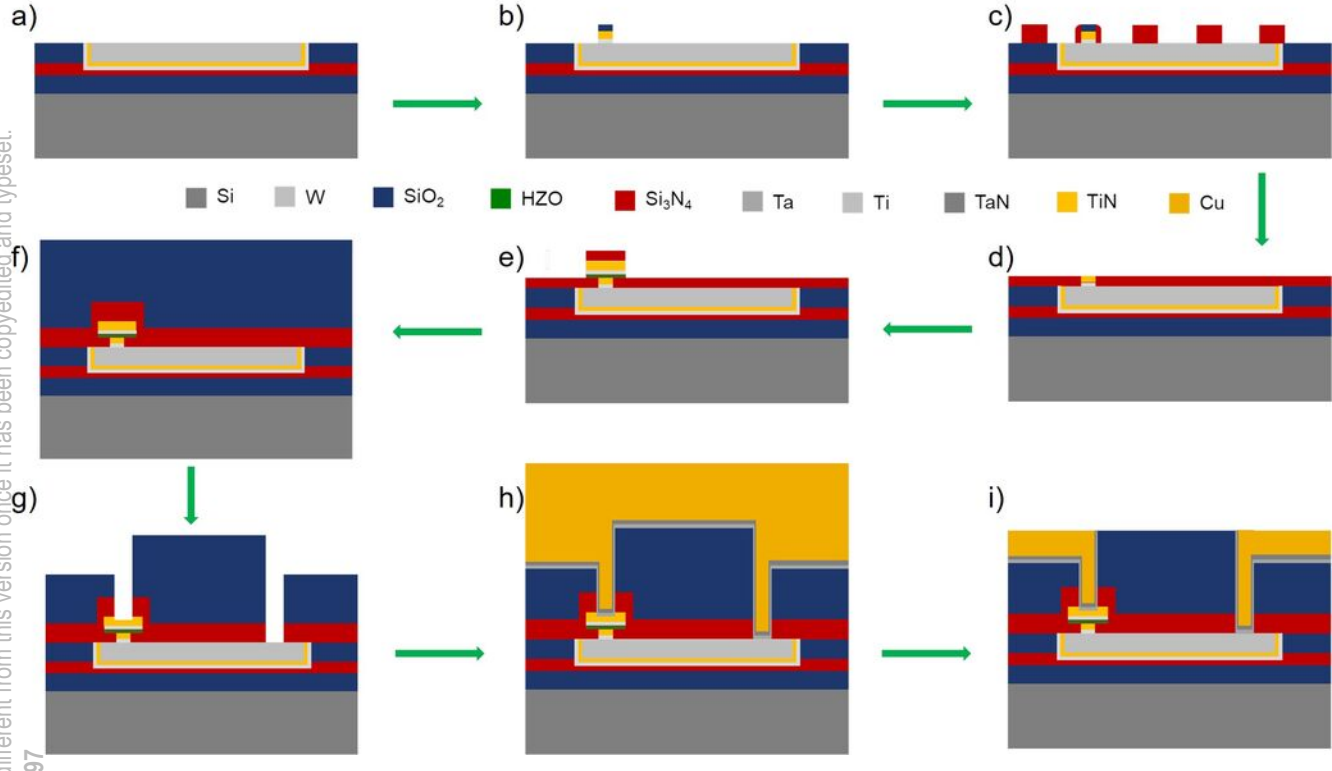
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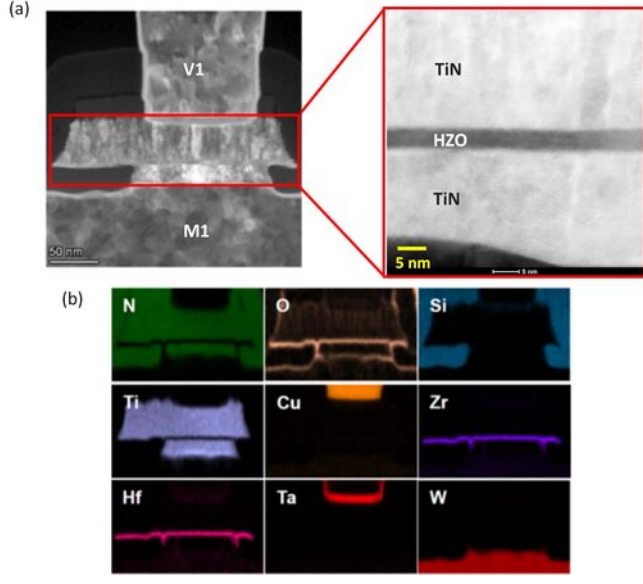
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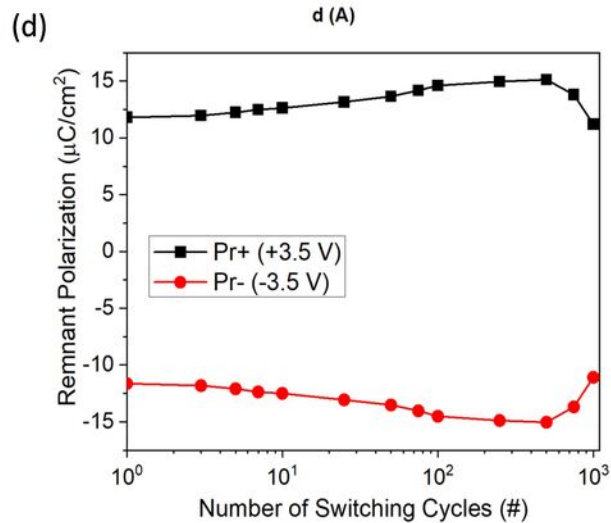
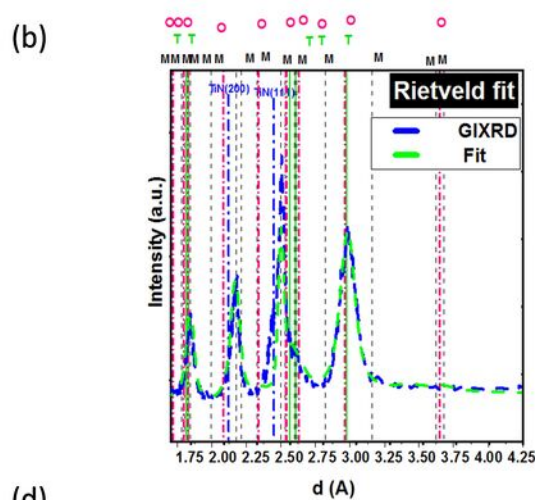
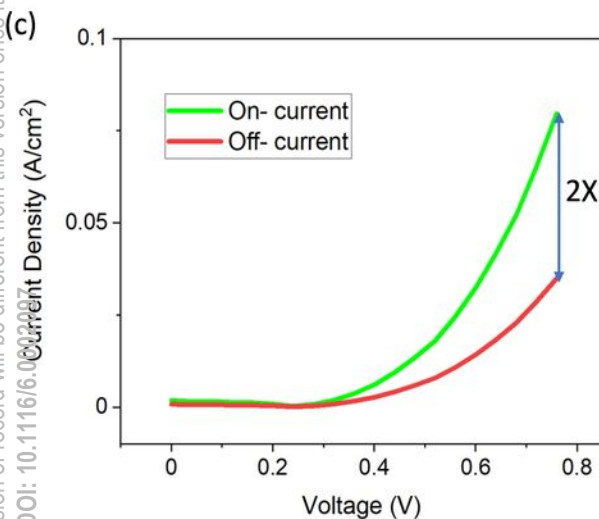
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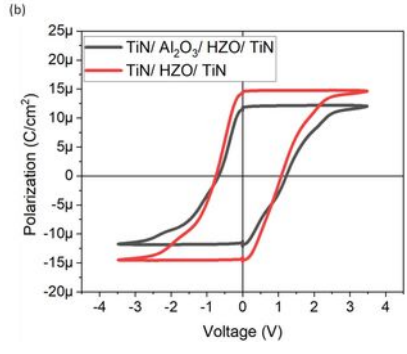
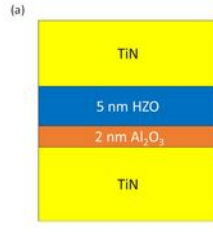


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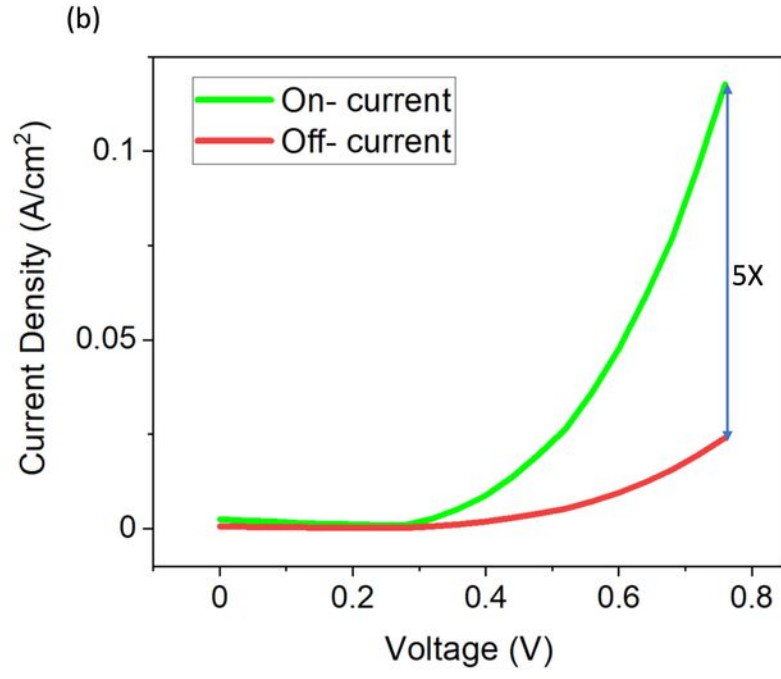
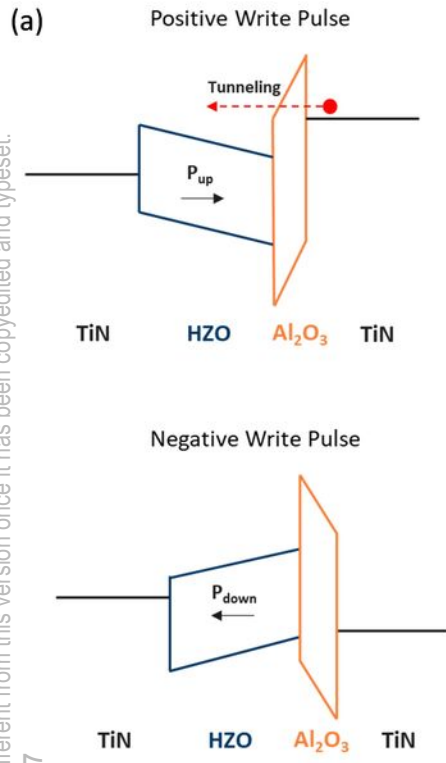


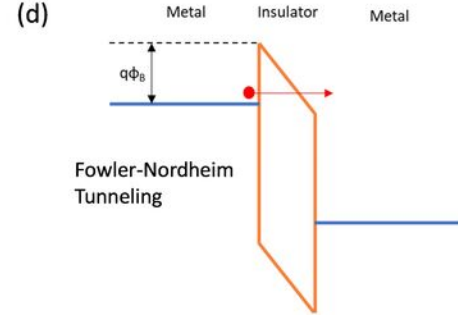
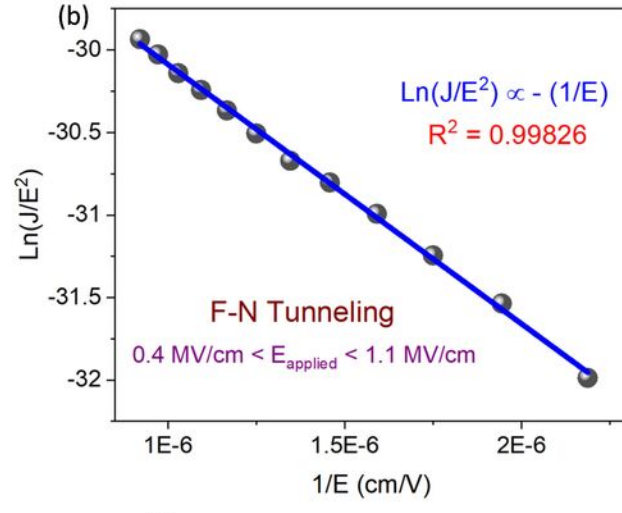
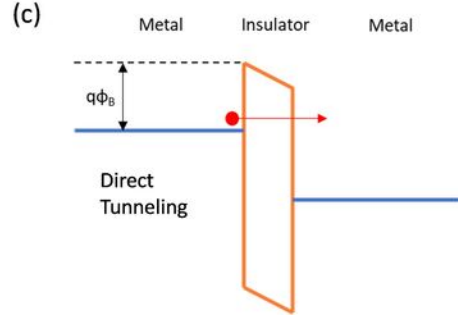
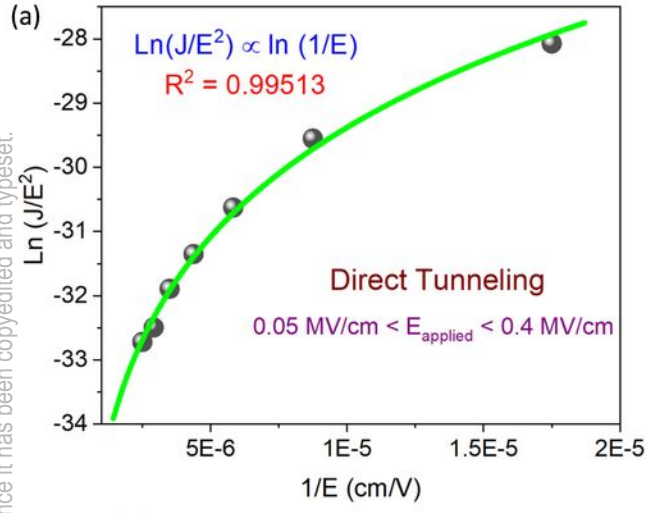


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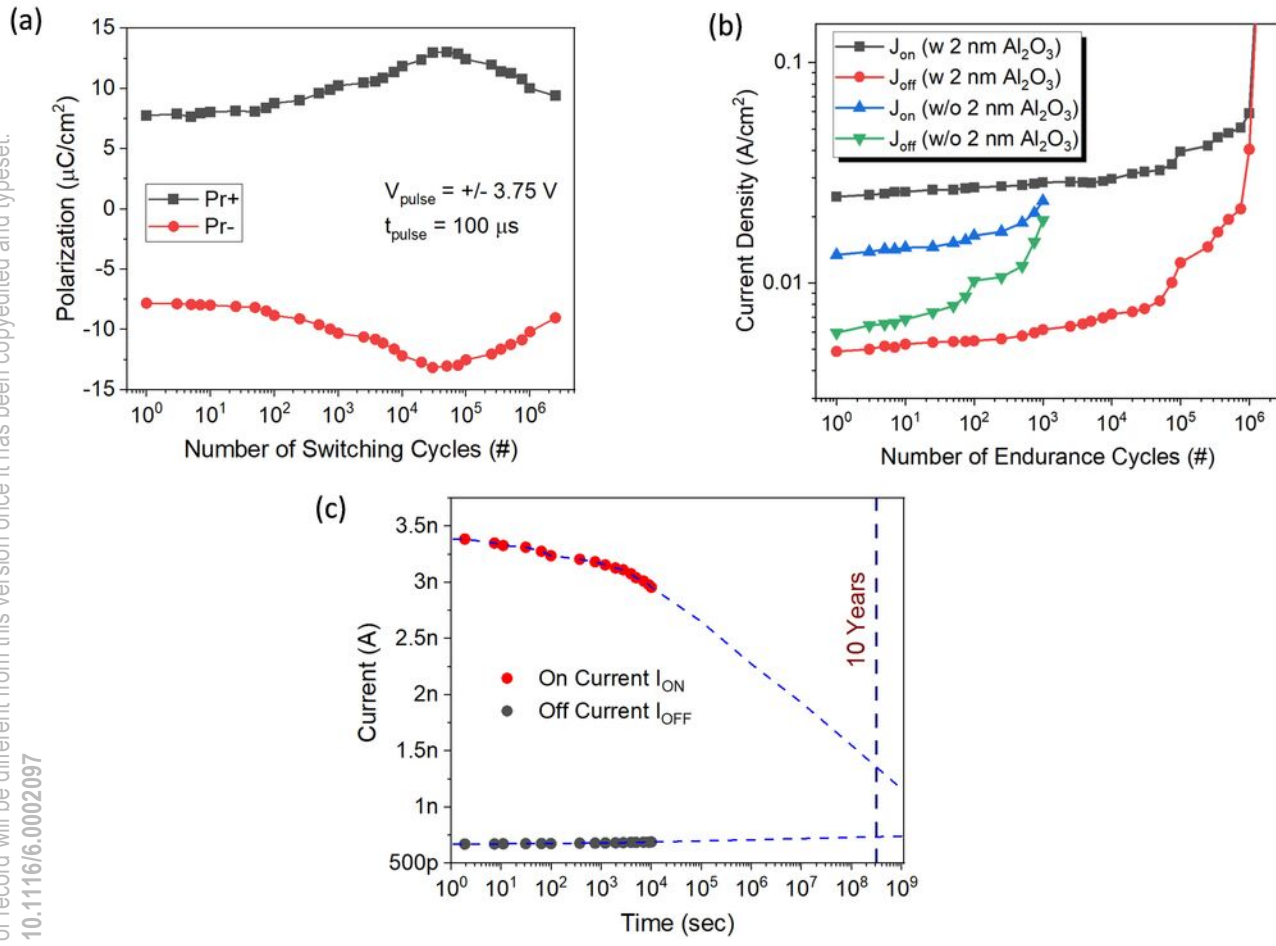


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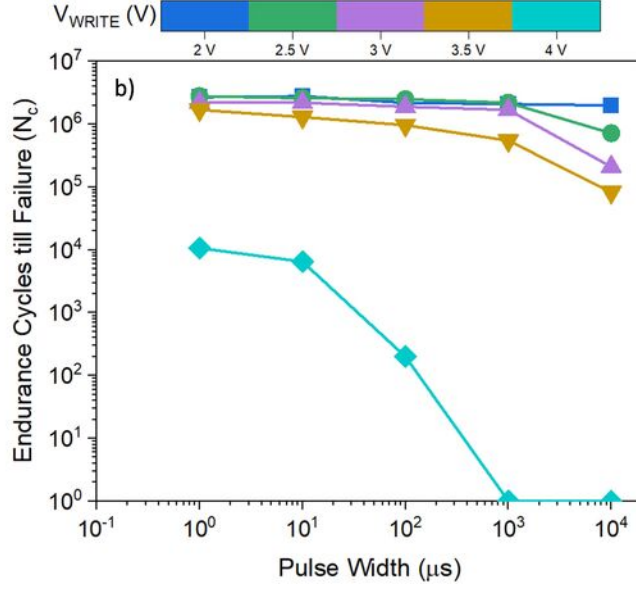
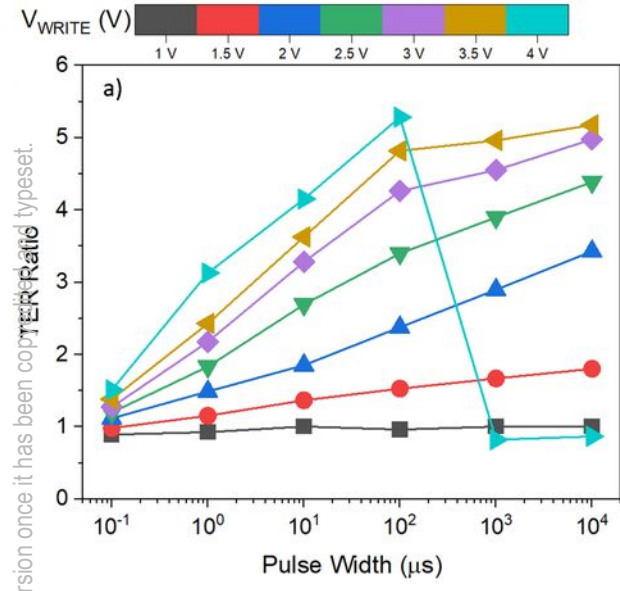


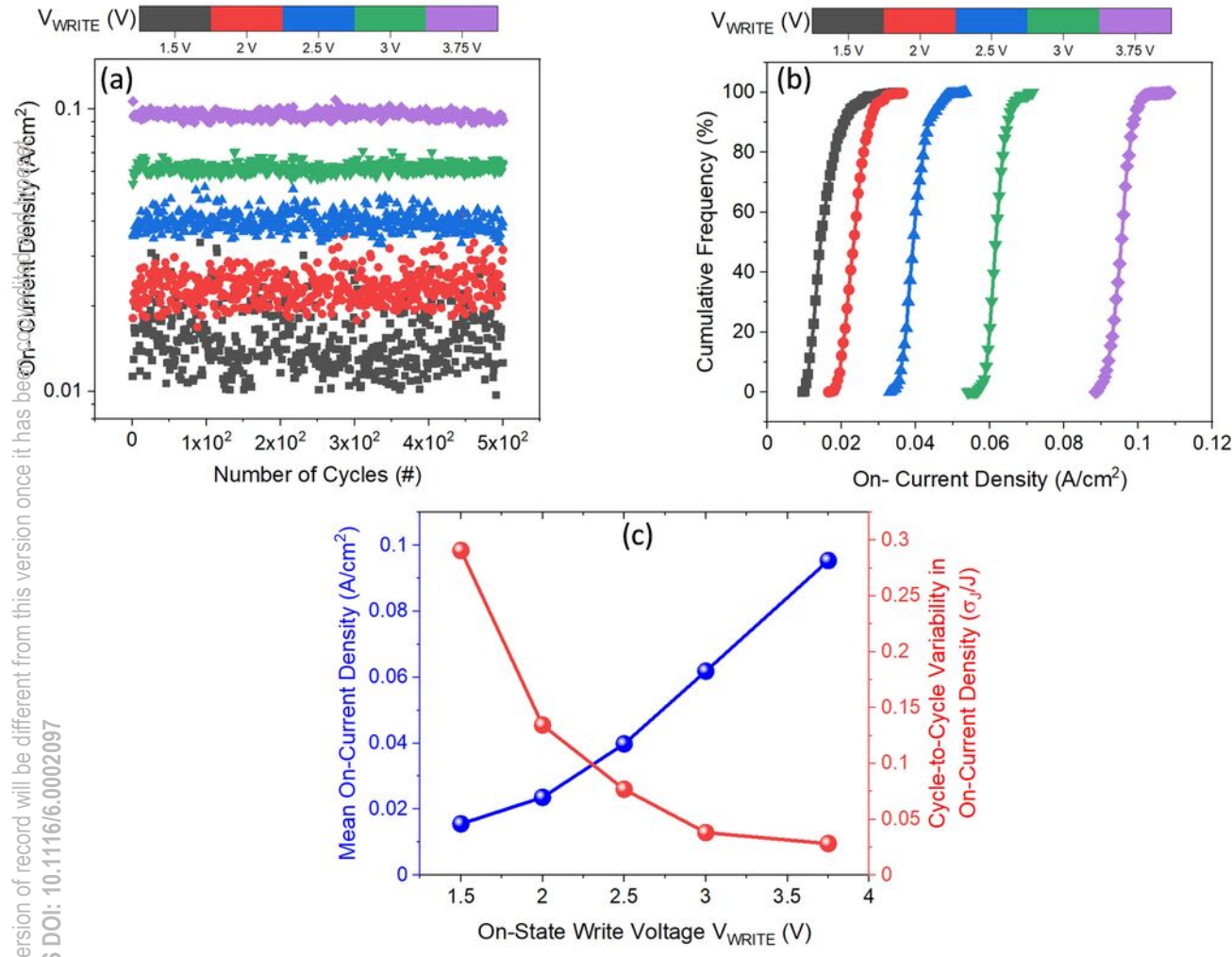


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