CuTi as potential liner- and barrier-free interconnect conductor

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Abstract— **CuTi layers are co-sputter deposited on 20-nm-SiO_2/Si(001) wafers at 350 °C to quantify their stability in direct contact with a dielectric and to explore the potential of CuTi as barrier- and liner-free interconnect metal. X-ray diffraction pole figures indicate a preferred 001 out-of-plane crystalline orientation and Rutherford backscattering confirms a stoichiometric composition. Vacuum annealing tests at 450 °C of CuTi layers indicate considerably higher thermal stability than for pure Cu layers, including negligible dewetting observed by scanning electron microscopy and negligible intermixing with the oxide substrate quantified by photoelectron spectroscopy. Four-point bend tests show a 25% higher interfacial toughness for CuTi/SiO_2 than Cu/SiO_2 interfaces. CuTi/SiO_2 samples also exhibit a 300-times longer failure time than Cu/SiO_2 during time-dependent dielectric breakdown tests using an externally applied 3 MV/cm electric field. The higher stability of CuTi in comparison to Cu is attributed to a higher cohesive energy in combination with an atomically thin self-limiting Ti oxide layer at the CuTi/SiO_2 interface.**

Index Terms—**CuTi layers, interconnects, stability, barrier-free**

I. Introduction

Cu interconnect technology including dual-damascene processing and Ta/TaN liner/barrier layers have dominated back-end-of-line integrated circuit manufacturing for over two decades [1, 2]. However, the decreasing pitch size for each technology node causes an increasing resistance and associated signal delay and power consumption [3, 4]. The resistance increase is due to both a reduced interconnect cross-sectional area and an increased Cu resistivity caused by electron scattering at surfaces [5-8] and grain boundaries [9-13]. As a result, considerable research effort has focused on exploring alternative materials to replace Cu metallization [14-17], considering both elemental metals like Ru [18], Co [19], Ir [20], Rh [21], W [22] and Mo [23], or compound conductors including $CuAl_2$ [24], NiAl [25, 26], Al_3Sc [27], Cu_2Mg [28], VNi_2 [5], and Ti_4SiC_3 [29] as conductive material. These alternative conductors have the potential to outperform the Cu line conductance at small dimensions based on either a suppressed resistivity size effect due to a small electron mean free path and/or a liner/barrier free metallization scheme [14]. Liner/barrier layers are required for Cu lines to facilitate adhesion and suppress electromigration and Cu diffusion into the dielectric [30, 31]. However, they occupy a considerable fraction of the space within the trench, effectively increasing the resistance of Cu lines. Conversely, a conductive material which does not require liner/barrier layers has a conductance advantage over Cu at small dimensions. We have recently quantified the intrinsic resistivity scaling of CuTi and $CuAl_2$ using a combination of transport measurements on epitaxial layers. We found that $CuAl_2$ [24] has a comparable resistivity scaling with W [22, 32] and Co [19, 33, 34] while CuTi has a worse resistivity scaling and only provides a conductance advantage if its large cohesive energy facilitates liner/barrier-free metallization [35]. Thus, in this letter, we present a study on the stability of the CuTi/SiO_2 interface, representing the first step towards a potential liner/barrier-free CuTi metallization. Direct comparison of CuTi/SiO_2 with Cu/SiO_2 layers indicates a range of CuTi advantages including a higher thermal stability, better wetting and less intermixing with the oxide, a higher interface toughness, and a higher stability against time-dependent dielectric breakdown. The CuTi electromigration (EM) performance is also expected to be superior, although it is not directly measured in this study. More specifically, based on previous studies on other metals including Cu and Co [36, 37], the EM activation energy is proportional to the melting point T_m [36, 38], while T_m is proportional to the cohesive energy [39]. The cohesive energy of 4.33 eV/atom for CuTi [35] is 24% larger than that for Cu (3.49 eV/atom) [40], resulting in a substantially larger expected electromigration performance for CuTi.

II. Procedure

CuTi and Cu films were deposited onto 20-nm-thick thermal SiO_2/Si(001) substrates in a ultrahigh vacuum DC magnetron sputtering system with a base pressure of 10^{-7} Pa [41, 42]. The multistep substrate preparation and layer deposition processes are described in more detail in our previous publication [35] and include co-sputtering of 51-mm-diameter Cu (99.999%) and Ti (99.995%) targets in 3 mTorr 99.999% pure Ar using constant powers of 60 and 50 W to achieve stoichiometric CuTi deposition onto substrates which are kept at 350 °C.

X-ray diffraction (XRD) polefigures were acquired with a PANalytical X'pert PRO MPD system using a point source with a polycapillary x-ray lens that provides a quasi-parallel Cu Kα beam with a divergence <0.3°. The diffraction angle was kept constant at $2\theta = 42.13°$ to detect the CuTi 012 reflection. Rutherford back scattering (RBS) spectra were obtained in a 10^{-7} Torr chamber using a 2 × 2 mm^2 2 MeV alpha-particle beam. The backscattered intensity was measured at a scattering angle of 166° and data analysis was done using the SIMNRA simulation software [43].

The scanning electron micrographs were obtained in a VERSA scanning electron microscope (SEM) with a 10 keV primary electron beam and a 6 mm working distance. X-ray

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photoelectron spectroscopy (XPS) depth profile plots from the same annealed Cu and CuTi layers were obtained with a PHI 5000 Versaprobe system with a hemispherical analyzer and an 8-channel detector using Al Kα radiation (1486.6 eV) and a 3 keV 2 mA Ar^+ beam incident at 45° relative to the surface normal over a 1 mm^2 area for sputter etching.

Four-point-bend mechanical tests were done on dummy-Si/epoxy/Ti/metal/SiO_2/Si test structures. More specifically, 50-nm-thick Cu or CuTi metal layers were deposited on 20-nm-thick thermal SiO_2/p-type Si substrates, followed by deposition of 200-nm-thick Ti adhesion layers in the same sputtering system. The Ti/metal/SiO_2/Si(001) stacks were bonded to dummy Si wafers with epoxy T88 and diced into 6 × 30 mm beams. A 400-μm-deep notch was machined into the host Si wafer to initiate the delamination during mechanical testing [44, 45]. Room-temperature time-dependent dielectric breakdown (TDDB) experiments were done on Cu/SiO_2/Si and CuTi/SiO_2/Si samples. The top electrodes were 100-μm-diameter 100-nm-thick Cu or CuTi layers that are formed using a lift-off process [26] while the bottom electrodes are 300-nm-thick Al layers deposited on the backside of the Si substrate to form ohmic contacts.

III. Results

Figure 1 shows representative XRD and RBS results from a 44.3-nm-thick CuTi layer. The XRD polefigure in Fig. 1(a) shows the CuTi 012 reflection as a circularly symmetric ring at a χ = 45 ± 3° sample tilt with negligible intensity at other χ values. The expected angle between CuTi 012 and 001 planes is 45°. Thus, the polefigure indicates a 001 out-of-plane growth direction with a random in-plane orientation and negligible misoriented grains, consistent with our previous work which indicates a 001 texture for CuTi/SiO_2 growth with a 1.7° rocking curve width [35]. This polycrystalline structure is as expected for the thin film growth on amorphous SiO_2, while the crystalline orientation of the underlying Si(001) substate is expected to have no effect on the CuTi growth. The RBS spectrum in Fig. 1(b) shows the measured reflected intensity vs particle energy as red data points and the result from data analysis as blue line. The peaks at 1.41 and 1.53 MeV are due to He reflections at Ti and Cu nuclei in the CuTi layer, the O-peak at 0.65 MeV is from the SiO_2 thermal oxide, and the Si shoulder below 1.1 MeV from the SiO_2 layer and the Si substrate. The O-peak shape indicates negligible oxygen impurity in the CuTi layer, as expected for deposition in a system with a 10^{-7} Pa base pressure which is estimated to lead to a maximum 0.1% impurity concentration. Quantitative analysis yields 49% Cu and 51% Ti atoms in the layer, confirming a stoichiometric CuTi composition within the ± 2% experimental uncertainty.

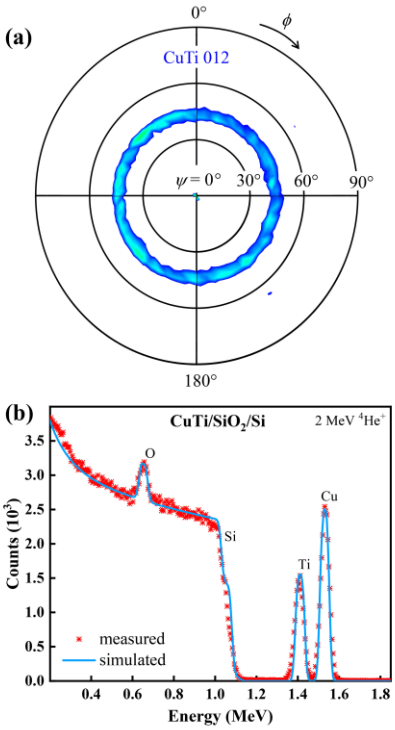

Fig. 1. (a) X-ray diffraction pole figure for the CuTi 012 reflection and (b) RBS spectrum from a 44.3-nm-thick CuTi/SiO_2 layer.

Figures 2(a) and (b) show secondary electron micrographs from as-deposited Cu and CuTi layers with a 40 nm (nominal) and a 44.3 nm (measured) thickness, respectively. Both Cu and CuTi show good surface coverage on the amorphous SiO_2 substrate, with 30-100 nm and 10-30 nm wide surface mounds, respectively. The micrograph from the Cu layer in Fig. 2(a) also shows dark contrast features which may indicate 10-50 nm wide pinholes caused by the poor wettability of Cu on dielectric SiO_2 [30], as previously reported for bare Cu films grown on SiO_2 without liner [46]. In contrast, no evidence for pinholes can be detected in Fig. 2(b) from the CuTi film. Figures 2(c) and (d) are SEM micrographs from the same Cu and CuTi layers but after vacuum (10^{-9} torr) annealing at 450 °C for 15 min. The Cu layer exhibits a discontinuous microstructure with large 100-300 nm wide islands, suggesting dewetting of the Cu on SiO_2 during annealing. The corresponding micrograph for CuTi in Fig. 2(d) shows a continuous film with 10-50 nm wide circular surface mounds and no pinholes or cavities, indicating only minor surface morphological changes during annealing of the CuTi layers. Thus, in summary, the SEM micrographs reveal quite dramatic microstructural changes during annealing of the Cu layer but relatively modest changes for CuTi, indicating a considerably higher thermal stability of the CuTi compound. We note that resistivity measurements show an infinite resistance for the annealed Cu layer, confirming the discontinuous microstructure. The CuTi sheet resistance is 14% higher after annealing than for the as-deposited layer, which may be attributed to increased surface roughness, surface oxidation during annealing and/or precipitation of Ti or Cu rich impurity phases. Figures 2(e) and (f) are XPS depth profile plots from the same annealed Cu and CuTi layers, respectively. The profile in (e) shows a Cu signal which decreases nearly linearly from 80 to 0 at.% over a sputter depth of 20 to 70 nm while the O and Si signals simultaneously increase, exhibiting a 2:1 ratio

as expected for SiO_2. The Si-signal is non-zero prior to sputter etching and remains approximately constant at 8±2 at.% for the first 20 nm of depth. This indicates that the Cu surface coverage is incomplete (80±5 %) for this annealed layer so that the SiO_2 substrate can be detected, consistent with the micrograph in Fig. 2(c). In contrast, the profile in Fig. 2(f) shows no detectable Si signal until a sputter depth of 43 nm is reached, indicating complete coverage of the SiO_2 by the CuTi layer. Further sputtering leads to a fast transition from Cu and Ti to Si and O within 3 sputter cycles, indicating a sharp interface between the CuTi film and the SiO_2 substrate with negligible intermixing and/or Cu diffusion into the SiO_2. The stark differences in the two depth profiles confirm the much better wetting of SiO_2 by CuTi than by Cu. Thus, CuTi is stable against dewetting in direct contact with the dielectric during typical BEOL thermal treatment processes, which is promising when considering its promise as a barrier-free interconnect metal.

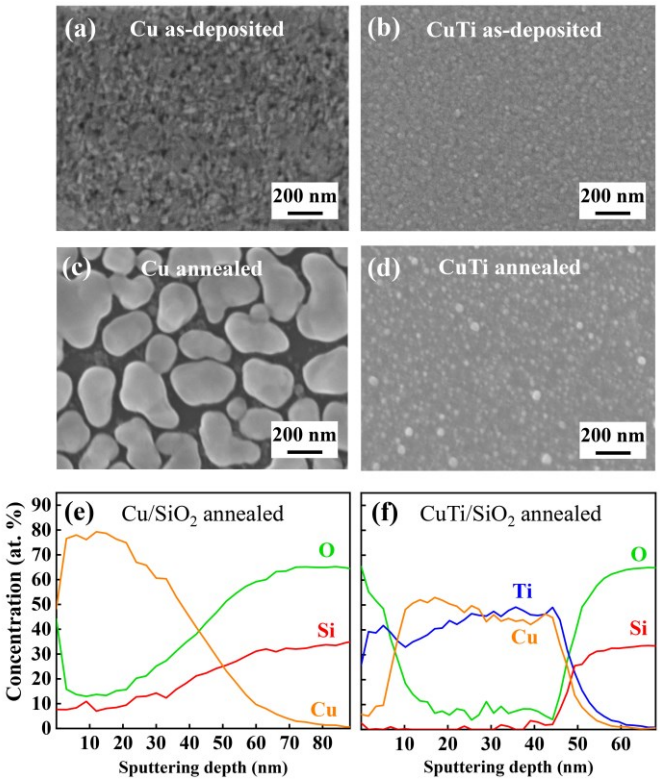

Fig. 2. SEM micrograph of as-deposited (a) Cu/SiO_2 and (b) $CuTi/SiO_2$ thin films. (c) and (d) show the corresponding Cu and CuTi micrographs after vacuum annealing at 450 ℃ for 15 min, and (e) and (f) are compositional XPS depths profiles of the annealed films.

Figure 3 shows the results from four-point-bend mechanical tests which are used to quantify the Cu-SiO_2 and CuTi-SiO_2 interface toughness G, also referred to as the interface debonding energy [47]. The plot in Fig. 3(a) shows typical load-displacement curves from a Cu and a CuTi sample, obtained using a slow strain rate of 0.01 µm/s. A steady-state interfacial delamination occurs in the dummy-Si/epoxy/Ti/metal/SiO_2/Si test structures [illustrated in Fig. 3(a)] when the crack from the notch tip reaches the weakest interface and spreads along the interface, forming a plateau in the load-displacement curve at a critical load P_c [44, 48]. The higher P_c for CuTi indicates a higher critical load for debonding of CuTi from SiO_2 than for the Cu-SiO_2 interface. The corresponding interface debonding energy is obtained using $G = K(1-\nu^2)P_c^2/E$, where E = 190 GPa and ν = 0.28 are the elastic modulus and Poisson's ratio of the Si substrate, and $K = 21L^2/16b^2h^3$ is a geometric factor where L is the spacing between inner and outer loading line, b is the beam width and h is the half thickness [49-51]. Fig. 3(b) shows the resulting interfacial toughness for the Cu-SiO_2 and CuTi-SiO_2 interfaces. The plotted solid black squares indicate the average values from five delamination experiments, the boxes denote the standard deviation and the whiskers indicate the minimum and maximum from the five measurements. The CuTi-SiO_2 interfacial debonding energy of 7.5 J/m^2 is 25% higher than the measured 6.0 J/m^2 for the Cu-SiO_2 interface. The better interfacial adhesion is expected to correspond to a higher electromigration (EM) performance [52]. Thus, the higher interfacial toughness of CuTi-SiO_2 suggests good EM resistance of possible liner-free CuTi interconnects.

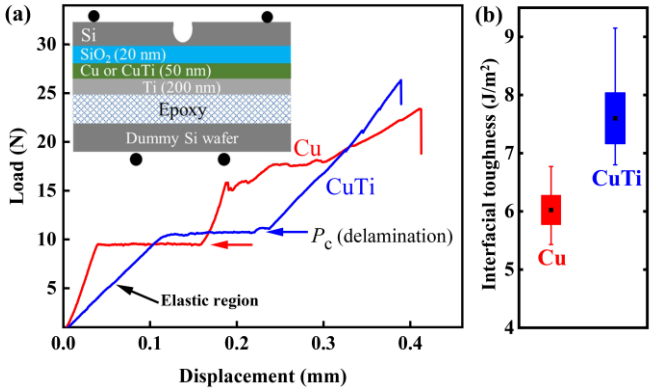

Fig. 3. (a) Representative load-displacement curves and (b) Cu-SiO_2 and CuTi-SiO_2 interfacial toughness determined from critical load P_c delamination plateaus during 4-point bend tests on test structures shown in the inset of (a).

Figure 4 shows the results from room-temperature TDDB experiments. Typical leakage current curves are plotted in Fig. 4(a) as a function of time for a $Cu/SiO_2/Si$ and a $CuTi/SiO_2/Si$ sample, using a positive bias of 6 V. Nearly the entire potential drop occurs across the 20-nm-thick SiO_2, corresponding to 3 MV/cm within the SiO_2 with negligible potential drop in the Cu or CuTi. The Cu/SiO_2 sample fails after ~10 s, while the failure for $CuTi/SiO_2$ occurs after 4000 s. This suggests that the ion drift into the SiO_2 is 400 times slower for the CuTi than the Cu layer, indicating a strong advantage of CuTi over Cu with regards to TDDB performance. The inset in Fig. 4(a) shows the leakage current for an inverse bias of -5 MV/cm. Inverse bias involves no ion drift into the oxide such that these experiments reveal the intrinsic breakdown of SiO_2, independent of if the top electrode is Cu or CuTi. Both samples exhibit a similar time to failure of ~200 s, confirming that the breakdown is independent of the metal layer composition, as expected for an inverse bias, and also indicating a consistent dielectric quality. We note that positive-bias experiments with this higher 5 MV/cm field lead to fast failure within a few seconds as metal ions quickly penetrate into and through the oxide and accumulate to reach a threshold level that causes nearly immediate dielectric breakdown [53]. Correspondingly, we use a smaller positive bias of 3 MV/cm for our statistical TDDB measurements and analyses and consider breakdown if the measured current reaches 10^{-1} A. This value is relatively high in comparison to other studies [53, 54] and is chosen because of our relatively large electrode area of 7.9×10^3 µm^2.

Figure 4(b) is a Weibull distribution plot showing the cumulative failure time from eight Cu and CuTi electrodes during 3 MV/cm TDDB tests. This quantitative analysis follows the most common approach to evaluate TDDB tests [53, 55-57]. The fitted scale parameters yield statistical failure times of 21 s for Cu and 6800 s for CuTi. The failure time for CuTi is over 300-times longer, indicating a superior interdiffusion reliability on bare SiO_2 dielectric for CuTi in comparison to Cu. The data fitting also yields the shape parameter β in the Weibull distributions of 1.5 and 2.3 for Cu and CuTi, respectively, suggesting a higher defect concentration in the SiO_2 in contact with Cu. It is generally believed that Cu ions that diffuse into SiO_2 bond to two-coordinated bridging oxygen atoms to form a shallow energy level in the SiO_2 band gap, allowing Poole-Frenkel type conduction [58]. Thus, the SiO_2 in direct contact with Cu (in comparison to CuTi) exhibits a higher localized defect concentration which is due to the interaction between migrated Cu ions and SiO_2. The resulting higher interdiffusion reliability of CuTi on SiO_2 is attributed to the higher cohesive energy which facilitates superior stability of the interconnect material. Specifically, a high cohesive energy has been related to a high stability under thermoelectric stress [59] and a high formation energy for vacancies, resulting in slow self-diffusion kinetics [16]. Therefore, the rate for Cu atoms leaving the CuTi layers is expected to be considerably lower than for pure Cu, yielding the observed improved TDDB stability.

The inset in Fig. 4(b) provides some additional information about the physical reasons for the CuTi-SiO_2 interdiffusion reliability. It is a plot of the XPS Si 2p peak evolution at the CuTi-SiO_2 interface region corresponding to sputter cycles #28 - 33. The peak for cycles #31-33 is at a binding energy of 102.9 eV, close to the expected 103.3 eV for SiO_2. However, it shifts left to lower binding energies near the CuTi layer for cycles #28-30, indicating a reduction of SiO_2. This indicates the formation of an interfacial Ti oxide layer at the SiO_2-CuTi interface. This interfacial oxide is expected to act as an intrinsic diffusion barrier layer to kinetically retard the diffusion between interconnect and dielectric, resulting in the measured enhanced interdiffusion reliability. The interfacial Ti oxide may also enhance interfacial adhesion [26], but we note that the plotted binding energy is simply a measure of the bond ionicity and cannot directly quantify the strength of the atomic bonds at the interface. We also note that XPS depth profiles after annealing exhibit similar characteristics, indicating that the interfacial oxide is self-limiting and is therefore expected to form a continuous layer with a uniform thickness, facilitating the stability of the CuTi-SiO_2 interface. Thus, the reliability of CuTi compensates for its larger resistivity scaling [35] and yields possible benefits for the future interconnects.

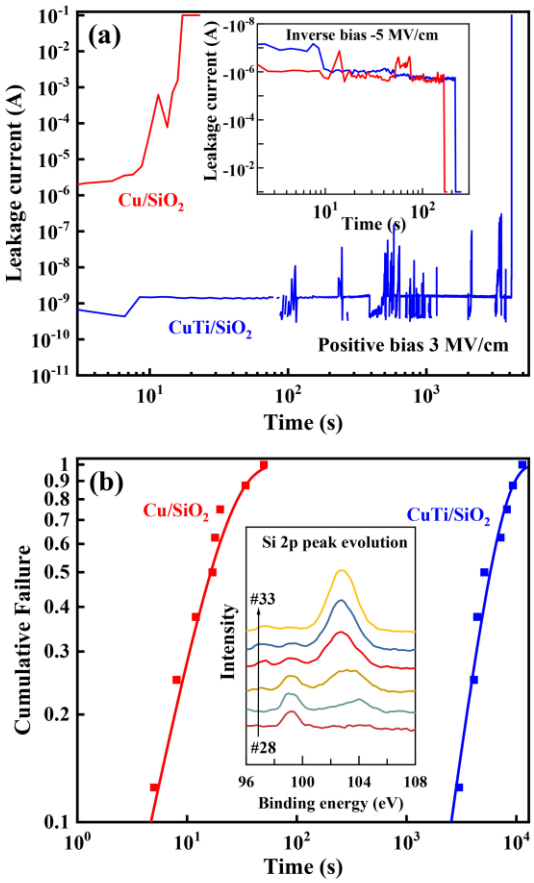

Fig. 4. (a) Typical leakage current vs time and (b) Weibull plots from 3 MV/cm TDDB tests of 20-nm-SiO_2 with Cu and CuTi top electrodes. The inset in (a) shows results from tests with -5 MV/cm inverse bias. The inset in (b) shows the XPS Si 2p peak near the CuTi-SiO_2 interface during a depth profile experiment for sputter cycles #28-33.

IV. Conclusions

CuTi layers on SiO_2 exhibit higher thermal stability against dewetting than Cu layers during vacuum annealing at 450 °C. They also exhibit negligible intermixing with SiO_2 and a 25% higher interfacial toughness, suggesting higher resistance against electromigration than Cu. CuTi-SiO_2 exhibits a 300-times higher failure time than Cu-SiO_2 during TDDB tests with 3 MV/cm. The higher stability of the CuTi-SiO_2 interface is attributed to a self-limiting interfacial Ti-oxide layer and indicates the potential for barrier-free CuTi metallization.

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