A High-Density 200-kW All Silicon Carbide Three-Phase Inverter for Traction Applications

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***Abstract*—This work presents the design and development of a high density 200-kW three-phase inverter for traction applications with elevated DC bus voltage, e.g., up to 1.2 kV. A state-of-the-art six-pack 1.7-kV silicon carbide (SiC) power module is used in this design. To achieve a compact system integration and ultra-low power loop inductance, the custom laminated bussing structure is optimized with the detailed design along the method of estimating the parasitic inductance presented in this work. The designs of other key components, such as a compact six-channel gate driver board, are also presented. The inverter prototype was tested at different switching frequencies and dead times to investigate their effect on the performance. The inverter achieved a peak efficiency of 99.3% at 10kHz, and a 43kW/L power density.**

Keywords—Silicon carbide, traction inverter, power density

I. Introduction

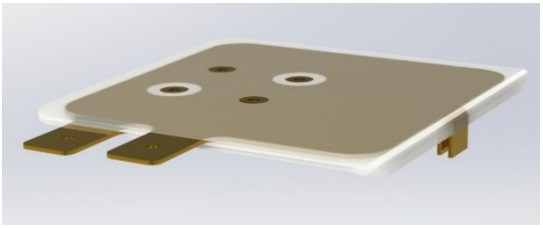
Major advancements are made in the power electronics field due to the megatrend of global electrification. With each step forward, the demand for smaller, lighter, and more efficient power conversion systems is increasing. The transportation electrification is a major point of interest due to the huge potential for carbon footprint reduction and energy savings, as it currently contributes to around 28% of total energy consumption in the U.S. [1]. Moreover, high power density is becoming more important especially with the movement towards more electric aircrafts (MEA) and all electric aircrafts (AEA) [2]. The maturity of silicon carbide (SiC) power semiconductors has enabled various new frontiers in the development of a wide range of power electronic applications. By providing faster switching speeds, higher breakdown voltages, and higher operating temperatures, SiC based power electronics require smaller passive components, simplified cooling solutions, and can be integrated in more compact packages [3]. Power switches in discrete packages like the common TO packages have substantial parasitics that limits the switching frequency and current capabilities of the device in practical applications, which greatly prevents the fully exploitation of the advantages of the new SiC devices [4], especially for the traction applications [5]–[7]. To address these issues, major manufacturers have rolled out power modules with more compact packages that features significantly low parasitic inductance and are optimized to enhance capabilities of the SiC switches.

This work was supported in part by the U.S. National Science Foundation (NSF) under CAREER Award ECCS-1751506.

In this work, the design of a high-density 200 kW, with rated 1 kV DC and 480 V output ac, three-phase inverter is proposed using a state-of-the-art 1.7 kV six-pack SiC power module (part number GE17045EEA3 [5]) from GE Aviation, achieving a peak efficiency of 99.3% at 10kHz, and a 43kW/L power density for the overall inverter system.

II. Power Stage Design and Optimization

The 1.7 kV six-pack module used in this work has a rated current of 450 A per switch with a 5 mΩ on-state resistance and integrated kelvin connections and temperature sensors. To minimize the power loop parasitic inductance and accommodate the unique bussing structure of the module, a custom copper bussing was designed with 3/32" (2.38mm) thick 110 copper laminates, separated by two layers of 3mil of PEI insulation film (total of 6mils, or 0.152mm), thus achieving adequate insulation while minimizing the inductance on the busbar by minimizing the distance between the two copper laminates. Using two layers



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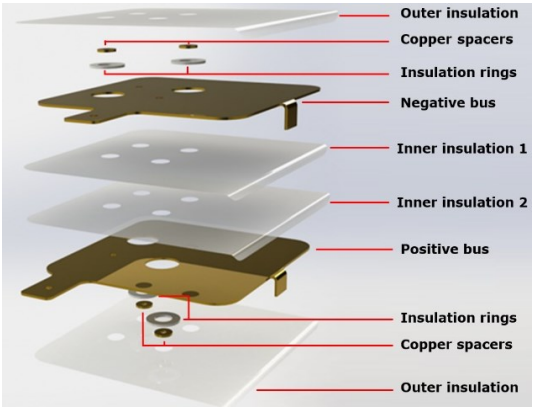

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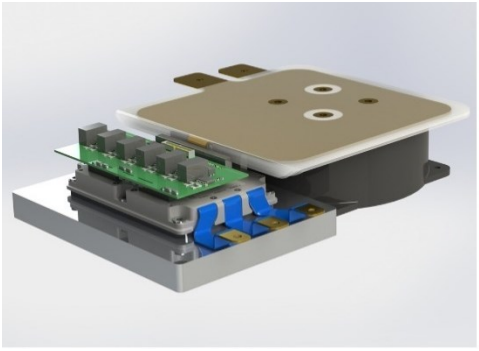
Fig. 1. (a) The overall custom copper bussing. (b) exploded view showing the components of the bussing



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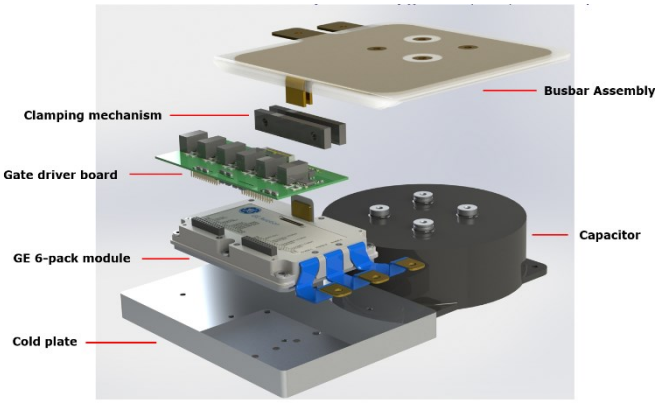

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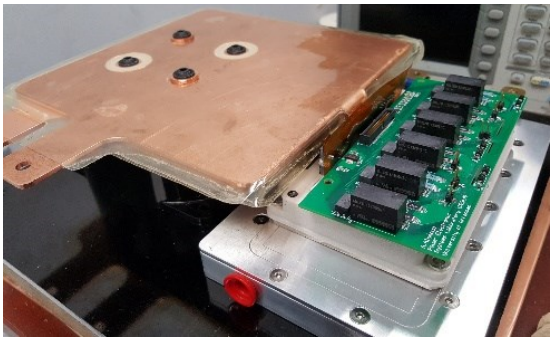
Fig. 2. (a) Inverter power stage assembly. (b) exploded view showing the components of the assembly.



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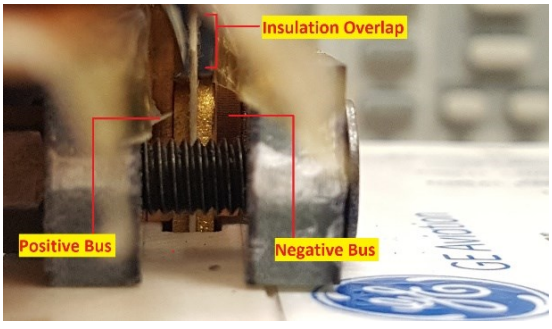

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Fig. 3. (a) the inverter power stage after assembling. (b) a zoomed in image of the bussing clamping mechanism.

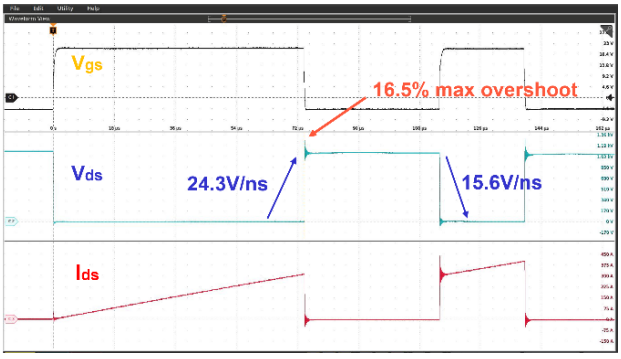
of insulation film minimizes the chance of having a breakdown due to imperceptible imperfections since each layer is capable of withstanding over 5kV. The bussing along an exploded view of its components can be seen in Fig. 1.

The busbar extrudes and bends downwards to fit over the module's DC bussing terminals, and is clamped over by two machined pieces of G10 fiberboard with M6 bolts. The bussing is mounted over a DC link capacitor with ultra-low inductance [8]. The module is mounted over an off-the-shelf coldplate and is driven by a custom gate driver board. The inverter assembly along with an explode view of the components can be seen in Fig. 2.

The gate driver board is designed based on the Texas Instruments® UCC21750 gate driver IC, and features a short circuit de-sat protection circuit, active miller clamp, and a soft turn off under fault conditions. The temperature signals from the power modules are isolated, and a low-voltage differential signaling protocol was used for all signal lines to minimize any electromagnetic interference. The assembled inverter is shown in Fig. 3(a) and a zoomed-in view of the clamping mechanism in action is shown in Fig. 3(b). The overall volume of the inverter is approximately 4.65 L, including the coldplate and gate driver board, which translates into a power density of around 43 kW/L with 200 kW rated power.

III. Design Validation using Switching Tests

Double pulse tests (DPTs) have been performed to validate the effectiveness of the prototype and extract the parasitic inductance of the current commutation loop. Fig. 4(a) shows a



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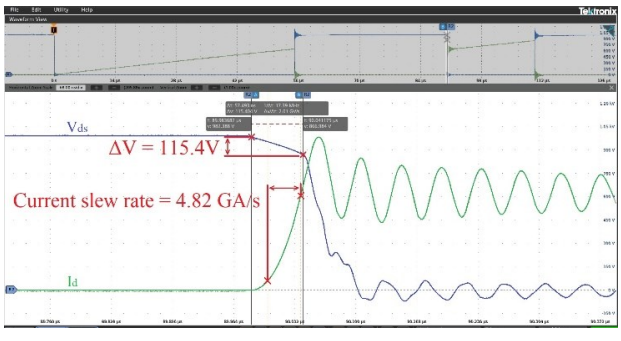

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Fig. 4. (a) DPT waveform at 1100V and 300A. (b) Inductance estimation using the initial voltage drop and the current slew rate at the switch turn-on waveform

typical DPT result at 1100 V DC, 300 A load current with 2.49 Ω external gate resistance. The measured drain-source voltage (Vds) overshoot was 182V and the dv/dt of the Vds is 24.3 V/ns.

During the turn-on, the waveform of the Vds drop has two distinct regions with different slew rates. The first region is slower and is dominated by the parasitic inductance of the power loop [9]. According to $v = L\ di/dt$, the power loop inductance can be extracted by measuring the voltage drop across the region and the drain current slew rate during the same period of time. The measured Vds drop at the first region of the turn-on waveform was around 115V, while the slew rate of Id was measured to be 4.82 GA/s, as demonstrated in Fig. 4(b). Then L can be found to be approximately 23.9 nH, which represents the parasitic inductance of the overall commutation loop, including the bussing, capacitor, and the module.

IV. High Power Experiemntal Study

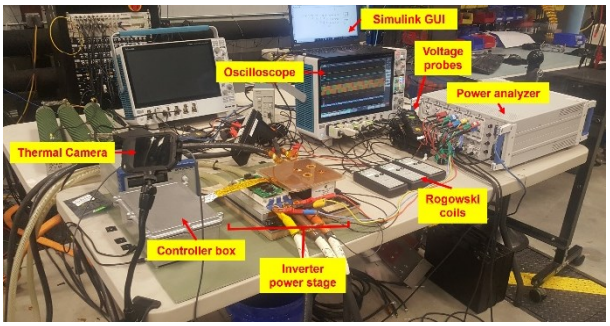
A. Test Setup

The inverter is controlled by a DSP board connected over a shielded differential line into the gate driver board. The DSP generates the PWM signals and monitors the gate driver board's fault signals. A trip zone module is incorporated to ensure fastest response to faults, and a real time communication with a custom Simulink interface enables the operators to modify and monitor the inverter parameters from a safe distance. The performance points and waveforms are captured by a Textronix MSO58 oscilloscope and a Hioki PW6001 power analyzer. A picture of the high power testing setup shown the main components can be seen in Fig. 5(a), while a zoomed-in image of the inverter power stage and shielded controller box can be seen in Fig. 5(b). The inverter current is controlled by a remote-controlled variable load bank with a 340 µH line reactance and the overall schematic diagram of the electrical setup could be seen in Fig. 5(c).

B. Experimental Results

The inverter prototype was tested up to the rated power with approximately 25 kW load steps. A typical inverter waveforms at 180 kW can be seen in Fig. 6(a). A combination of different gate resistors, switching frequencies, and dead times were tested to demonstrate their impacts to the performance of the inverter. Fig. 6(b) shows the efficiency vs. power curves for 2.49, 5.1, and 10 Ω gate resistors at a switching frequency of 10 kHz, where the lower gate resistance increases the efficiency, as the higher switching speed would result in lower switching losses. In Fig. 6(c) the inverter was tested at 5, 10, and 20 kHz with a 5.1 Ω external gate resistor. The results show a decrease in efficiency with higher switching frequencies due to the higher switching losses.

While previous experiments were performed with a fixed 1.5 µs dead time (DT), Fig. 6(d) demonstrates the efficiency curves at 1, 1.5, and 2µs DT. Although marginal, lower DT positively affected the efficiency.



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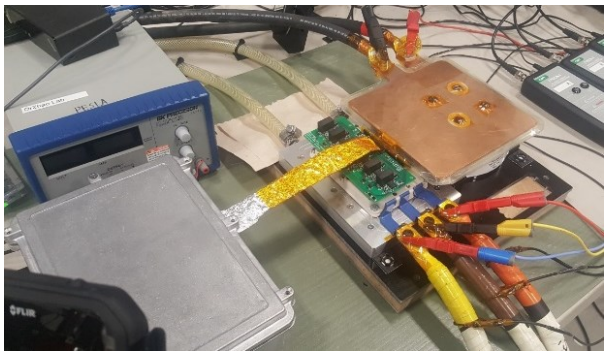

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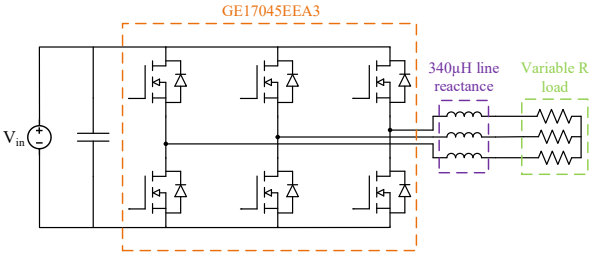

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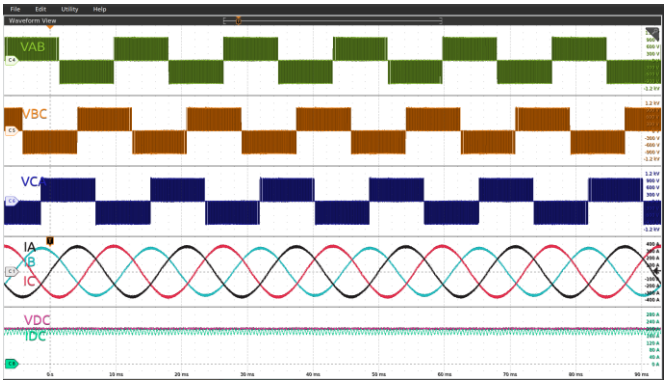
Fig. 5. (a) High power test setup showing main components. (b) a zoomed-in image of the inverter power stage and shielded controller box. (c) the schematic diagram of the inverter testing circuit.

V. Conclusion

This work presented the design and the development of a high-density 200-kW three-phase traction inverter using a 1.7-kV six-pack SiC power module for a simplified design and high-power density. With the custom laminated bussing architecture, the proposed design achieved less than 24nH of commutation loop inductance and a max overshoot of 182V at a slew rate of 24.3 V/ns. The inverter achieved a peak efficiency of 99.3% at 10kHz, and a 43kW/L power density. The performance was evaluated at different operating points and the effect of different gate resistors, switching frequencies, and dead times on the inverter's efficiency was demonstrated.



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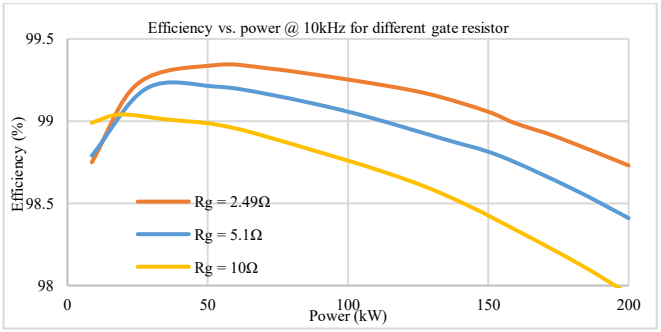

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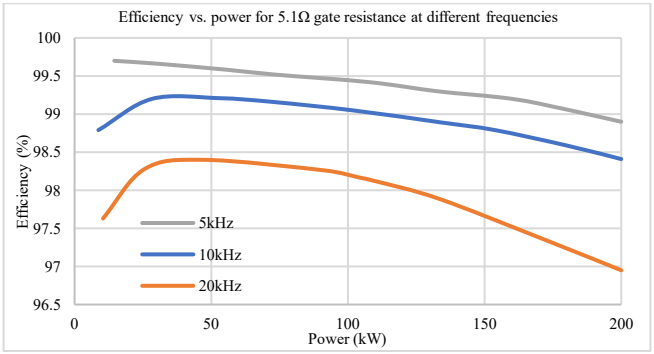

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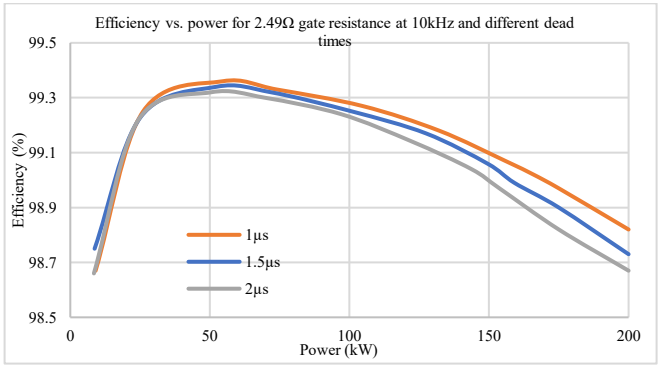

(d)

Fig. 6. (a) Inverter waveforms at 180kW. (b) Efficiency vs. power curves for different gate resistors. (c) Efficiency vs. power curves for different frequencies. (d) Efficiency vs, power curves for different dead times

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