Design and Demonstration of a Medium-Voltage High-Power All Silicon Carbide ANPC Converter with Optimized Busbar Architecture

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***Abstract*—In this paper, the design and optimization of a high-power active-neutral-point-clamped (ANPC) converter using 1.7 kV silicon carbide power modules and low-inductance laminated bussing architecture are presented. Various optimizations have been performed to reduce parasitic inductance along the current commutation loops (CCL), while achieving high power density and meeting insulation requirements. Due to the low inductance in the CCLs, the proposed ANPC design can support up to 2.6 kV DC link voltage. In addition, a method to improve the accuracy of voltage ringing frequency measurement during the switching transient has been proposed, which can further lead to a precise CCL stray inductance calculation that agrees well with the measurement using impedance analyzer and the Q3D based simulation. Extensive experimental studies, including switching tests and continuous power tests, have been performed to validate effectiveness of proposed methods and the converter prototyped.**

***Index Terms*—ANPC converter, laminated busbar, optimization, silicon carbide**

I. Introduction

AMONG all the three-level (3-L) converter topologies, the classic neutral-point-clamped (NPC) converter has many distinctive advantages, such as its modularity, reliability and robustness [1]. The NPC converters have been widely adopted in the medium-voltage (MV) applications, such as the pump storage, wind power, and high-power drivetrain [2]. However, as the major drawback of NPC converters, uneven power loss distribution among the power switches remains unsolved until the introduction of the active NPC (ANPC) converter in 2001 [3], which introduces extra redundant switching states to realize the active loss balancing among all power switches [4]-[6]. The ANPC converter has been a good alternative to the NPC converter in many MV applications.

The silicon (Si) insulated gate bipolar transistor (IGBT) is still the dominate solution for 3-L converters [7]-[11] in the mobile applications, which offers high blocking voltage and is commercially available. However, excessive switching losses prevent the IGBT-based converters from operating at higher switching frequency, which in turn enlarges volume of the filter including the passive components. With the state-of-the-art silicon carbide (SiC) MOSFET, which offers much fast-switching speed and lower switching loss compared to its Si counterpart [12]-[16], the 3-L converter can be designed to operate at higher switching frequency while withstanding the DC link voltage in MV applications.

In practical applications, the fast-switching speed of the SiC MOSFETs can lead to excessive voltage overshoot across the switches, due to the parasitic inductance along the current commutation loop (CCL) in an ANPC converter. This voltage overshoot may lead to design derating with either lower dc bus voltage or slower switching speed of the switches, which prevents the fully utilization of the SiC devices. To address these issues, the low-inductance CCL designs are critical for MV ANPC converters. The total stray inductance along the CCL usually consists of three parts, i.e., parasitic inductance of the power modules, the stray inductance of the busbar, and equivalent series inductance (ESL) of the DC-Link capacitors, among which the stray inductance of the busbar relies on its geometry and the converter system architecture, thus need to be carefully designed and optimized.

The CCL stray inductance of an ANPC converter can vary significantly depending on the rated voltage and power of the converters. For example, for a MV converter rated below 100 kVA, less than 10 nH CCL stray inductance can be achieved using the multilayer printed circuit board (PCB) based bussing structure [17], shown in Table I. When the rated power reaches 250 kVA and beyond, the lowest CCL stray inductance in a MV converter reported is 78 nH [10], [18]-[22], due to the use of high-current power modules and larger size busbars with design constraints to accommodate the insulation requirements, as shown in Table I. For low-voltage (LV) high power 3-L

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TABLE I
COMPARISON AMONG PROPOSED DESIGN AND OTHER WORKS

Reference	Proposed design	[6]	[9]	[11]	[17]	[20]	[21]	[22]	[31]	[32]	[33][34]
Power for three phase (kVA)	500	500	N/A	200	93	750	1000	250	1000	450	211
DC voltage (kV)	2.6	1	N/A	1.2	2	2	2.4	0.7	3	1	0.74
Small loop (nH)	24.6	6.5	48	55	N/A	78	N/A	>21.82	>50.27	>12.7	19.2
Large loop (nH)	57.6	17.5	76	135	9.9	208	115	N/A	>74.17	N/A	N/A

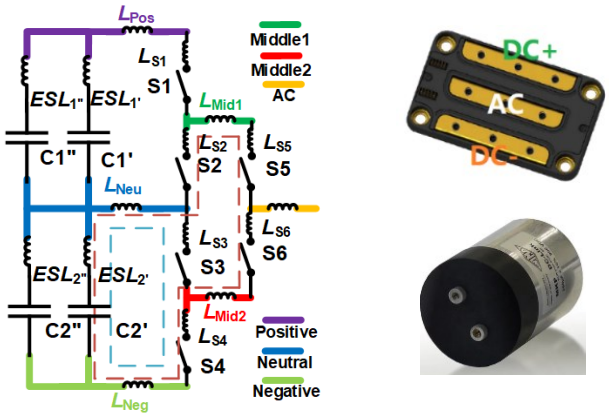


Fig. 1. The schematic of the single-phase ANPC with two CCLs labeled in dashed lines and color labeled parasitic inductance of each component with the pictures of the SiC power module and cylinder DC link capacitor used for the design.

converters, the CCL stray inductance can be much lower, such as the design with 6.5 nH stray inductance presented in [6], due to the more compact system design and the use of discrete devices and/or modules with small footprint, shown in Table I. Following discussions about the rarity of high-power MV ANPC converters with low stray inductance on their common current loop (CCL), it becomes evident that constructing a busbar for such converters is intricate. This process demands a nuanced balance among insulation, current conduction, and stray inductance, which hasn't been achieved well in other three-level converter design shown in Table I. The implementation of a low stray inductance busbar offers significant advantages, including the reduction of overshoot voltage and the enablement of elevated DC bus voltage within the same device rating. Moreover, it effectively mitigates electromagnetic interference, ensuring a cleaner power output, and facilitates swift switching speeds, thereby reducing switching losses and enhancing overall efficiency. However, the scarcity of MV ANPC converters with low stray inductance underscores the formidable challenge in achieving this optimal design for improved converter performance. This rarity emphasizes the complexity and importance of realizing MV ANPC converters with low stray inductance for enhanced operational efficiency.

In addition, the design validation, e.g., the CCL stray inductance measurement, is essential for both 3-L converter designs [6], [9]-[11], [18]-[23] and other converter designs [24]-[28], where the CCL stray inductance is usually extracted from the ringing in the voltage waveform during the switching transient. The accuracy of this approach depends on the calculation of the frequency of the voltage ringing, which however can be affected by many factors. Therefore, it is worthwhile to validate the accuracy of CCL stray inductance extraction method based on the experimental waveforms [29] and determine the best practice.

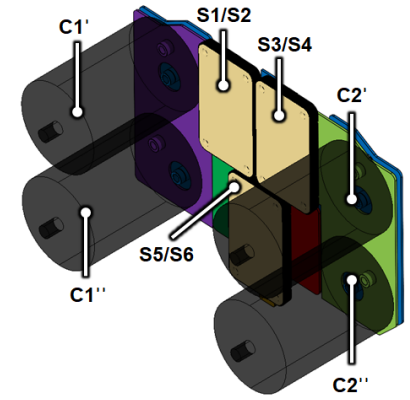
In this paper, the design and validation of a 500 kVA all SiC ANPC converter with low inductance bussing structure are presented. The proposed converter aims at the high power applications in the heavy equipment, such as the large mining trucks [30], where the DC bus voltage can be higher than 2.4 kV with air cooling. The rest of the paper is organized as follows. The power stage design including the laminated busbar to accommodate the requirements for high voltage insulation, the low stray inductance, and high operating power is presented in Section II. The design validations, using the simulation based on Q3D, the measurement based on impedance analyzer, and the calculation based on switching test results, are presented in Section III along with extensive discussions on how to improve the accuracy of inductance extraction proposed. In Section IV, the testing results from various experimental studies are presented to validate the proposed design, followed by the conclusions in Section V.

II. ANPC POWER STAGE DESIGN AND OPTIMIZATION

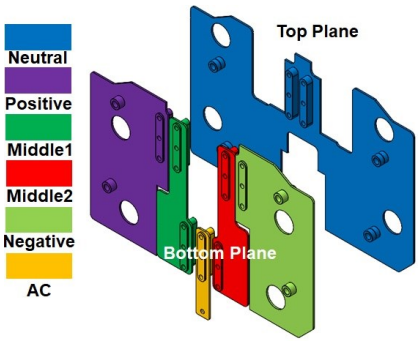
In this work, to enhance the modularity of the system, the building block concept is adopted, i.e., the three phase ANPC converter is formed by paralleling three single-phase ANPC building blocks. Each single-phase ANPC converter consists of six switches as shown in Fig. 1. The operating principles of this topology and the two CCLs have been explained in detail in [6] and [11], which are not repeated here. The small loop and large loop are labeled by the dashed blue line and dashed brown line, respectively in Fig. 1. The power modules selected for the converter prototype is the 1.7 kV SiC half bridge (HB) module HT-3234 using MOSFET dies [35] from Wolfspeed. The current conduction ability of it satisfies the specification of the converter listed in Table I, with 393 A conduction ability at case temperature T_c = 125 °C and 681 A conduction ability at T_c = 25 °C. The gate driver used for the power module is the HM3 fabricated by Wolfspeed, with the turn-on and turn-off gate resistors being 5 Ω and 2.5 Ω. The gate driver IC is from Littlefuse with 14 A current conduction ability [36] Each single-phase ANPC building block consists of three HT-3234 modules. The three-level DC link consists of four DCP6S06195E000KS0F DC link capacitors in 2×2 configuration.

A. Initial Busbar Design with Insulation Considerations

To reduce the stray inductance in the busbar [6], [21], the laminated structure should be utilized instead of the co-planar

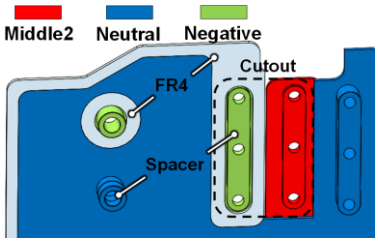


(a)

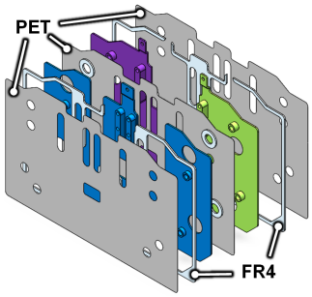


(b)

Fig. 2. The 3-D module of the initial design: (a) the assembly of the single-phase power stage, including the busbar, the capacitors, and the power modules and (b) the color-coded busbar layers.



(a)



(b)

Fig. 3. The insulation considerations (a) between metal plates and spacers and (b) between metal plates and for the edges of the busbar.

arrangement, since the laminated bussing can enhance the magnetic flux cancellation between layers. The pictures from different angles of the preliminary bussing design are shown in Fig. 2 to illustrate the arrangement of the busbar, capacitors, and power modules. The busbar layers are color coded in Fig. 2 to match with the electrical connections shown in Fig. 1. As can be seen in Fig. 2(b), the bottom copper plane consists of several copper plates, including Positive, Negative, Middle1, Middle2, and AC bars, while a wide Neutral plane is placed on the top, leading to a two-layer laminated bussing structure. The thickness of each metal plate is 2 mm to ensure enough current conduction ability. The capacitors are placed on the sides of the building block.

The maximum operating voltage of the proposed ANPC is 2.6 kV, listed in Table I. To meet voltage insulation requirements, the thickness of the polyethylene terephthalate (PET) film between the two stacked layers of busbar is 0.5 mm, while 0.25 mm thick PET films are applied to the exterior surface of the busbar. With 60 kV/mm dielectric strength, 0.25 mm and 0.5 mm thick PET films are capable of withstanding 15 kV and 30 kV, respectively. As shown in Fig. 3(a), spacers are used to provide low inductance contact between components. In order to bolt the screws to the power modules and capacitors, the spacers from the bottom copper plane should go through the Neutral plane, shown in Fig. 2(b), and Fig. 3(a). For the distances between the spacers and metal plates, both creepage and clearance distances should be satisfied. According to [37], a minimum 13 mm should be maintained between terminals with 1.3 kV voltage difference, and 26 mm for 2.6 kV, so cutouts are required on both the top and bottom planes, as shown in Fig. 3. On the edges of the busbar, FR4 is also applied for sealing. The overall insulation realization is illustrated in Fig. 3(b).

According to the equation for the total inductance ΣL of the conduction path with two conductors [6], [38], [39]:

$$\Sigma L = L_{con1} + L_{con2} + 2M \tag{1}$$

where L_{con1} and L_{con2} are self-inductances of two conductors and M is the mutual inductance, the total stray inductance can be reduced from the following several perspectives.

To reduce the self-inductance, the conductors on the CCLs should have large width and small length according to (2) [6],

$$L_{se} = \frac{\mu_o \mu_r l}{\pi}\left(\frac{1}{8} + \frac{2h}{h+w}\right) \quad (d \ll h \| d+h \ll w) \tag{2}$$

where μ_0 and μ_r are the vacuum and relative permeability of the insulation material, h, w, and l are the thickness, width, and length of the conductor, and d is the distance between two adjacent conductors, illustrated in Fig. 4.

The equation for the mutual inductance is discussed in [6],

$$M = \frac{\mu_0 \mu_r \cdot l \cdot h \cdot \cos\varphi}{\pi\sqrt{4(d+h)^2 + kw^2}} \tag{3}$$

where k is the correction coefficient and φ is the angle between the current direction of two conductors, which is shown in Fig. 4.

To reduce the mutual inductance between two conductors, directions of the current flow on the two conductors should be opposite, so that $\cos\varphi$ can be as small as possible. Specifically, when φ is larger than 90°, the $\cos\varphi$ and M becomes negative, which is the result of magnetic flux cancelation, illustrated in Fig. 4[40].

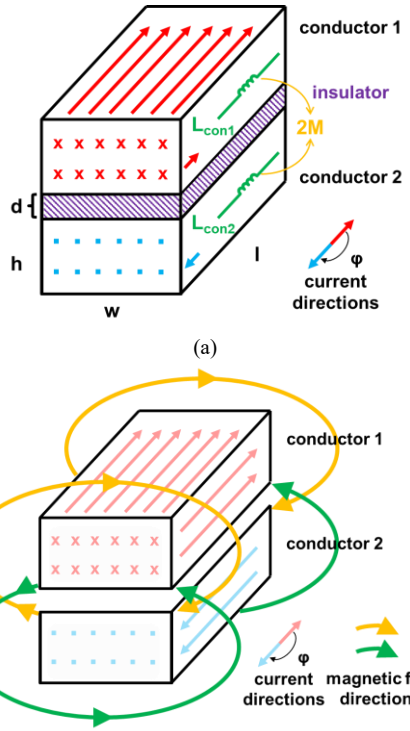


Fig. 4. The mechanism of the self and mutual inductance for two conductors, (a) illustrating the parameters for calculating inductance, (b) illustrating the magnetic field about the conductors.[40]

Since the converter circuit is symmetrical, the analysis of the upper small and long loops is the same as the one of the lower ones. So, only the lower loops are analyzed in this work.

The total inductance of the lower small loops ΣL_{sm} in the proposed converter is calculated in equation (4):

$$\Sigma L_{sm} = L_{sm} + M_{sm} + \tilde{M}_{sm} \tag{4}$$

where L_{sm} is the self-inductance of each component in the small loop, M_{sm} is mutual inductance among all components in the small loop with significant impact, while $\tilde{M}_{sm}$ is the mutual inductance over the CCL with neglectable value. The specific expressions of L_{sm} and M_{sm} for the lower small loop are,

$$L_{sm} = \frac{L_{C2'} + L_{C2''}}{2} + L_{neu} + L_{s3} + L_{s4} + L_{neg} \tag{5}$$

$$M_{sm} = M_{neu}^{neg} \tag{6}$$

where $L_{C2'}$ and $L_{C2''}$ are ESLs of $C2$' and $C2$", respectively; the L_{neu} and the L_{neg} are the self-inductance of Neutral-plate and Negative-plate, respectively; the L_{s3} and the L_{s4} are the self-inductance of switches S3 and S4, and the M_{neu}^{neg} is the mutual inductance between Neutral-plate and Negative-plate.

In the process of minimizing L_{sm}, with the selected power module and capacitor, only L_{neu} and L_{neg} can be reduced by widening and shortening metal plates Neutral and Negative, shown in Fig. 2(a). To decrease M_{sm}, the current flow on the metal plates Neutral and Negative should be as opposite as possible. As shown in Fig. 5(a), thanks to the position of the components and the shape of the two plates, the commutation currents on the two plates in the small loop flow in the opposite directions. As a result, the mutual inductance M_{sm} can be negative.

In the initial busbar, since all metal plates are integrated into a single structure, the plates Middle1 and Middle2 need to be bolted down to the modules from the top, shown in Fig. 2. As a result, large holes need to be cut on the plates Neutral as well as Positive (or Negative) to insert spacers to connect the Middle1 (or Middle2) to the modules, which significantly reduces the overlapping area between Neutral and Positive or Negative, shown in Fig. 3(a) and Fig. 5(a). No doubt, the self-inductances for the plates Neutral and Positive/Negative are increased and the negative mutual inductance between Neutral and Positive/Negative is reduced due to the inevitable cutouts in the initial design. The inductance of the initial busbar design on the small and large loops at 10 MHz are 23 nH and 50 nH, respectively.

B. Enhanced Busbar Design with Inductance Reduction

As shown in Fig. 4 and Fig. 5(b), if the overlap area between the plates Neutral and Positive (or Negative) can be enlarged, the width w of the conduction cross areas of two plates can be larger in equation (2), so the self-inductances of the busbar can be reduced. Also, with the overlap area between two plates increased, the currents that flow on these plates are in more opposite directions, as shown in Fig. 5(b) and Fig. 6, which means the angle φ in equation (3) is larger, resulting in a lower mutual inductance value. As a result, the total stray inductance in equation (1) is smaller. However, the improvement of the overlap area cannot be achieved by using an integrated laminated bussing structure.

To reduce the parasitic inductance while still satisfying the voltage insulation requirements, the three-dimensional busbar concept is adopted in the enhanced design to fully utilize the z-dimension of the bussing architecture. As shown in Fig. 6, the enhanced design consists of two sets of separated busbars. The busbar on the top is formed by the Neutral, Positive, and Negative plates, which are laminated into a set of two-layer busbar, i.e., Busbar II in Fig. 6. The spacers are used to lift it up, such that the one-layer bussing structure, i.e., Busbar I in Fig. 6, at the bottom formed by Middle1, Middle2 and AC plates can be bolted down to the modules. In this way, spacers in Busbar I are connected to modules without the need to have cutouts on Busbar II.

The cross-sectional view of the two designs is shown in Fig. 7 to highlight the differences. The initial design, with large cutout the metal plates Neutral, Positive, and Negative, have limited overlapping area, especially near the spacers of plate Middle 1 and Middle 2, shown in Fig. 2(b) and Fig. 7(a). Though all metal plates can be integrated into a compact bussing structure in the initial design, the reduction of the overlapping area results in a higher total stray inductance of the busbar due to the reduced magnetic flux cancellation. In comparison, the metal plates in the enhanced design consists of two individual sets of busbars, Busbar I and Busbar II, shown

in Fig. 6 and Fig. 7(b), where the overlapping areas between the plates Neutral and Positive/Negative are significantly increased, resulting in a lower total stray inductance due to the improved negative mutual inductance, according to equation (4) and (6).

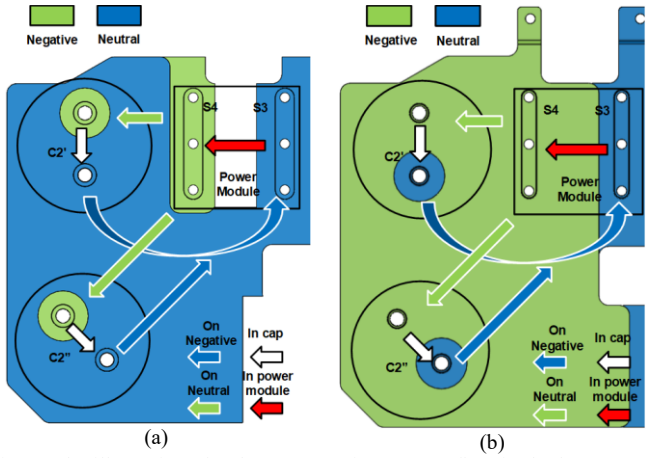


Fig. 5. The illustrations for the commutation current flow in the lower small loop, viewing from the top, (a) in the initial design, and (b) in the enhanced design.

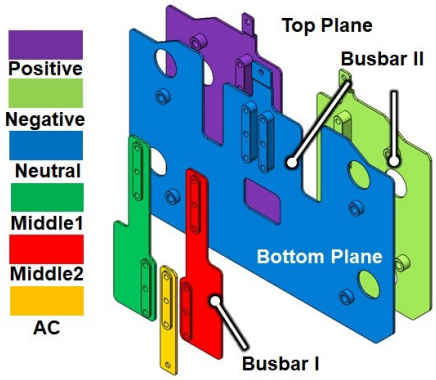


Fig. 6. The the color-coded busbar layers in the enhanced design.

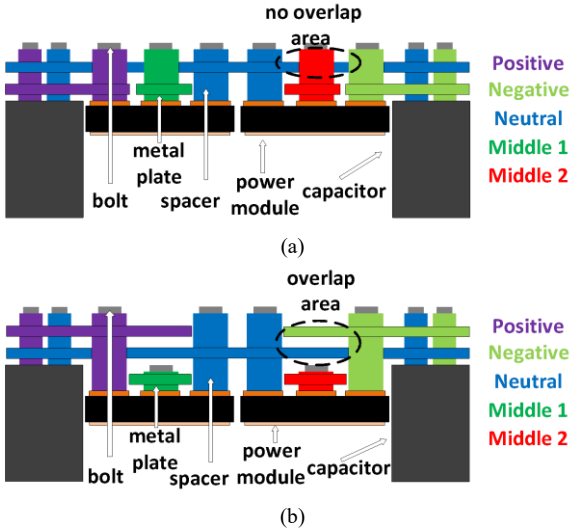


Fig 7. The cross-sectional views of the two design (a) the initial design; (b) the proposed design.

Compared to the initial design, the enhanced busbar design can effectively reduce the total stray inductance. According to the Q3D simulation, the inductances of the busbar on the small and large loops of the enhanced design are 9 nH and 27 nH at 10 MHz, respectively, which represent over 60% and 46% reduction compared to the initial design. The comparison of stray inductances of the two designs is summarized in Fig. 8.

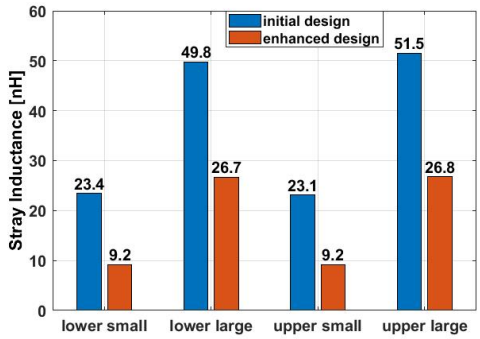


Fig. 8. The Q3D simulation results for the stray inductance of the busbar on all four CCLs at 10 MHz in the (a) initial design and (b) enhanced design.

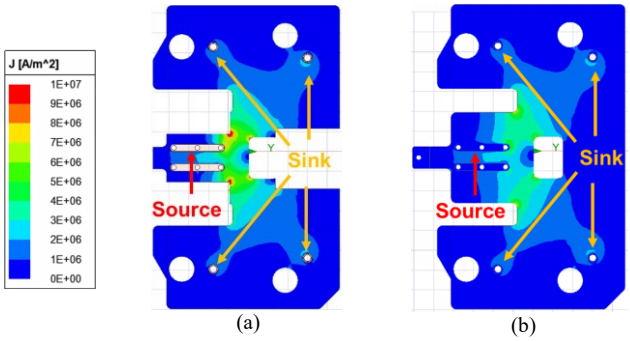


Fig. 9. The simulation results of the current density on the metal plate Neutral using Maxwell for (a) the initial design and (b) the enhanced design.

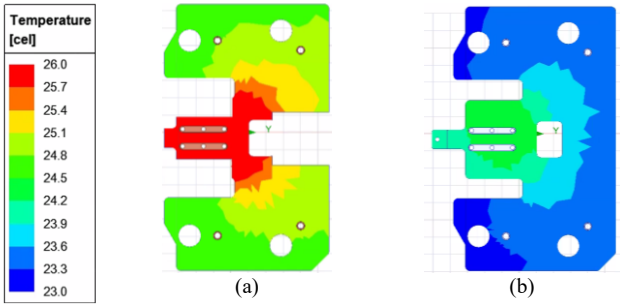
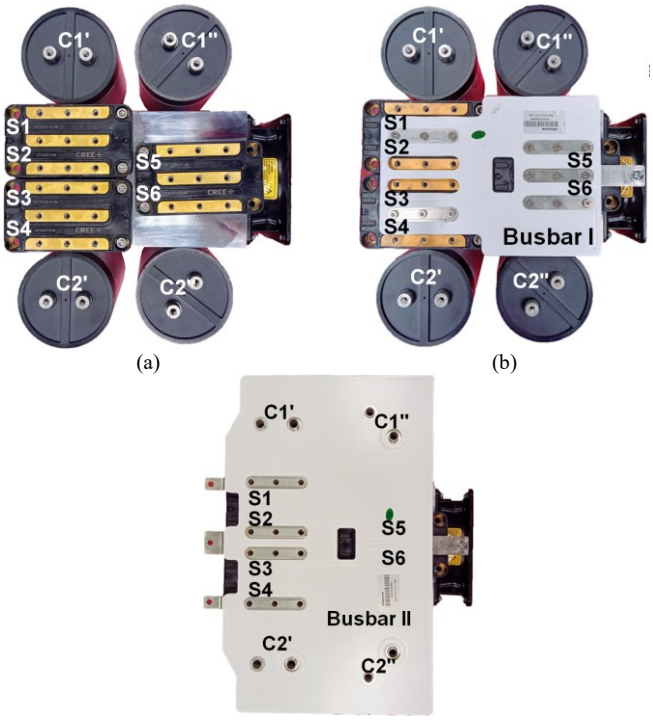


Fig. 10. The simulation results of the temperature rise on the metal plate Neutral using Icepak for (a) the initial design, and (b) the enhanced design.

Besides, the improved geometry of the enhanced busbar design can further reduce the current density and the temperature rise of metal plate Neutral during operation. The current density is simulated based on Maxwell, the results of which are illustrated in Fig. 9. The spacers that connect the power modules are set to be the source with 500 Arms current excitation for the extreme operating condition, and the spacers for the capacitors are the sinks, which are shown in Fig. 9. With wider conduction paths for current, the plate Neutral in the enhanced design has lower current density than the plate in the initial design, especially on

the corner of the plate. Similarly, as shown in the temperature simulation using Icepak, the plate Neutral in the enhanced busbar design is cooler than that of the initial design, illustrated in Fig. 10. As a result, the service life of the enhanced busbar design can be longer than that of the initial design. Also, judging from the simulation results shown in Fig. 10, the temperature of the plate Neutral in the enhanced design is lower than 26 °C when conducting 500 Arms current, which ensures that this plate can satisfy the design specifications.

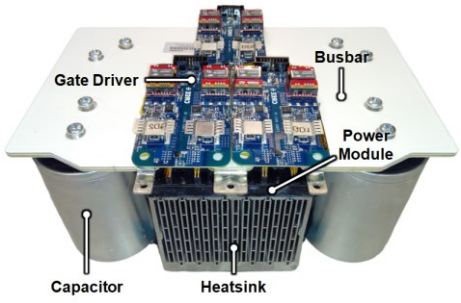
What's more, the initial design is an integrated bussing structure, while the enhanced design consists of two sets of busbars, which may slightly increase the complexity for system assembly. The prototype of proposed ANPC phase-leg using the enhanced busbar design at different stages is shown in Fig. 11, while the picture of the fully assembled ANPC phase-leg building block and the three-phase inverter are shown in Fig. 12.



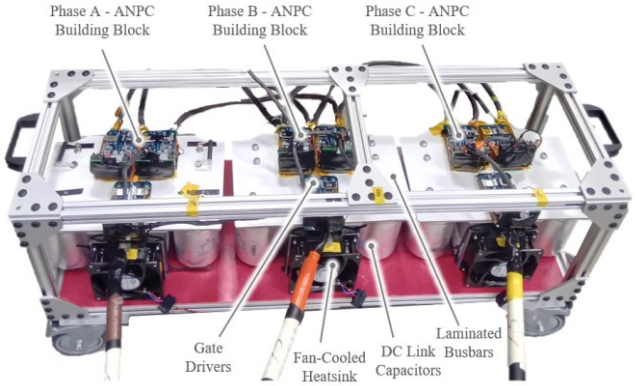
(a) (b)

(c)

Fig. 11. The top view of the ANPC converter during system assembly (a) the arrangement of the capacitors and the power modules of the ANPC converter, (b) with the Busbar I installed and (c) with both Busbar I and II installed.



(a)



(b)

Fig. 12. Pictures of the ANPC converter prototype (a) ANPC phase leg and (b) three-phase ANPC inverter.

III. CCL Stray Inductance Measurement

A. Measurement using Impedance Analyzer

In this work, one of the methods used to measure the stray inductance is an impedance-analyzer-based approach. The Keysight E4990A was used for stray inductance measurement. The results of measured inductance of the busbar and capacitor assembly on the lower small loop and lower large loop are listed in Table II.

As shown in Fig. 13(a), when extracting inductances on the lower small loop, the measured components include the Neutral and Negative plates and capacitors C2' and C2", with the half bridge module excluded in this measurement. As a result, when calculating the total inductance, the measured inductance of the HB module from DC+ to DC- should be added to the measurement result of the lower small loop. The same principle is also applied to the inductance of the lower large loop, where the stary inductance of the busbar and capacitor assembly is extracted, as shown in Fig. 13(c). The measurement setups are shown in Fig. 13(b) and (d) for the inductance extraction of the lower small and large loops, respectively. The inductance of the module, measured from the terminal DC+ to DC- using impedance analyzer, is listed in Table III. With the HB module included, the total stray inductance, based on measurement, for the lower small loop and lower large loop are 27.5 nH and 52.24 nH, listed in Table VIII. With the symmetrical design of the busbar, the stray inductances for the upper and lower CCLs should be the same.

TABLE II
MEASURED INDUCTANCE OF BUSBAR/CAPACITOR ASSEMBLY

Measured Inductance	Result @ 10 MHZ (nH)
Lower small loop	20.52
Lower large loop without S3 connected (Fig.13(c))	45.26
Lower large loop with S3 connected (Fig. 14)	25.77

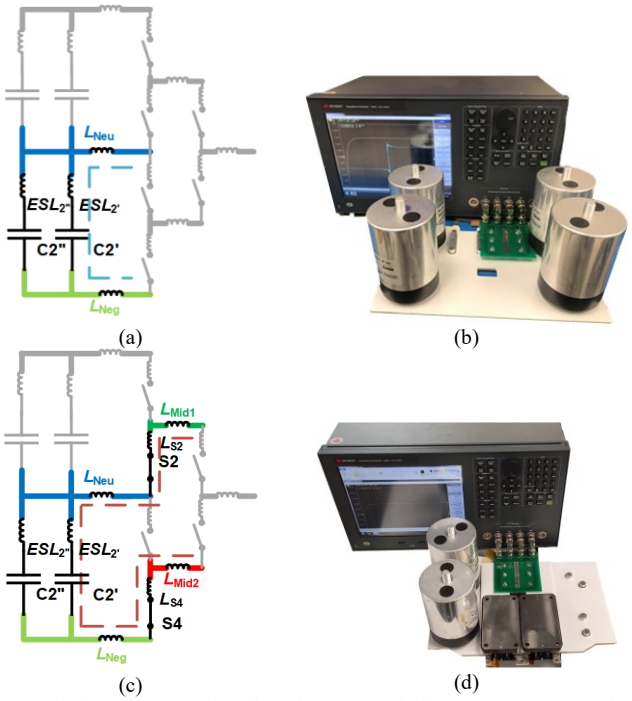


Fig. 13. The impedance analyzer based CCL stray inductance measuremned (a) the equvilant circuit for the lower small loop and (b) the corresponding setup, (c) the equvilant circuit for the lower large loop with S3 disconnected and (d) the corresponding setup.

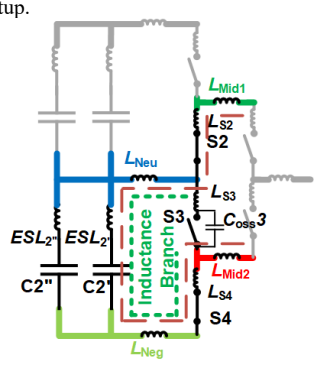


Fig. 14. The equvilant circuit for the lower large loop induatcne measument with S3 (off-state) connected to the busbar, which should be avoided.

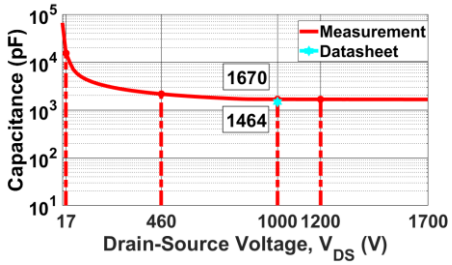


Fig. 15. Measured output capacitance of the power module vs. the value in datasheet.

One thing should be noticed is that, when the lower large loop is measured using impedance analyzer, as shown in Fig. 13(c), the switch S3 should not be connected to the busbar, even when it is in the OFF state, because the output capacitance of S3 can affect the measurement. As shown in Fig. 14, when S3 is physically connected to the busbar, the output capacitor of S3 is connected in parallel with the inductance branch, which contains the inductance of S4, Neutral plate, Negative plate, C2', and C2", leading to reduced impedance of the lower large loop and an increased equivalent inductance. This is especially true when a small DC bias voltage is applied to S3 from the impedance analyzer, results in an output capacitance more than 10 times larger than that at 1000 V rating voltage, as shown in Fig. 15. The output capacitance value (C_{OSS}) of the switch is measured through CV test using B1505A Curve Tracer from Keysight. The measured values under different DC voltage and the value in the datasheet are plotted and listed in Fig. 15 and Table IV.

As shown in Fig. 13(d), the module consists of S3 and S4 is still shown in the setup, since the S4 at ON state should still be physically connected to the busbar, while switch S3 should not be connected to busbar. The output capacitance and the impedance of S3 in the low voltage conditions and the impedance of the impedance branch are listed and calculated in Table IV, and the Appendix, accordingly.

TABLE III
MEASURED MODULE INDUCTANCES

Measured Inductance	Result @ 10 MHz (nH)	Datasheet Value (nH)
HB module from DC+ to DC-	6.98	7 [35]
HB module from DC+ to AC	6.75	N/A
HB module from AC to DC-	7.49	N/A

TABLE IV
OUTPUT CAPACITANCE OF THE DEVICE UNDER DIFFERENT VOLTAGES

C_{OSS} of each device in HB module	Measurement (nF)	Datasheet Value (nF)
1200 V	1.66	N/A
1000 V	1.67	1.46[35]
460 V	2.15	N/A
17 V	15.33	N/A

Fortunately, the S3 in the OFF state does not need to be disconnected from the circuit when doing DPT. The reason is that different from the low voltage measurement condition of the impedance analyzer, the high DC-link voltage is applied to S3 when doing the DPT, such that the low output capacitance of S3 doesn't have substantial impact to the impedance value. The output capacitance and the impedance of S3 in the high voltage conditions are listed and calculated in Table IV, and the Appendix, accordingly.

In addition, besides reading the value from the datasheet, the parasitic inductance from the power module, especially the inductance from each switch, should be measured as well. Normally, the stray inductance of each switch in the HB power module is considered to be half of the inductance of the entire module. However, for the power module used in this work [38], the inductances from terminal DC+ to terminal AC, and from terminal AC to terminal DC-, i.e., the inductances of the top and bottom switches, are not half of the inductance from terminal DC+ to terminal DC-. This discrepancy is mainly due to the mutual inductances between conductors inside the module, which reduces the total inductance of the HB module. As shown

in Table III, only the inductance from terminal DC+ to terminal DC- is available in the datasheet. If the inductance of each switch is estimated as half of the module inductance, it is much lower than the actual value.

B. Stray Inductance Analysis using Simulation

In this work, Q3D simulation is also conducted to extract the stray inductance of the lower small and large loops in the enhanced busbar design, which are 9.2 nH and 26.7 nH at 10 MHz, respectively. To calculate the total parasitic inductance along the CCLs accurately, the measured inductance of the power module in Table IV was used and the inductance of the DC-link capacitors is also measured using impedance analyzer, which 17.32 nH for each capacitor.

For the lower small loop, which consists of two DC-link capacitors in parallel, busbar, and one HB module, as shown in Fig. 1, the inductances of the components, used to calculate the total inductance, are listed in Table V. Since the DC-link capacitors C2' and C2" are in parallel configuration, the factor 0.5 should be used to determine the ESL from the capacitors.

The lower large loop consists of two DC-link capacitors, busbar, one HB, and bottom switches of the other two HB modules, as shown in Fig. 1. The total inductance of this loop is calculated based on the component inductances listed in Table V. The inductances of the lower small and large loops, based on simulation, are 24.84 nH and 57.32 nH, respectively, listed in Table V, and Table VIII.

TABLE V
THE CCL INDUCTANCE CALCULATION USING BUSBAR INDUCTANCE EXTRACTED FROM SIMULATION

CCL	Components	Value	Method
Lower Small Loop Total = 24.84 nH	Busbar	9.2 nH	Q3D Simulation
	0.5 × Capacitor ESL	8.66 nH	Measurement
	Module (DC+ to DC-)	6.98 nH	Measurement
Lower large loop Total = 57.32 nH	Busbar	26.7 nH	Q3D Simulation
	0.5 × Capacitor ESL	8.66 nH	Measurement
	Module (AC to DC-) × 2	14.98 nH	Measurement
	Module (DC+ to DC-)	6.98 nH	Measurement

C. CCL Inductance Calculation using Switching Tests

The total stray inductance [24] in the CCL can be extracted from the oscillation of switching waveforms obtained using double pulse tests (DPT) as

$$L_s = \frac{1}{4\pi^2 f_r^2 C_{oss}} \tag{7}$$

where f_r is the switching oscillation frequency, and C_{OSS} is the output capacitance of the device under test. Usually, the f_r can be approximately derived from the first cycle of the voltage ringing [6], [28], which, however, is normally lower than the oscillation frequency derived from the fast Fourier transform (FFT) of multiple cycles in the voltage ringing. As a result, the frequency extracted from the first cycle leads to an over-estimated stray inductance. According to the results shown in [6], [23], and [28], the calculated inductances based on f_r derived from the first cycle of the rings are more discrepant with the simulation values, compared with the one based f_r derived from the FFT. Therefore, the FFT method to obtain the f_r offers enhanced accuracy. In addition, for the output capacitance of the device under test, measurement is recommended since the actual C_{OSS} value can vary largely versus the operating voltage.

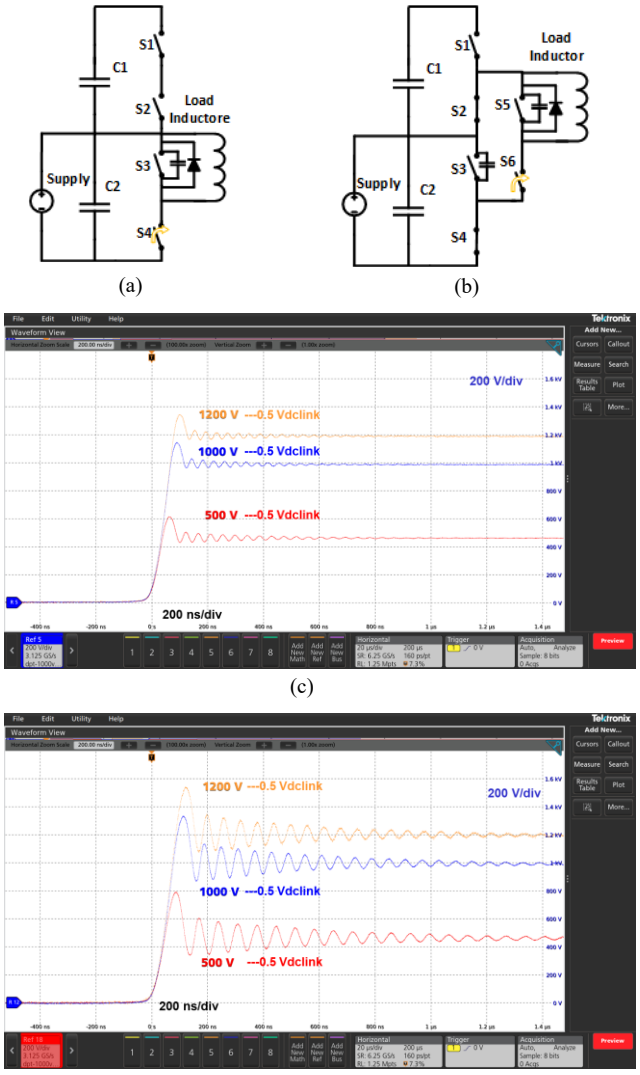


Fig. 16. DPT for ANPC phase leg: test circuits for (a) the small loop and (b) the large loop; (c) and (d) are the corresponding DPT results under different voltages.

The DPT circuits for ANPC phase leg and corresponding experiment waveforms are presented in Fig. 16. In the test for the lower small loop, the switch S4 is switching while S3 is turned off consistently. In the test for the lower large loop, the switch S6 is switching, while S5 is always off. Because the voltage oscillation during device turn-off transient is more obvious than the one in the turn-on transient, only the turn-off waveforms of S3 and S5 are presented. The switching oscillation of S3 is used to calculate the inductance on the small loop while the oscillation of S5 is used for the large one. Because the designed DC voltage for the converter is 2.6 kV listed in Table I, the test voltage for the switch, which is half of the DC link voltage, is up to 1.2 kV. The test conditions of the DPT are 460V 400A, 1000V 400A, and 1200V 400A.The

voltage waveforms in Fig. 16 show that the converter can work properly with 1.2 kV on each switch, with2.4 kV on DC bus.

The frequencies determined using the first cycle of the oscillation for S3 and S5 are 18.49 MHz and 12.87 MHz, and C_{OSS} value at 1000 V is 1.46 nF from the datasheet, shown in Table IV. According to (1), the calculated inductances on the small and large loops are 50.75 nH and 104.74 nH, which are significantly larger than the simulation results and measured results from impedance analyzer.

In contrast, the inductance values based on the f_r extracted using FFT and measured C_{OSS} under 1000V DC bias can be more accurate. With f_r being 25.94 MHz and 16.78 MHz, and C_{OSS} being 1.67 nF, as shown in Fig. 15, the calculated inductances of the small and large loops are 22.54 nH and 53.87 nH, listed in Table VI, which are much close to the simulation and the impedance analyzer measurement. The inductances on the small and large loops based on the proposed extraction method under different DC link voltages are listed in Table VI, considering the variation of C_{OSS} under various voltage listed in Table IV. The Tukey window function and zero padding are applied before doing FFT. The sampling rate of the waveform is 3.125 GB/s. Because the 460 V testing condition deviates significantly from the real operating condition, its results are excluded from the inductance calculation listed in Table VI. One thing that should be also noticed in Table VI is that, thought the extracted oscillation frequencies are identical for 1000 V and 1200 V testing condition, the calculated inductances are different due to the variation of *Coss* under these two DC voltage. The average values of these inductances are listed in Table VI and Table VIII. The voltage overshoot for device S3 and S5 in the DPT is also presented in Table VII. In all the different DC bus voltage, the overshoot is acceptable.

To compare the stray inductance values obtained using three different methods studied in this work, Table VIII summarizes results from impudence analyzer, Q3D simulation results, and extraction from DPT results, which shows good agreement among all three.

TABLE VI
INDUCTANCE CALCULATION USING SWITCHING TEST RESULTS

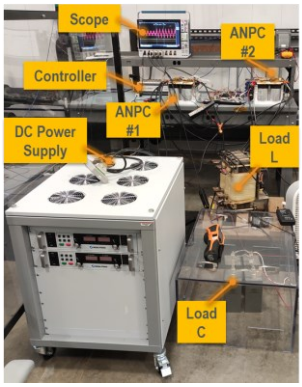
DC Link voltage	f_r of S3 (MHz)	L in small CCL (nH)	f_r of S5 (MHz)	L in Large CCL (nH)
1200 V	25.94	22.68	16.78	54.19
1000 V	25.94	22.54	16.78	53.87
Avg. L value (nH)		22.61		54.03

TABLE VII
VOLTAGE OVERSHOOT IN DPT UNDER DIFFERENT DC BUS VOLTAGE

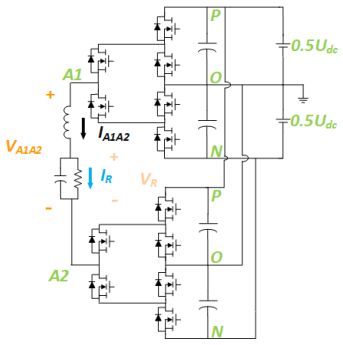
DC Link Voltage	Overshoot for S3	Overvoltage Percent for S3	Overshoot for S5	Overvoltage Percent for S5
1200 V	1343 V	11.92%	1535 V	12.92%
1000 V	1141 V	14.1%	1327 V	32.7%
460 V	612 V	33.13%	789 V	71.16%

TABLE VIII
COMPARISON OF THE EXTRACTED CCL INDUCTANCE BASED ON MEASUREMENT, SIMULATION AND EXPERIMENT.

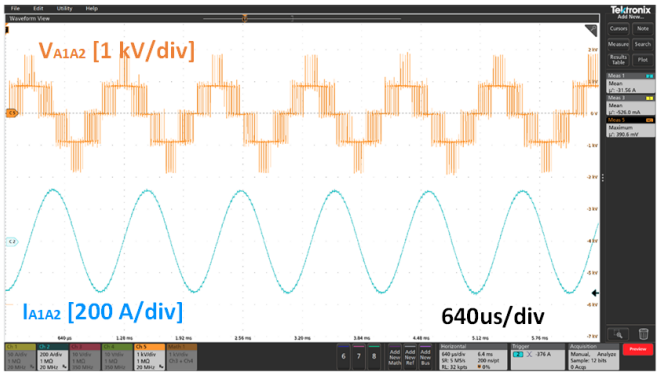
Extraction method	Lower small loop (nH)	Lower large loop (nH)
Impedance Analyzer	27.5	52.24
Q3D Simulation	24.84	57.32
DPT Waveform	22.61	54.03



(a)



(b)



(c)

Fig. 17. Experimental study of the ANPC power stage (a) the test setup of the single-phase pump-back test using two ANPC power stage; (b) the diagram of the single-phase pump-back test; (c) the experimental waveforms of the test

IV. CONVERTER LEVEL EXPERIMENTAL STUDIES

To validate the feasibility of the proposed design and evaluate the performance of the developed prototype, extensive experimental studies were performed. Due to the limitations of the power supplies and load bank, the three-phase continuous power test was performed using 1000V DC bus with load power up to 200kW. To validate the ability to operate at higher voltage and current, the single-phase pump-back test was also performed.

A. High Power Single-phase Pump-back Test

Experimental studies using two back-to-back connected single-phase ANPC power stages are performed to validate the effectiveness of the design under continuous operation. As shown in Fig. 17 (a) and (b), the pump-back test setup using two ANPC power stages to drive the RLC load is performed. The typical result with 1800 V DC bus, SPWM and 0.55 modulation index is shown in Fig. 17 (c). The switching frequency of the SiC MOSFET is 20 kHz, while the line frequency of the output ac is 1000 Hz. The operating power of the converter under this condition is 81.7 kVA. This test demonstrates the operating ability of the converter under MV DC bus voltage and 245 kVA apparent power for a three-phase system.

B. Three-phase Load Test

The continuous operation of the converter is tested with reduced DC link voltage at 1000 V, due to the limitation of the

high power supply in author's testing facility. As shown in Fig. 18(a), three single phase ANPC converters are used to form a three-phase ANPC inverter with output connected to a three-phase resistive load bank. The switching frequency is 20 kHz and the line frequency is 60 Hz. The output power of the three-phase ANPC converter is gradually increased from 50 kW to 200 kW. The efficiency at 200 kW is 98.7% measured the using math function in the oscilloscope. The three-phase line-to-line voltages and load currents at 200 kW are shown in Fig. 18(b), which validates the capability of the converters under high power condition.

V. Conclusion

In conclusion, this paper meticulously presents the design intricacies of a 500 kVA 2.6 kV 3-Level ANPC converter, with a specific emphasis on the power stage and overall prototype performance validations. One key challenge addressed in this work is to optimize the laminated busbar design to meet voltage insulation requirement while minimizing the parasitic inductance, which is essential for SiC converters. Incorporation of the innovative 3D busbar design concept results in a notable 50% reduction in stray inductance compared to conventional laminated busbars. The proposed methods for improving the accuracy of stray inductance extraction through simulation, measurement, and experimentation further enhance the robustness of the design. The successful continuous power test serves as a conclusive demonstration of the operational prowess of the designed converter, validating the effectiveness of the outlined design procedures.

Appendix

The impedance for the opened S3, when the resonant frequency f_s = 10 MHz and DC voltage across the S3 V_{dc} = 1000V, can be calculated as

$$Z_{S3}\,|_{1000V} = 2\pi f_s L_{S3} - \frac{1}{2\pi f_s \cdot C_{OSS}|_{1000V}} = 9.12\Omega$$

where $C_{OSS}|_{1000V}$ = 1.66 nF is the output capacitance of S3 under 1000 V dc bias, and the L_{S3} = 6.75 nH is the stray inductance of the switch S3.

While the impedance for the opened S3, when f_s = 10 MHz and V_{dc} = 17V, can be calculated as

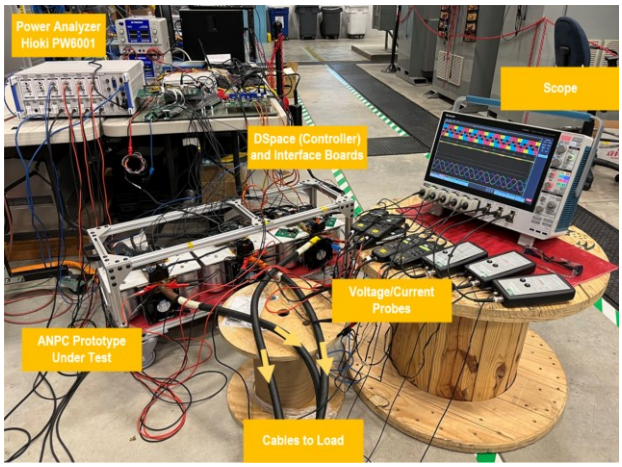
$$Z_{S3}\,|_{17V} = 2\pi f_s L_{S3} - \frac{1}{2\pi f_s \cdot C_{OSS}|_{17V}} = 0.62\Omega$$

where $C_{OSS}|_{17V}$ = 15.33 nF is the output capacitance of S3 under 17 V dc bias.

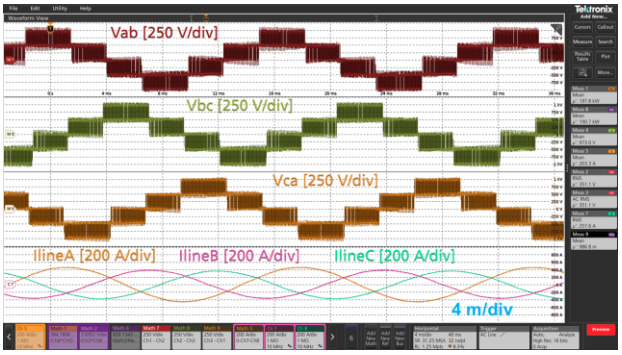
Impedance for the inductance branch, Z_L, when f_s = 10 MHz, can be calculated as:

$$Z_L = \left| 2\pi f_s L_{S4} + 2\pi f_s L_{sm} - \frac{1}{2\pi f_s \cdot C_2} \right| = 1.76\Omega$$

where L_{S4} = 7.49 nH is the stray inductance of the switch S4, L_{sm} = 20.52 nH is the stray inductance of the small loop without S3 and S4, and C_2 = 390 µF is the capacitance of the DC-link capacitor C_2.



(a)



(b)

Fig. 18. Experimental study of the ANPC power stage (a) the test setup of the three-phase test; (b) the experimental waveforms of the 200 kW test.

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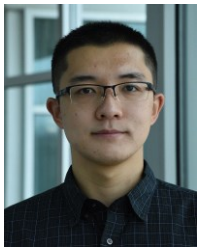

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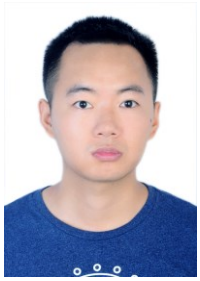

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