An Active Gate Driver Control Scheme for Steady-state Current Balancing of Paralleled SiC MOSFETs

Nan Lin, *Student Member, IEEE*, Ahmad Jaber Radi Al Hmoud and Yue Zhao, *Senior Member, IEEE*

***Abstract*- Silicon carbide (SiC) modules are increasingly adopted in high power applications, where paralleling multiple modules is a common practice to achieve high current carrying capability. This, however, leads to unbalanced current sharing among the paralleled modules. Active gate driver (AGD) can regulate switching behavior of MOSFETs, which has been widely studied to solve the unbalanced current issue among paralleled SiC MOSFETs. An AGD control method targeted at mitigating steady unbalanced current among paralleled SiC MOSFETs is proposed in this brief. The equivalent on-state drain-to-source resistance of paralleled MOSFETs is regulated by applying pulse width modulation (PWM) between two voltage rails in the AGD to compensate parameter mismatches causing steady-state unbalanced current. The proposed AGD can also eliminate the transient unbalanced current by manipulating the delay between the devices in parallel. Comprehensive double pulse tests were conducted to validate the effectiveness of the proposed method. Extensive loss analysis has been performed to highlight the ability of the proposed AGD to achieve evenly loss distribution among modules under different case temperatures and DC bus voltages. The proposed AGD current balancing method is straightforward to implement but was proven to effectively address the current issues among the paralleled SiC modules.**

I. Introduction

Silicon carbide (SiC) MOSFETs are gaining popularity due to their distinctive advantages such as fast switching speed and low switching losses. In high power applications, paralleling multiple modules is a common practice for higher current capability. Due to parameter mismatches among paralleled SiC modules, unbalanced current can often be observed, which leads to over current and/or over temperature issues, thus poses significant challenges to system reliability [1].

Active gate driver (AGD) is an emerging technology to improve the switching performance of power devices [2], which enables its application in current balancing of paralleled SiC MOSFETs. An AGD that can synchronize both current edges and slopes is proposed in [3]. The gate driving current is regulated by voltage-controlled sink and source in [4] to improve the current sharing. Most AGD based current balancing methods only address transient unbalanced current issue [3], [4] since it is believed that the steady state unbalanced currents can be balanced by the positive temperature coefficient (PTC) of SiC MOSFET's drain-to-source on state resistance i.e., R_{ds_on} [4]. However, the steady-state unbalanced current may not be fully balanced by the PTC of SiC MOSFET's R_{ds_on}. This is because that R_{ds_on} of SiC is not as sensitive to temperature as its Si counterpart [5]. In addition, the R_{ds_on} of SiC MOSFET may even show negative temperature coefficient (NTC) when the gate-to-source voltage changes [6]. It is quantitively analyzed in [7] that the PTC effect is limited. The current balancing performance may be compromised if the steady state unbalanced current is not handled properly.

AGD method that can suppress steady state unbalanced currents have also been reported [8]. AGD in [8] uses a buck converter to regulate steady-state gate voltage for current balancing.

There are other methods that can solve the steady-state unbalanced current issue. Device screen may help select devices with the minimum R_{ds_on} mismatch [9]. However, it is time-consuming and requires curve tracer which may not always be available. This cannot suppress the steady state unbalanced current caused by asymmetric circuit layout, which also contributes to steady state unbalanced current and is inevitable in some cases [10]. Inserting differential mode choke can also help suppress steady-state unbalanced current [5], but the complexity of differential choke increases sharply when more than 2 MOSFETs are paralleled.

A novel AGD control method is proposed in this brief to address the steady-state unbalanced current issue by switching gate voltages between two fixed voltage rails using pulse width modulation (PWM). A simple two level AGD output stage circuit is adopted, which can also easily realize gate voltage delay control for transient unbalanced current mitigation. Meanwhile, the method is also generic for multiple modules in parallel.

This brief is organized as follows. Section II presents causes of unbalanced current between paralleled MOSFETs. Section III introduces the proposed AGD control scheme. Section IV presents experimental results and section V concludes this brief.

II. Root Cause Analysis of Unbalanced Current

Parameter mismatch is the major issue that leads to unequal current sharing among the paralleled SiC modules. Unbalanced current can occur during either the switching transient or the steady state. Threshold voltage, i.e., V_{th}, is considered as the major cause of the transient unbalanced current [11]. Unbalanced current during the steady state, i.e., when modules are ON, comes from the impedance mismatch in the power loop, which can be caused by asymmetric layout of the power loop and unequal R_{ds_on} of the paralleled modules.

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All authors are with the Power Electronic Systems Laboratory at Arkansas (PESLA), University of Arkansas, Fayetteville, AR 72701 USA (email: nl005@uark.edu, aalhmoud@uark.edu, yuezhao@uark.edu).

To experimentally study the unbalanced current sharing, in this work, the clamped inductive load (CIL) test with two SiC modules in parallel is performed. The equivalent circuit of the CIL setup is shown in Fig. 1. The devices under test (DUTs) are two randomly selected SiC power modules, i.e., M_1 and M_2, Microchip MSCSM170AM058CT6LIAG. Using a curve tracer (Keysight B1505a), the values of V_{th} and R_{ds_on} of two modules samples at different virtual junction temperatures are extracted and plotted in Fig. 2, where both R_{ds_on} and V_{th} mismatches can be observed.

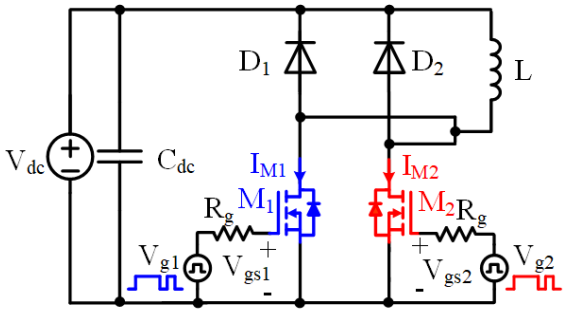


Fig. 1. The equivalent circuit of the CIL setup with 2× modules in parallel.

Fig. 3 shows a typical CIL test result, including the gate-to-source voltages, i.e., V_{gs}, and the corresponding current waveforms for M_1 and M_2, which are triggered by identical gate signals, i.e., V_g, using conventional gate driver (CGD) control. Since the V_{th} of M_1 is lower than that of M_2, the current of M_1, i.e., I_{M1} rises earlier and faster than the current of M_2, i.e., I_{M2}, as shown in the zoomed-in portion in Fig. 3. Due to the R_{ds_on} mismatch, the steady-state unbalanced current can also be observed when both modules are fully turned on. I_{M1} is higher than I_{M2} during the steady state because of the lower value of $R_{ds\_on\_M1}$.

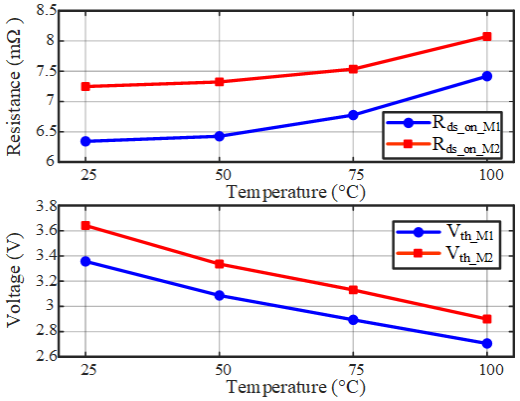


Fig. 2. Curve tracing data of two SiC module samples.

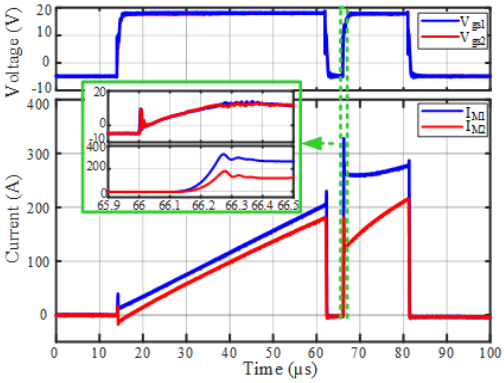


Fig. 3. CIL test waveforms of M_1 and M_2.

III. Proposed AGD Control Scheme for Steady-State Current Balancing

The R_{ds_on} of a MOSFET [12] can be deduced from its output characteristics as:

$$R_{ds\_on} = \frac{V_{ds}}{I_{ds}} = \left(\frac{\beta}{2} \left(2\left(V_{gs} - V_{th}\right) - V_{ds} \right) \left(1 + \lambda V_{ds}\right) \right)^{-1} \quad (1)$$

where $\beta = \mu_n C_{ox} W/L$, μ_n is the charge-carrier effective mobility, C_{ox} is the capacitance of the oxide layer, L is the channel length, W is the channel width, and λ is the channel length modulation parameter. β *and* λ can be extracted by curve fitting as described in [13].

It can be inferred from (1) that R_{ds_on} can be regulated by V_{gs}, which makes it feasible to mitigate steady-state unbalanced current caused by R_{ds_on} mismatch. To regulate the V_{gs}, a straightforward way is to introduce an additional controllable voltage source in the gate driver [8], which increases complexity of the system. Therefore, this work proposes a PWM based gate voltage regulation method implemented in the AGD architecture in Fig. 4.

As shown in Fig. 4, an FPGA controller serves as the local controller to process the command from the main controller and drives the output stage circuit. The output stage of the AGD adopts a simple circuit with only two gate driver ICs. Although a more complicated AGD output stage circuit usually brings better controllability, it is verified in this work that a good overall current balancing can also be achieved with the help of the proposed AGD control method.

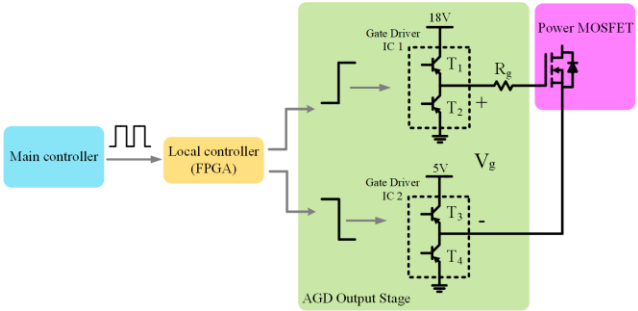


Fig. 4. Diagram of the AGD architecture.

As shown in Fig. 5, four gate voltage levels can be generated using two gate driver ICs, where the potential of both the gate and source terminals of the switch can be controlled. The voltage level is determined using a simple

logic signals input to the gate driver ICs. For example, T_1 and T_4 are turned on in mode a as indicated by the red traces, so that the gate terminal of the power MOSFET is connected to the 18 V voltage rail while the source is connected to the ground. The actual gate voltage for this mode, i.e., V_{g_a}, is the voltage difference between the gate and source terminals. Three other modes can be configured in a similar way to realize different gate voltage levels. The proposed AGD architecture utilizes two voltage rails, i.e., 18 V and 5 V in this work, to generate four different gate voltage values while maintaining a very simple design with low part count, and seamless transition between operating modes.

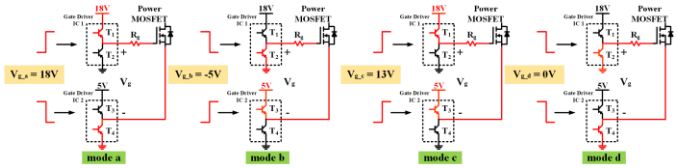


Fig. 5. Operating principle of the AGD.

The effectiveness of the proposed method is firstly verified using simulation, with the typical waveforms of the gate voltage PWM regulation method shown in Fig. 6 based on the circuit in Fig. 1, where the R_{ds_on} of M_2 is set to be 20% higher than that of M_1. Gate voltage of M_1 is only regulated during the second pulse to address the steady-state unbalanced current.

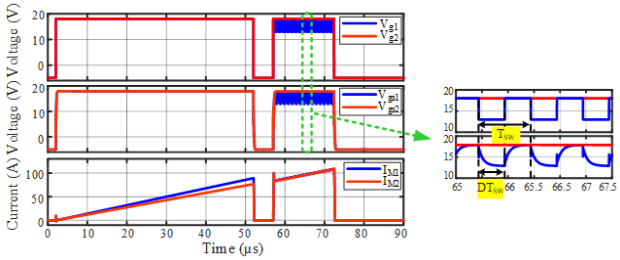


Fig. 6. Steady-state unbalanced current suppression by PWM regulation.

As shown in Fig. 6, gate voltage of M_1, i.e., V_{g1}, is regulated by a PWM signal switching between 18 V and 13 V during the second pulse, to increase its equivalent R_{ds_on}. Meanwhile, gate voltage of M_2, i.e., V_{g2}, is kept at 18 V during the same period. Since no voltage regulation is applied during the first pulse, the steady-state unbalanced current exists due to R_{ds_on} mismatch. With the gate voltage PWM regulation on M_1, two MOSFETs show good current sharing during the second pulse.

Utilizing the AGD structure in Fig. 5, it is possible to switch between two positive voltage levels, i.e., V_{g_a} and V_{g_c}, through the gate driver ICs. Therefore, if the gate voltage is switched between the two voltage levels for a certain period during the steady state, as shown in the top subfigure of Fig. 6, it results in an equivalent V_{gs} that can be regulated by the duty ratio of V_{g_c}, which regulates the equivalent R_{ds_on}.

Due to the existence of gate resistance and MOSFET input capacitance, V_{gs} keeps charging and discharging the capacitance over a PWM cycle, as shown in the middle subfigure of Fig. 6. The V_{gs} during a PWM cycle can be expressed as:

$$\begin{cases} V_{gs} = V_{g\_c} + \left(V_{g\_a} - V_{g\_c}\right) e^{-\frac{t}{C_{iss} R_g}} \ (0 < t < DT_{sw}) \\ V_{gs} = V_{g\_a} + \left(V_{g\_c} - V_{g\_a}\right) e^{-\frac{t}{C_{iss} R_g}} \ (DT_{sw} < t < T_{sw}) \end{cases} \tag{2}$$

where C_{iss} is the MOSFET input capacitance, R_g is the gate resistance, D is duty ratio of V_{g_c}, T_{sw} is the switching period of PWM gate voltage. Based on (2), the equivalent V_{gs}, i.e., V_{gs_eq}, can be calculated as (3) and equivalent R_{ds_on} can be determined using (1) and (3) as:

$$R_{ds\_on\_eq} = \left(\frac{\beta}{2} \left(2\left(V_{gs\_eq} - V_{th}\right) - V_{ds} \right) \left(1 + \lambda V_{ds}\right) \right)^{-1} \tag{4}$$

As for the selection of the two positive voltage levels in the AGD, the $R_{ds\_on\_eq}$ can be regulated by D according to (3) and (4). The maximum $R_{ds\_on\_eq}$, i.e., $R_{ds\_on\_eq\_max}$, provided by the AGD can be calculated from (4) when D=1. To ensure the designed AGD hardware has enough control capability, the $R_{ds\_on\_eq\_max}$ should be larger than the maximum R_{ds_on} in datasheet. This can be used to verify the design of the two voltage levels V_{g_a} and V_{g_c}.

Since the AGD can be equivalent to a RC circuit when controlled in switched between two gate voltage levels during steady state, the switching period should be larger than the time constant to have enough gate voltage change as shown below:

$$T_{SW} > R_g C_{iss} \tag{5}$$

To ensure a good dynamic performance and reduce the current ripple introduced by the gate voltage PWM regulation, T_{sw} should be much smaller than the width of the current pulse it regulates.

It should be noted that the proposed method switches the AGD in high frequency during the steady state, so there is no high di/t or dV/dt through the device, which are the causes of gate voltage oscillation [14]. This is also verified by the test waveforms in the next section.

IV. Experimental Verification

An experimental test setup based on Fig. 1 is developed to validate proposed the AGD concept, a picture of which is shown in Fig. 7. Fig. 8(a) shows the busbar used in the test, which can have three modules in parallel in total. The parasitic inductance and resistance are analyzed in Ansys Q3D, which shows little mismatch among the three power loops. A picture of the AGD output stage board is shown in Fig 8(b).

$$V_{gs\_eq} = \frac{1}{T_{SW}} \int_0^{T_{sw}} V_{gs} dt = \frac{1}{T_{SW}} \left(\left(V_{g\_c} - V_{g\_a}\right) \left(DT_{SW} + 2R_g C_{iss} e^{-\frac{DT_{SW}}{R_g C_{iss}}} - R_g C_{iss} \left(1 + e^{-\frac{T_{SW}}{R_g C_{iss}}} \right) \right) + V_{g\_a} T_{SW} \right) \tag{3}$$

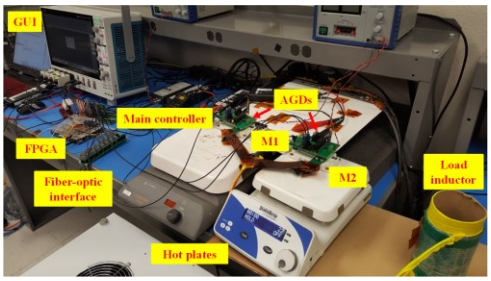
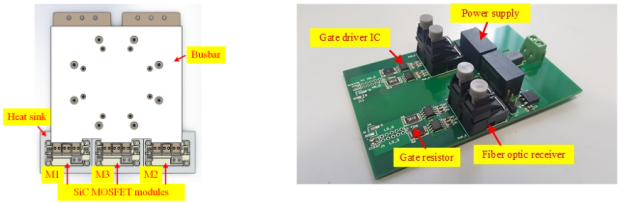


Fig. 7. A picture of the test setup.



(a) (b)

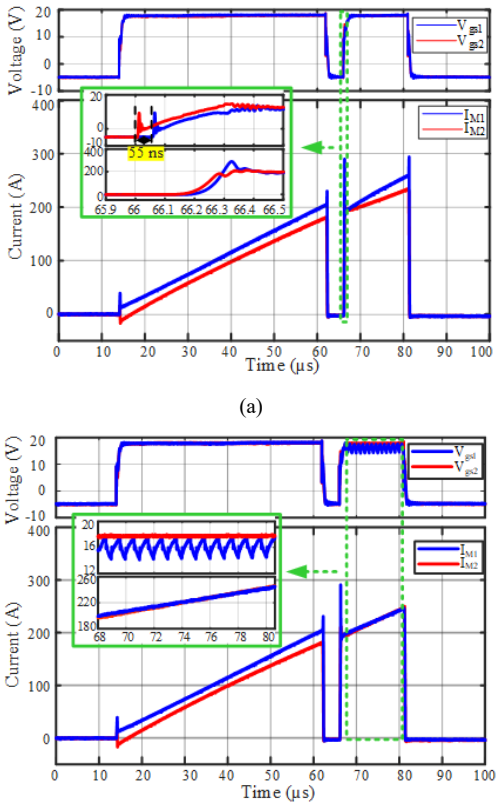
Fig. 8. Figures for (a) Busbar. (b) AGD board.

The bottom switches in the two SiC modules are paralleled as DUTs. The top switches are turned off with body diodes used as freewheeling diodes. The middle points of the two modules are connected to a 40 µH air core inductor. Each module is placed on a dedicated hot plate to control its case temperature. A Xilinx FPGA board is used as the local controller to generate gate signals for the DUTs.

Fig. 9 shows CIL test results with the proposed AGD at room temperature, while the results using CGD control on the same setup were shown in Fig. 3.

Curve tracing data in Fig. 2 shows V_{th} mismatch and transient unbalanced current is observed in Fig. 3. Gate voltage of M_1 is first controlled to be 55 ns lagging behind M_2 by the AGD FPGA controller, so that the two currents reach the same value at the end of turn-on period as shown in Fig. 9(a). This transient unbalanced current suppression method is easy to implement and has been validated in previous AGD based current balancing method [15].

To suppress the remaining steady-state unbalanced current during the second pulse in Fig. 9(a), the gate voltage PWM regulation is applied on M_1 during the second pulse in Fig. 9(b) while using the same time delay adopted in Fig. 9(a). The switching frequency of the PWM pulse is 1 MHz with the 40% duty ratio. The two gate voltage levels in the PWM regulation are 18 V and 13 V. I_{M1} and I_{M2} are on top of each other during the second pulse thanks to the gate voltage PWM regulation. Since the switching period is much smaller than the second current pulse, there is little current ripple introduced by the gate voltage PWM regulation as observed from Fig. 9(b).



(a)

(b)

Fig. 9. CIL test waveforms of two paralleled modules with (a) only V_g delay regulation and (b) both V_g delay and V_g PWM regulations.

To further validate the effectiveness of the proposed AGD control method on loss balancing across the paralleled modules, CIL tests are conducted at various bus voltage and load current conditions at 25 °C. Fig. 10 shows loss data with 800 V bus versus different total load currents from the two paralleled modules. The top two subfigures present loss data of the two MOSFETs tested using CGD and AGD control, respectively. The bottom subfigure shows total loss of the two paralleled MOSFETs using CGD and AGD control, respectively. When CGD control is adopted, the loss of M_1, i.e., E_{1_CGD}, is almost twice of the loss of M_2, i.e., E_{2_CGD}, due to the large difference in both conduction and switching losses, which are represented by dark and light shaded areas in each bar chart. The numerical data for each loss as well as the total loss for each MOSFETs are marked in Fig. 10. When AGD control is adopted, as shown in the middle subfigure in Fig. 10, losses of the two MOSFETs, i.e., E_{1_AGD} and E_{2_AGD} are much more balanced since both conduction and switching losses of the two MOSFETs have close values. In the bottom subfigure of Fig. 10, the total loss of the two MOSFETs using CGD control, i.e., E_{total_CGD} is close to the total loss using AGD control, i.e., E_{total_AGD}. This implies that the proposed AGD concept does not introduce additional loss while balancing the loss distribution between the two MOSFETs. The numerical data for the total losses for the two paralleled MOSFETs are marked in different colors in the bottom subfigure.

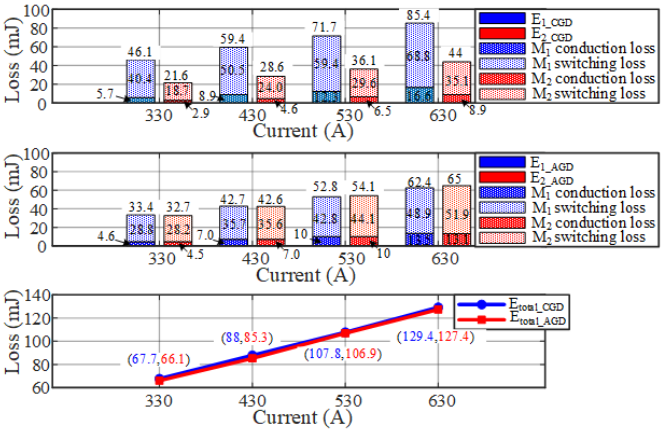


Fig. 10. Loss analysis of paralleled MOSFETs with DC bus voltage at 800 V.

To further verify the robustness of proposed AGD method against temperature variation, loss data at different module case temperatures are shown in Fig. 11. The numerical data for each loss as well as the total loss for each MOSFETs are marked in Fig. 11. Similar to the data shown in Fig. 10, the AGD method realizes balancing loss sharing while remaining similar total loss to the CGD method.

A third module, M_3, is parallel connected with M_1 and M_2 at the position in Fig. 8(a) to validate the proposed AGD method with multiple paralleled modules. The V_{th} and R_{ds_on} of M_3 at 25 °C are 3.37 V and 6.47 mΩ, respectively. CIL test result of the three modules using CGD control is shown in Fig. 12(a). The proposed AGD method is applied on the second pulse, which suppresses both transient and steady-state unbalanced currents, as shown in Fig. 12(b). The current of M_2 is used as the reference for both transient and steady-state unbalanced current control to the currents of the other two modules.

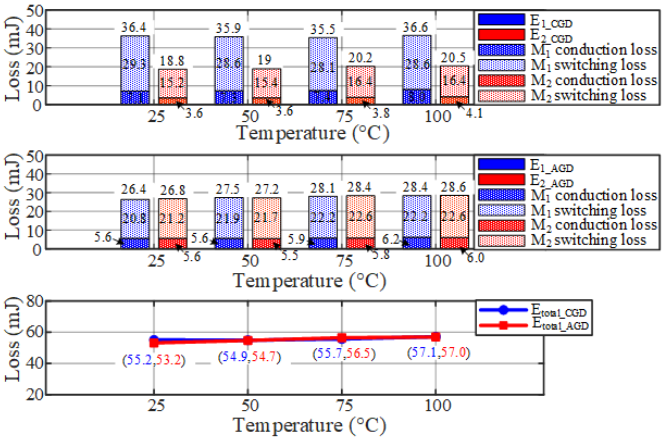
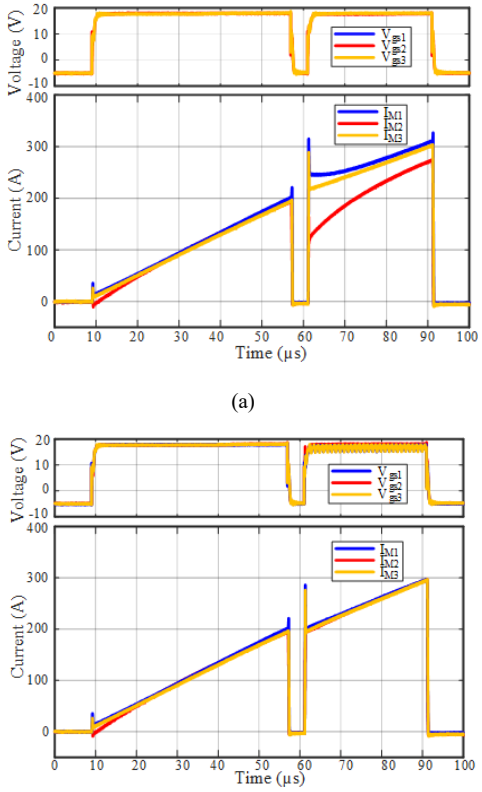


Fig. 11. Loss analysis of paralleled MOSFETs at different temperatures.



(a)

(b)

Fig. 12. CIL test waveforms of three paralleled modules using (a) CGD control. (b) proposed AGD control.

V. Conclusion

An AGD control scheme for suppressing steady state unbalanced current is proposed in this brief. The gate voltage is controlled in PWM to regulate the equivalent R_{ds_on} of paralleled SiC MOSFETs for current balancing. The proposed method is realized by a simple AGD output stage circuit, which can also be integrated with gate voltage delay control for transient unbalanced current mitigation. Experimental test results have verified that the proposed AGD method is effective at various working conditions and is robust to temperature variation. Test results also show the balanced loss sharing without total loss penalty on the paralleled MOSFETs. In addition, the proposed method has been verified for multiple modules in parallel.

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