A Megawatt-Scale Si/SiC Hybrid Multilevel Inverter for Electric Aircraft Propulsion Applications

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***Abstract*- This paper presents the design and development of a megawatt-scale medium-voltage (MV) hybrid inverter prototype to validate its feasibility and potentials for the electric propulsion on the next-generation electric aircraft system with an onboard MV dc distribution, e.g., 3 kV dc bus in this work. The proposed hybrid converter consists of a three-level active-neutral-point-clamped (ANPC) stage using 3.3 kV silicon IGBTs cascaded with an H-bridge stage using cost-effective 1.2 kV SiC MOSFETs in each phase. Comprehensive design and evaluation of the full-scale prototype are elaborated, including the low-inductance busbar design, converter architecture optimization and system integration. In addition, a low computational cost space vector modulation with common-mode voltage (CMV) reduction feature is proposed to fully exploit the benefits of SiC MOSFET in this hybrid topology. Extensive simulation and experimental results are provided to demonstrate the performance of each power stage and the full converter assembly in both the steady-state operation and variable frequency operations. Compared with the widely adopted IGBT based ANPC converter in MV applications, the proposed 7-L hybrid inverter system features higher power efficiency, reduced harmonics, higher dc voltage utilization, reduced CMV and lower dv/dt, while remains cost effective compared to the solution using MV SiC MOSFETs.**

***Index Terms*—Electric propulsion, medium voltage, multilevel inverter, silicon carbide MOSFETs.**

I. Introduction

More-electric aircraft (MEA) and all-electric aircraft (AEA) technologies [1]-[3] have received more and more attention in the aviation industry, aiming at achieving better flight experience, higher fuel efficiency, lower maintenance and reduced carbon footprint. However, stepping from the traditional fossil fuel-oriented propulsion system towards the electrical counterpart is still a challenging task since it could involve tremendous modifications to the system architecture and re-designs of the airborne electric power generation, storage, distribution, and conversion [4].

Nowadays, novel architectures and concepts of multiple electric propulsion systems have been introduced by various manufacturers and research institutes worldwide, such as Boeing, Airbus, NASA, Rolls-Royce, and ESAero [5]. In commercial airliners, the low voltage distribution is a mature candidate at the present time. For instance, the Boeing 787 with approximately 1 MW onboard electric power generation capability adopts 115-235 VAC, ± 270 VDC to distribute power for auxiliary onboard electrical power systems, such as HVAC, actuators, avionics, air conditioner and de-icing [2], [3]. Due to the use of low voltage distribution for such a large amount of power, the high amount of current is inevitable results in more copper for wiring cores, connectors and resultant power losses, thereby increasing the weight of the aircraft and degrading the overall efficiency In contrast, the use of medium-voltage (MV) dc distribution is a long-term solution for the next-generation electric aircraft, which can leverage lightweight and high efficiency for new aircraft design. For example, a 3 kV MV dc distribution was selected for Airbus's E-Fan X and was tested in 2021 [6], whose one of the four jet engines was replaced by a 2 MW electric fan powered by a 2.5 MW Rolls-Royce AE 2100 Engine. In 2030, NASA will launch a new design with 1 kV MV dc distribution, named STARC-ABL, in which an electric-propulsion motor is installed at the rear of the aircraft. By 2050, N3-X turbo-electric aircraft with the cutting-edge superconducting technologies, also developed by NASA, will be equipped with ± 2 kV dc distribution system. Therefore, the evolutions of the onboard MV dc electric power system are expected to gain momentum in the development of future aircraft and bring foreseeable advancements for transportation electrifications.

To make it compatible with the MV dc bus, the MV inverters should be comprehensively investigated for the high

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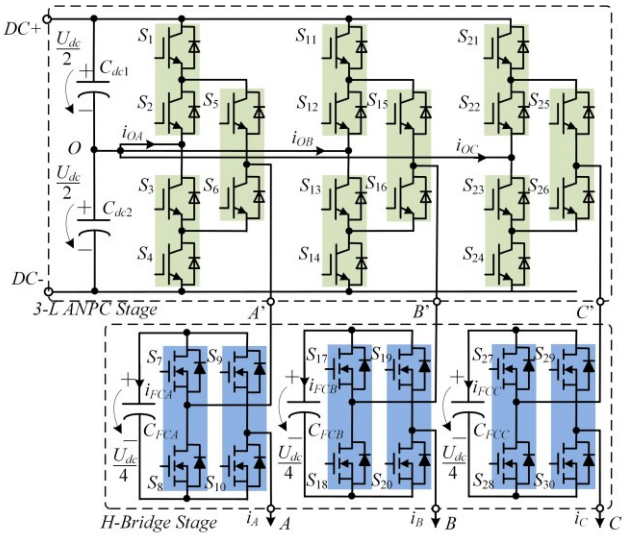


Fig. 1. Topology of the 7-L ANPC-H converter.

TABLE I.
7-L ANPC-H CONVERTER PARAMETER SPECIFICATION

Parameter	Description
dc link voltage	3 kV
H-bridge capacitor voltage	750 V
3.3 kV IGBT Module	FF450R33T3E3
3.3 kV SiC MOSFET Module	Cree 3.3kV XHV-7
1.2 kV SiC MOSFET Module	CAS325M12HM2
Voltage stress of switches in ANPC	1.5 kV
Voltage stress of switches in HB	750 V
Rated designed power	1 MVA
Operating fundamental frequency	Up to 1 kHz
Switching frequency	20 kHz
ANPC floating capacitor	293 μF
H-bridge floating capacitor	390 μF

power-density electric propulsion systems in the MEA or AEA. Compared with the conventional two-level counterpart [7], the multilevel power converters [8], [9] have lower harmonics in the ac output voltage, lower device voltage stress, dv/dt, electromagnetic interface (EMI) emissions and the potential to reduce the common-mode voltage (CMV) [10], [11] which causes motor shaft current and put bearing insulation at risk, thereby threatening electric motor lifetime. In the light of these advantages, three-level (3-L) topologies have already been demonstrated for aerospace applications with low voltage dc bus, such as T-type [12], [13], neutral point clamped (NPC) [14]-[16], active neutral point clamped (ANPC) converters [17]-[19]. Among the 3-L converters for propulsion applications in the literature, dc bus voltage was up to 2.4 kV [17]-[19] with improved converter power density and efficiency. However, high dv/dt caused EMI issue could prevent 3-L converter from operating with higher dc bus voltage, otherwise additional heavy dv/dt filter and/or EMI filter [18], [19] should be carefully designed for system noise immunity. To address the issues, the topologies with a higher number of output voltage levels become a trend [20], such as five-level (5-L) [21], [22] and seven-level (7-L) converters [23]-[26], etc. Among them, the hybrid converters with cascaded floating H-bridge (HB) structure are attractive solutions due to their voltage boost capability, such as the T-type converter cascaded with HB, i.e., 7-L T^2-H converter [25], and ANPC converter cascaded with HB, i.e., 7-L ANPC-H converter [26]-[28]. When comparing the 7-L ANPC-H with T^2-H converter, the ANPC-based hybrid converter has the advantage of lower voltage stress across power devices and balanced loss distributions. Although the 7-L topologies have been reported, especially from the perspectives of control and modulation methods, to best of authors' knowledge, no proposal have been presented to study the feasibility of using the 7-L converter for MV propulsion applications. To bridge this gap, in this work, a MW-scale 7-L hybrid converter prototype, which consists of a Si IGBT based ANPC and SiC HB substages, is developed with a feasibility demonstration for MV aerospace motor drive applications.

More specifically, this paper presents the design and development of a 1 MVA hybrid 7-L converter prototype with a 3 kV dc bus for next-generation electric aircraft propulsion. The low-inductance and high current busbar design for ANPC power stage using 3.3 kV silicon IGBTs and/or silicon carbide MOSFETs, and the HB power electronics building blocks (PEBB) using 1.2 kV SiC MOSFETs are comprehensively discussed and validated through the MV tests. Recently, due to a significant volume increase of the low-voltage SiC devices, mainly driven by the booming of the vehicle market, the use of 1.2 kV SiC MOSFETs in this design is cost effective, while still enabling various advantages of the 7-L MV converter. In addition, a computationally efficient space vector modulation (SVM) scheme with CMV reduction is also presented. Simulation and experimental results are given to validate the 7-L hybrid converter prototype with successfully operating over a wide range of output fundamental frequency, e.g., 60 Hz, 400 Hz and 1 kHz, for MV aircraft electric propulsion systems. Furthermore, a detailed comparison among the state-of-the-art Si and SiC based multi-level inverter topologies is presented to highlight advantages of the hybrid multilevel inverter studied in this work.

II. Power Stage Design and Implementation

A. System Overview

Fig. 1 shows the circuit configuration of the 7-L ANPC-H converter, which consists of two cascaded power stages, i.e., three-level (3-L) ANPC stage implemented by 3.3 kV Si and/or SiC power switches and H-bridge stage implemented by 1.2 kV SiC power switches. Table I lists the overall parameter specification. Assuming the ANPC has a balanced dc link with a total dc link voltage as U_{dc}, the voltage across the two series connected capacitors C_{dc1} and C_{dc2}, which are also called floating capacitors, are both $U_{dc}/2$. The ANPC phase-leg can generate three voltage levels, i.e., $-U_{dc}/2$, 0 and $U_{dc}/2$, with respect to the neutral point O. In each H-bridge converter, the dc voltage across its floating capacitor is regula-

TABLE II.
GATE SIGNALS AND FC CHARGE/DISCHARGE STATE FOR ALL THE SWITCHING STATES

Path	State	u_a	i_a	u_{FC}	u_{dc1}	u_{dc2}	$S_1S_3S_5S_7S_9$ ($\bar{S}_2\bar{S}_4\bar{S}_6\bar{S}_8\bar{S}_{10}$)
i	6	$3U_{dc}/4$	+ –	↓ ↑	* *	* *	11101
ii	5	$U_{dc}/2$	+ –	* *	* *	* *	11111
iii	5	$U_{dc}/2$	+ –	* *	* *	* *	11100
iv	4	$U_{dc}/4$	+ –	↑ ↓	* *	* *	11110
v	4	$U_{dc}/4$	+ –	↓ ↑	↑ ↓	↓ ↑	00101
vi	4	$U_{dc}/4$	+ –	↓ ↑	↑ ↓	↓ ↑	11001
vii	3	0	+ –	* *	↑ ↓	↓ ↑	00111
viii	3	0	+ –	* *	↑ ↓	↓ ↑	11011
ix	3	0	+ –	* *	↑ ↓	↓ ↑	00100
x	3	0	+ –	* *	↑ ↓	↓ ↑	11000
xi	2	$-U_{dc}/4$	+ –	↑ ↓	↑ ↓	↓ ↑	00110
xii	2	$-U_{dc}/4$	+ –	↑ ↓	↑ ↓	↓ ↑	11010
xiii	2	$-U_{dc}/4$	+ –	↓ ↑	* *	* *	00001
xiv	1	$-U_{dc}/2$	+ –	* *	* *	* *	00000
xv	1	$-U_{dc}/2$	+ –	* *	* *	* *	00011
xvi	0	$-3U_{dc}/4$	+ –	↑ ↓	* *	* *	00010

ted as $U_{dc}/4$, which leads to three possible output voltage levels for the H-bridge converter, i.e., $-U_{dc}/4$, 0, $U_{dc}/4$. Due to the cascaded structure, there are 7 possible output voltage levels, which are corresponding to 7 switching states, at the ac output terminal of each phase-leg in the hybrid 7-L converter. The switching states of phase A, B and C are defined as S_A, S_B, S_C = 0, 1, …, 6, and the corresponding output line to neutral, i.e., V_{AO}, voltage levels are $-3U_{dc}/4$, $-U_{dc}/2$, $-U_{dc}/4$, 0, $U_{dc}/4$, $U_{dc}/2$, $3U_{dc}/4$, respectively.

The gate signals and the dc floating capacitors charge/discharge state of the 7-L ANPC-H converter, using phase A as an example, during all the switching states with different phase current polarities are summarized in Table II, where + stands for the instantaneous ac current flows out from phase-leg to the load, and vice versa; ↑, ↓, and * stand for the floating capacitor charging, discharging and bypass, respectively. There are 16 conduction paths, i.e., i – xvi, for the seven switching states, where switching states 1 to 5 have redundant conduction paths.

The 3-L ANPC converter could achieve devices loss or junction temperature balancing. Because ANPC commutation between output $-U_{dc}/2$ and 0, and commutation between output $U_{dc}/2$ and 0, have multiple redundant paths [31]. Based on commutation paths of 7-L ANPC-H converter, its inner A-NPC stage could also have multiple redundant paths for commutations between its output $-U_{dc}/2$ and 0, and between $U_{dc}/2$ and 0. Hence, the ANPC stage inside 7-L ANPC-H converter could also have devices loss balancing capability, which is not investigated in this work.

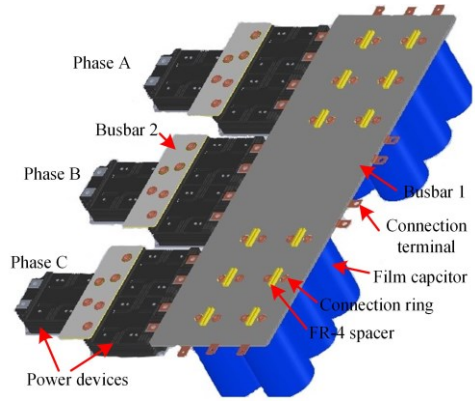


Fig. 2. The designed 3-L ANPC stage.

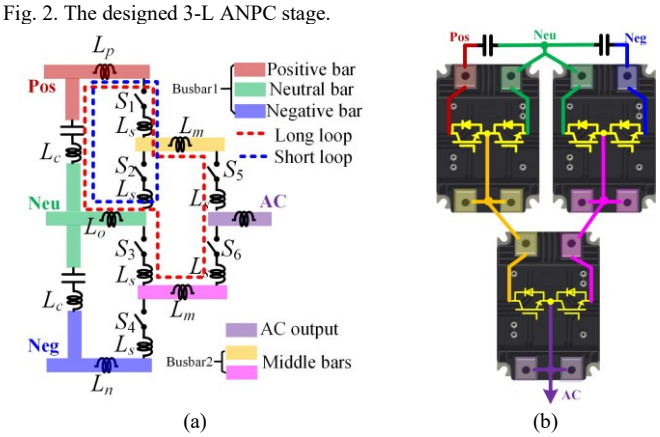


Fig. 3. (a) diagram and (b) power module placement in an ANPC phase-leg.

B. ANPC Power Stage Design

A 3D rendering for the proposed 3-phase ANPC design is shown in Fig. 2. The per phase equivalent circuit considering the stray inductance in the current commutation loop (CCL) is illustrated in Fig. 3(a). As shown in both figures, the busbar 1 consists of three conductive copper layers, i.e., dc positive, neutral and dc negative ("Pos", "Neu" and "Neg", respectively), while busbar 2 consists of two copper layers. The arrangement of the power modules in each phase leg is shown in Fig. 3(b), which considers the layout symmetry, total footprint, and the parasitic inductance in the multiple CCLs for an ANPC. The power modules used in 3-L ANPC power stage are Infineon 3.3 kV half bridge IGBT modules XHP-3 package and/or Cree 3.3 kV half bridge XHV-7 [32] SiC MOSFET modules. Noted that the adopted 3.3 kV Si and SiC modules have the same power terminals definition and dimensions.

On the dc link, twelve 1.5 kV 195 μF film capacitors DCP6S06195E000 from WIMA are adopted to form the dc link capacitor bank on the busbar 1. The arrangement of the 12 capacitors is optimized to achieve lower stray inductance, meet the required capacitance, and ensure sufficient voltage withstanding capability to operate in MV applications. As sho-

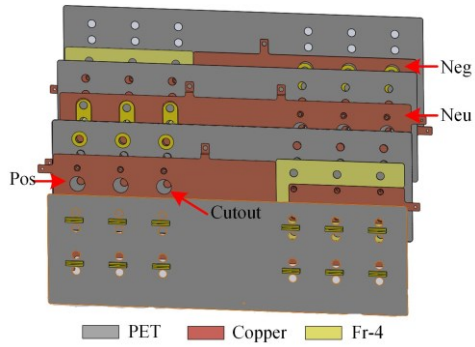
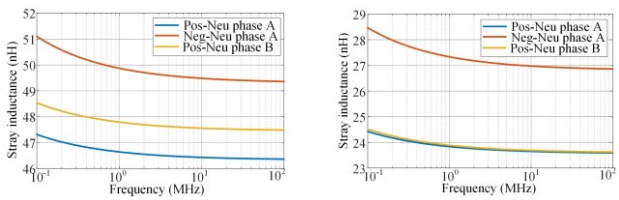


Fig. 4. The exploded view of busbar 1.



(a) (b)

Fig. 5. The simulated busbar stray inductance of (a) long loops, (b) short loops.

wn in Fig. 2, the 12 capacitors are divided into groups with 6 capacitors in each group. The capacitors that are close to phase A, form C_{dc1} in Fig. 1 and the other 6 capacitors form the C_{dc2}. In each group, the 6 capacitors are in 2×3 configuration, i.e., 2 capacitors in series and 3 in parallel. In this way, the total capacitance for C_{dc1} is 293 μF and each capacitor withstand 750 V at rated condition for the proposed hybrid 7-L converter. The equivalent stray inductance (ESL) of each capacitor is 40 nH, so the total stray inductance for C_{dc1} is 26.67 nH. These parameters are the same for the C_{dc2}.

By adopting the multilayer laminated layout design, as shown in Fig. 4, reduced parasitic inductance of busbar 1 is achieved, due to the increase of the negative mutual inductance among the planar copper planes as the result of the magnetic cancellation. The ANSYS Q3D [29] was used to extract the parasitic inductance of the ANPC copper busbars.

For each ANPC phase leg, it has long/short current commutation loops (CCL) for both positive-to-neutral and negative-to-neutral switching states transitions. The long/short loops for positive-to-neutral switching are illustrated in Fig. 3(a). Due to the geometrical symmetry of busbar 1, the stray inductances of the loops for positive-to-neutral, and neutral-to-negative in phase A can be the same as the ones for in phase C. While the inductances in phase B will be slightly different since phase B is in the middle. However, within phase B, the CCL inductance for positive-to-neutral and neutral-to-negative are identical. As a result, four CCLs in phase A and two CCLs in phase B are analyzed, which can also represent the rest six CCLs in busbar 1. In phase A leg, as shown in Fig. 5, the simulated stray inductances of long loops for positive-to-neutral and neutral-to-negative in phase A are 46.4 nH and 49.4 nH at 10 MHz, respectively, and the results for short loops of those two are 23.6 nH and 26.9 nH, respectively. As a comparison, stray inductance of long/short loops for positive-

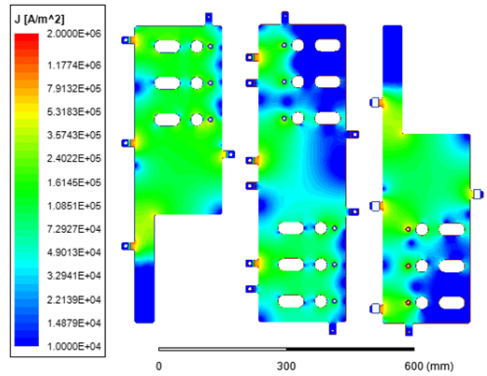
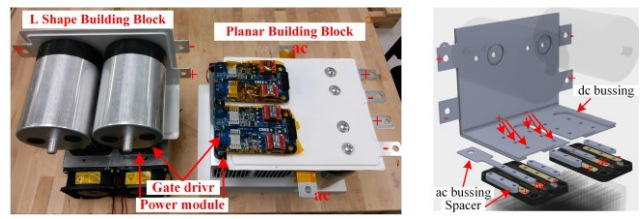


Fig. 6. Current density simulation result.



(a) (b)

Fig. 7. Picture of the (a) L shape and planar HB building blocks, (b) 3-D exploded view of the L-shape bussing structure.

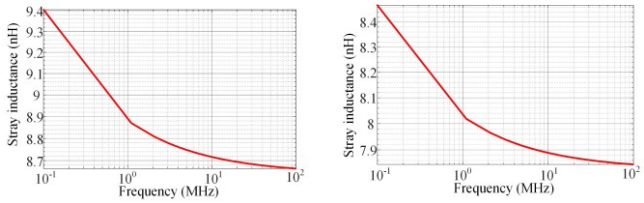
to-neutral in phase B are also 47.5 nH and 23.6 nH, respectively.

The voltage difference across two adjacent conductive copper planes in Fig. 4 is 1.5 kV. To ensure the proper voltage insulation, two 0.75 mm polyethylene terephthalate (PET) film layers are sandwiched among the three copper planes, while the exterior surface of busbar 1 is covered by the 0.25 mm PET film layers. To strengthen insulation, FR-4 material is applied to fill the space within the multilayer bussing structure and the edge of the busbar. The cutouts on busbars are made for capacitors installation with FR-4 applied inside. According to insulation calculation for busbar 1, the creepage distances between conductive bars with different voltage potentials meet IEC 60664 standard which requires 15 mm creepage distance for 1.5 kV and 30 mm creepage distance for 3 kV. To extend the creepage distance for the connections of capacitors on the PET surface layers, FR-4 spacers are placed on between holes for capacitor terminals, which is shown in Fig. 2.

The current distributions in dc positive, neutral and dc negative copper layers were simulated. In the simulation, the connection terminals for power modules are defined as the sinks where the current goes out from the busbar, while the dc input tabs and the rings for capacitor terminals are defined as the sources, where the current go into the busbar. Fig. 6 shows a typical current distribution map when the power stage is operated at 300 kW, where the max current density occurs on the tabs to the modules. The current density can be reduced by increasing the width of those tabs.

C. H-Bridge PEBB Design

Two compact air-cooled H-bridge building blocks are prototyped as shown in Fig. 7(a), i.e., a vertical design using L shape bussing structure with dimensions of 11.25” × 7” × 10”



(a) (b)

Fig. 8. The simulated stray inductance of the PCB (a) L shape bussing, (b) planar bussing.

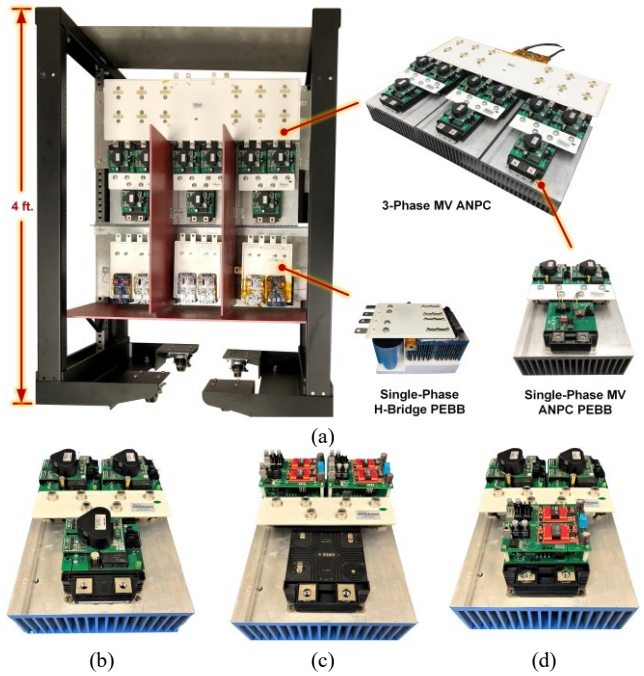


Fig. 9. Photograph of the (a) 1MVA 7-L electric propulsion converter; 3-phase ANPC MV ANPC in 7-L converter could be assembled by single-phase MV ANPC PEBB with structures (b) All-Si (c) All-SiC, and (d) Hybrid Si+SiC;

and total volume of 12.9 L, and a planar building block using a flat busbar with the size of 9.5" × 9.5" × 7" and total volume of 10.35 L. In both designs, two 1.5 kV 195 μF film capacitors DCP6S06195E000 from WIMA are used as dc capacitors, since film capacitors could provide better high-frequency performance compared with conventional electrolytic capacitors and could achieve higher capacitance with lower volume and cost compared with ceramic capacitors. The SiC power modules in the two designs are the 1.2 kV half-bridge CAS325M12HM2 from Wolfspeed. The commercial off-the-shelf dual-channel differential gate driver boards are used to drive the SiC modules. The gate driver has roughly the same footprint as the power module and has all the essential protections such as under/over voltage lockout, reverse polarity, and overcurrent lockout protection with indicator. In both designs, the fan/forced cooled heatsink LA7/100 12V with 0.1 C/W thermal resistance from Fischer Elektronik is used for power module cooling.

The development and demonstration of the planar building block has been reported in [30]. With the two ac terminals mounted on opposite sides and dc terminals on one side, this design is suitable for ac cascading structure, such as cascaded

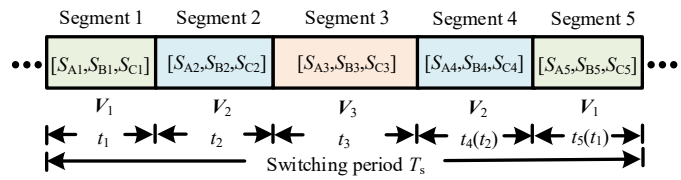


Fig. 10. Diagram of a five-segment switching sequence.

H-bridge (CHB) converter. Instead, the two ac terminals are mounted on one side and dc terminals are reserved on opposite sides, such that this design is suitable for multiphase structure with series-connecting multiple PEBBs' dc terminals. The L shape bussing structure exploded view is shown in Fig. 7(b). ANSYS Q3D is used to simulate the parasitic inductance of the two bussing structures shown in Fig. 7(a). The simulated results are shown in Fig. 8. The simulated stray inductance for L shape bussing is around 8.7 nH at 10 MHz, and inductance for planar bussing is below 7.9 nH at 10 MHz, which are both low to yield acceptable switching performance. Since the planar bussing has lower stray inductance and volume, also considering the hybrid 7-L converter in this work is based on cascading structure, the planar bussing structure is selected in this work.

D. System Assembly

A custom 4-ft tall rack system is developed to hold the full-scale 7-L ANPC-H converter as shown in Fig. 9(a), where ANPC power stage is mounted on the top and three H-bridge converters are placed on the bottom. The fiberglass boards are placed between the phase legs of the 7-L ANPC-H converter to achieve sufficient insulation strength for the prototype. All gate drivers are fed with an auxiliary isolated 12 V dc power supply. The prototype is fed with a 3 kV input dc power supply and can generate up to 3.18 kV rms line-to-line ac voltage. In this work, ANPC power stage is assembled by three single-phase MV ANPC PEBB. There are three ANPC PEBBs investigated in this work, which are: all-Si switch positions shown in Fig. 9(b), all-SiC switch positions shown in Fig. 9(c), and hybrid "Si+SiC" switch positions shown in Fig. 9(d). In the hybrid PEBB, switch positions S_5 and S_6 are implemented by SiC MOSFETs, the other switch positions are Si IGBTs. The adopted 3.3 kV Si and SiC modules have the same power terminal dimensions, which provides ease-of-replacement when transiting among three setups.

III. Space-Vector Modulation with Voltage Balancing and CMV Reduction

A computational efficient SVM scheme is adopted for the established hybrid 7-L converter prototype, based on the general space vector sequences calculation without requiring look-up tables (LUTs) [33], [34]. By adopting the scheme, all available five-segment switching sequences and their respective duty cycles are achieved with simple calculation, when the rotating reference vector locates in certain a modulation triangle. To achieve floating capacitors voltage balancing and CMV reduction, a finite-control-set model predictive control (FCS-MPC) scheme is adopted in this paper

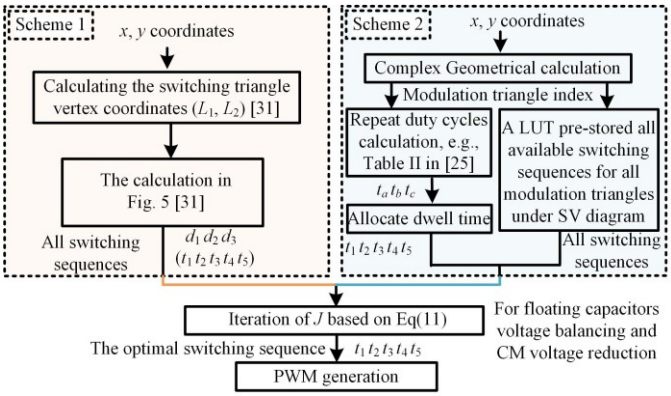


Fig. 11. The implementation flowcharts of scheme 1 (the proposed scheme) and scheme 2 (the conventional scheme in [25]).

to select the optimum switching sequence.

Fig. 10 shows the diagram of a five-segment switching sequence. At the jth (j=1, …, 5) switching state in a five-segment switching sequence, a function E_j is designed to assess the dc floating capacitors voltage drifting in the converter as

$$E_j = \frac{1}{2}\sum_{x=A,B,C}\left(C_{FC}\Delta v_{FCx}\right)^2 + \frac{1}{2}\sum_{y=1,2}\left(C_{dc}\Delta v_{dcy}\right)^2 \tag{1}$$

where the voltage differences are given as,

$$\Delta v_{FCx} = v_{FCx} - \frac{1}{4}U_{dc} \tag{2}$$

$$\Delta v_{dcy} = v_{dcy} - \frac{1}{2}U_{dc} \tag{3}$$

where v_{FCx} (x = A, B, C) is the H-bridge dc floating capacitor voltage in phase A, B, C respectively. v_{dcy} (y = 1, 2) is the voltage across the positive arm capacitor and negative arm capacitor in dc link, respectively.

All the dc floating capacitors approach an overall balancing state when the cost function (1) is minimized. The derivative of the cost function can be represented as,

$$\frac{dE_j}{dt} = \sum_{x=A,B,C}\Delta v_{FCx} i_{cx} + \sum_{y=1,2}\Delta v_{dcy} i_{cy} \tag{4}$$

where i_{cx} (x = A, B, C) is the current through the H-bridge capacitors in phase A, B, C respectively. i_{cy} (y = 1, 2) is the current through the positive arm capacitor and negative arm capacitor in the dc link, respectively.

The dc link of the hybrid 7-L converter can be modeled as

$$\Delta v_{dc1} = -\Delta v_{dc2} \tag{5}$$

$$i_O = i_{c1} - i_{c2} \tag{6}$$

$$i_O = i_{OA} + i_{OB} + i_{OC} \tag{7}$$

where i_O is current flowing out of the middle point O, and i_{OA}, i_{OB}, i_{OC} are current from O to phase-leg A, B, C respectively.

Substituting (5) to (7) into (4) yields

$$\frac{dE_j}{dt} = \left(v_{FCx} - \frac{U_{dc}}{4}\right)\left(i_{cA} + i_{cB} + i_{cC}\right) + \left(v_{dc1} - \frac{U_{dc}}{2}\right)\left(i_{OA} + i_{OB} + i_{OC}\right) \tag{8}$$

where the terms i_{cA}, i_{cB}, i_{cC}, i_{OA}, i_{OB}, i_{OC} all can be determined based on the switching state as illustrated in Table II.

According to [28], CMV at the jth (j=1, …, 5) switching state is derived based on converter phase voltages u_{AO}, u_{BO} and u_{CO}, where

$$u_{CMj} = \frac{1}{3}\left(u_{AO} + u_{BO} + u_{CO}\right) = \frac{U_{dc}}{4}\left(S_A + S_B + S_C - 9\right) \tag{9}$$

To reduce CMV, a cost function is given by (10) to minimize the error between the predicted one and desired value which is 0 in this paper.

$$J_{CM} = \sum_{j=1}^{5}\left|u_{CMj}\right| \tag{10}$$

For the switching sequence over one sampling period, a total cost function J is defined as (11) to balance floating capacitor voltages and simultaneously reduce CMV, where t_j is the dwell time of the jth switching state in the switching sequence, and $\lambda(0\leq\lambda\leq1)$ is the weighting factor for CMV. Hence, multiple values of cost function (11) are calculated using all the available switching sequences. With this FCS method, the optimal switching sequence can be determined by the one that minimizes the cost function (11).

$$J = \sum_{j=1}^{5} t_j \frac{dE_j}{dt} + \lambda J_{CM} \tag{11}$$

To demonstrate the efficiency and simplicity of the proposed SVM scheme in implementation, the flowcharts of the proposed scheme and the conventional 7-L SVM [25] are both given in Fig. 11. By adopting the two schemes, the same groups of switching sequences and the dwell time are achieved, if the reference vector has the same coordinates in space vector diagram. However, in the conventional scheme, duty cycles and all available switching sequences should be prestored in complex LUTs, which consumes much effort and controller resources. Also, the LUTs require the re-design for multilevel converters with different voltage levels. Instead, the proposed SVM scheme only requires some generic and fast calculation, getting rid of complex LUTs. In addition, this scheme is generalized for multilevel converters with different voltage levels.

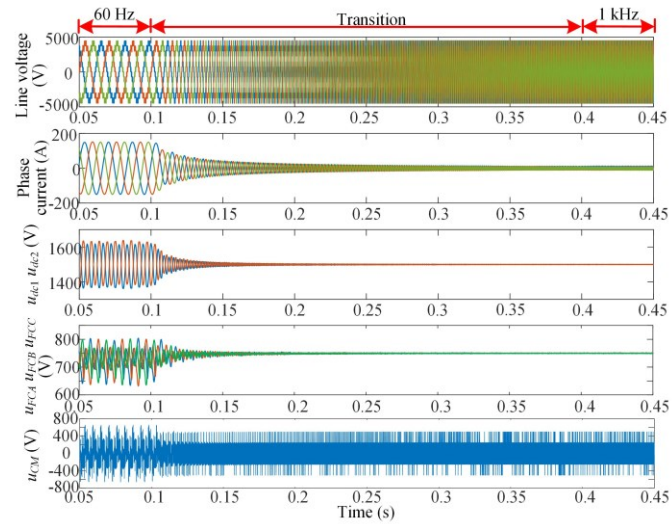


Fig. 12. Variable frequency operation from 60Hz to 1000Hz.

IV. Simulation Studies

To simulate the variable frequency operation for electric pr-

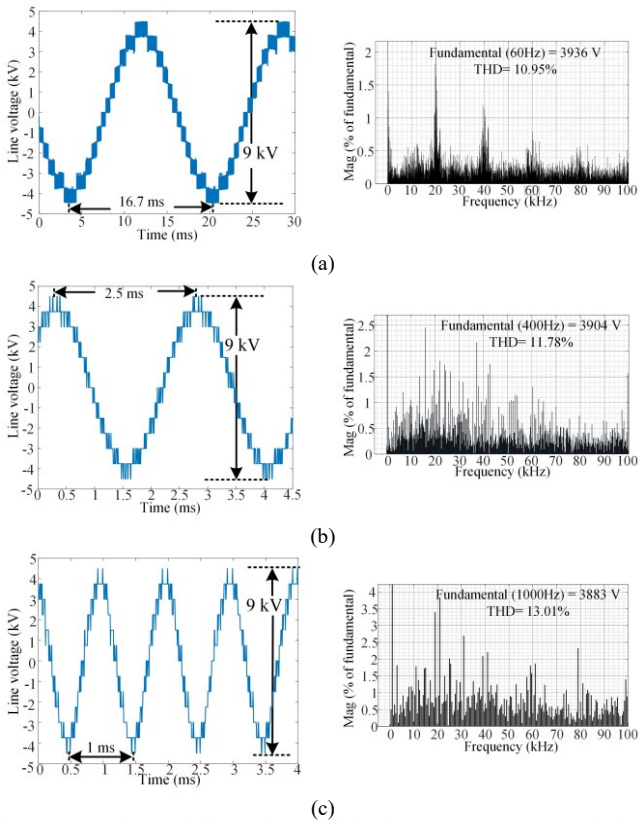


Fig. 13. Waveforms of line voltage and its harmonics spectrum analysis at fundamental frequency (a) 60Hz, (b) 400Hz and (c) 1kHz.

opulsion, this paper tested the hybrid 7-L ANPC-H converter operated with the variable output frequency from 60 Hz to 1000 Hz with the modulation index of 1.3. The modulation index m of this hybrid 7-L converter is defined as (12), where full modulation index for linear modulation region in SVM is 1.5 when phase voltage amplitude V_{ref} equals to $\sqrt{3}U_{dc}/2$. The load used in the dynamic test was a three-phase resistor-inductor (RL) load. The weighing factor λ is set to be 6.7×10^{-5}. Fig. 12 shows the simulation results including waveforms of the hybrid converter ac output line voltage, phase currents, dc voltage across floating capacitors in both dc link and H-bridges, and the CMV. The fundamental frequency increases from 60 Hz to 1000 Hz within 0.3 s with averaged ramp rate of 3133 Hz/s. According to simulated results, the capacitors voltages are all controlled at their rated value over the entire frequency range. The phase currents are gradually reduced during the transition from low frequency to high frequency range, since the load impedance increases with the increase of the fundamental frequency of the output. Thus, the proposed SVM strategy can be effectively applied for the 7-L ANPC-H converter prototype over the full-frequency operation.

$$m = \sqrt{3}\left|V_{ref}\right| / U_{dc} \tag{12}$$

The detailed waveforms of ac output line voltage at 60 Hz, 400 Hz and 1000 Hz are presented in Figs. 13(a), (b), (c), respectively. With the modulation index 1.3, the hybrid converter generates 13 levels in the ac line voltage under diff-

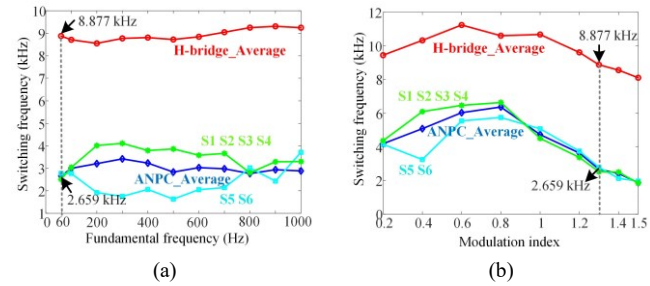


Fig. 14. The switching frequency of semiconductors in the ANPC and H-bridge stages under (a) a modulation index of 1.3 and different fundamental frequency, (b) a fundamental frequency of 60 Hz and different modulation indexes.

erent fundamental frequencies with the peak-to-peak value of ac line voltage is 9 kV. The harmonic spectrums of the three ac line voltage waveforms are given in Figs. 13(a), (b), (c), and their corresponding total harmonics distortion (THD) values are 10.95%, 11.78%, 13.01%, respectively. Noted that the harmonics are mainly concentrated on the multiple times of the SVM switching frequency, which is 20 kHz. Although there are fewer switching actions over one fundamental cycle for high-frequency operations such as 400 Hz and 1000 Hz than low-frequency conditions such as 60 Hz, the THD in the high-frequency scenarios only slightly increased.

The switching actions of all devices in both ANPC and H-bridges are counted such that the averaged switching frequency of devices in ANPC and H-bridge is derived under different conditions. Fig. 14(a) shows the switching frequency of ANPC devices and H-bridge devices under different operated fundamental frequency when applying modulation index 1.3 for the hybrid 7-L converter. The average switching frequency curve is flat versus the ac output fundamental frequency. The ANPC devices have much lower switching frequency, which are implemented using IGBTs. Fig. 14(b) shows the switching frequency under different modulation indexes when operated with 60 Hz fundamental frequency. With the increasing of modulation index, the switching actions in both ANPC and H-bridge decrease. Note, half-bridge based ANPC switches S_1/S_2, S_3/S_4 and S_5/S_6 have complementary PWMs. S_1/S_2 and S_3/S_4 are symmetrical in modulation. Hence, S_5 has the same switching frequency as S_6, and S_1~S_4 have the same switching frequency. Based on summarized curves, S_5/S_6 have comparatively lower switching frequency than S_1~S_4 in ANPC.

To validate the proposed scheme for capacitors voltage balancing with simultaneous CMV reduction, the Fig. 15 shows waveforms when modulation index step changed from 1.3 to 0.61, meanwhile, the CMV reduction scheme (λ = 6.7×10^{-5}) is applied and then switched off to show the impact. According to results under modulation index 0.61, CMV peak-to-peak is reduced from 3500 V to 1040 V when CMV reduction scheme is applied. In case of modulation index 0.61 with CMV reduction scheme applied, there are only voltage transitions between adjacent voltage levels in phase voltages, however inducing more voltage fluctuation across the dc floating capacitors. Also, dc floating capacitors voltage is stable in the modulation index transient from 1.3 to 0.61, whi-

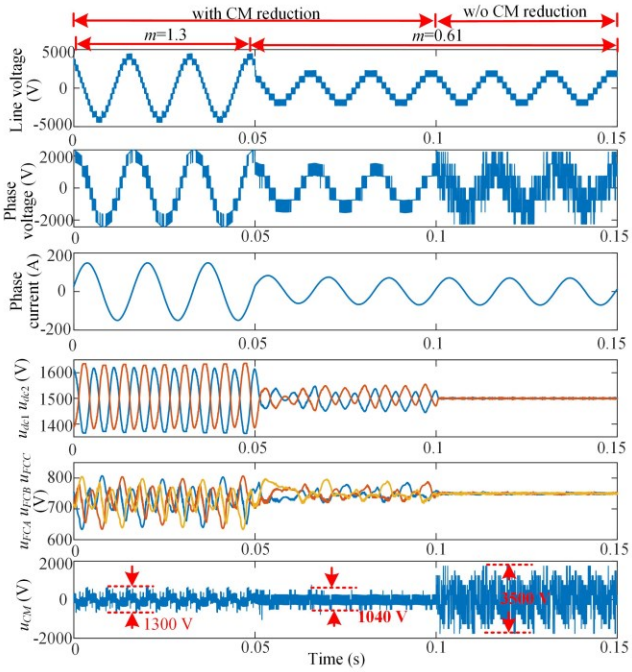


Fig. 15. Modulation index transition from 1.3 to 0.61 with and without applying CMV reduction scheme.

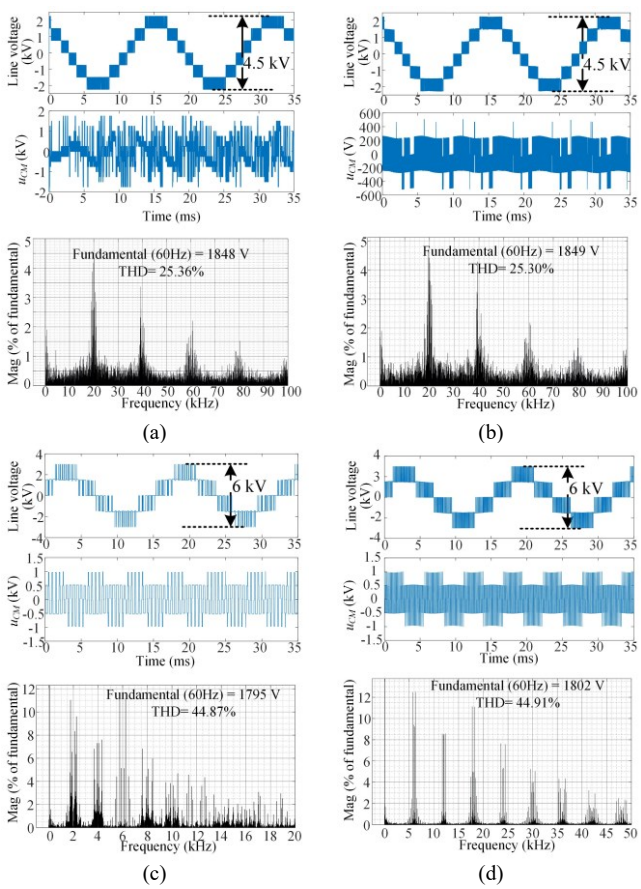


Fig. 16. Line voltage, CMV and line voltage harmonics spectrum of (a) 7-L ANPC-H when CMV reduction scheme is not applied, (b) 7-L ANPC-H when CMV reduction scheme is applied, (c) 3-L ANPC with 2 kHz switching frequency and (d) 3-L ANPC with 6 kHz switching frequency.

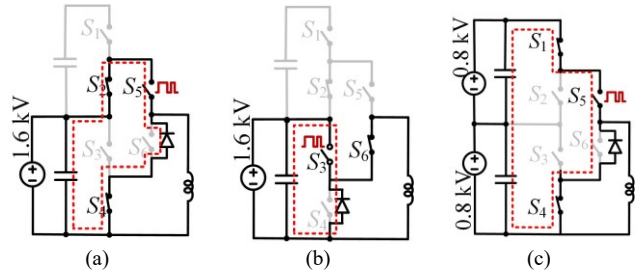


Fig. 17. CIL tests schematics for (a) case 1 (b) case 2 (c) case 3.

ch demonstrates the proposed SVM can balance capacitors voltage and can operate simultaneously with the CMV reduction scheme.

To reveal the advantage of this hybrid 7-L converter in terms of the THD and CMV, the 3-L IGBT-based ANPC is simulated for comparison with 3 kV dc link as well. The modulation index used in the simulation is also 0.61, which can theoretically generate approximately 1.8 kV ac line voltage. To ensure a fair comparison, the ac output line voltage and CMV of 7-L hybrid converter under the same modulation index, when without and with CMV reduction scheme, are given as Fig. 16(a) and (b) with line voltage harmonics spectrum exhibited. Fig. 16(c) shows ANPC ac line voltage and CMV waveforms and line voltage spectrum when applying 2 kHz switching frequency. Fig. 16(d) shows the corresponding results when ANPC applying 6 kHz switching frequency, since ANPC devices average switching frequency is also around 6 kHz in 7-L ANPC-H converter shown in Fig. 14(b). The THD values of the four cases are 25.36%, 25.3%, 44.87%, 44.91%, respectively.

According to the comparison results with 3-L ANPC, the hybrid 7-L converter with CMV reduction scheme could generate far less harmonics and lower CMV when they both output the same ac line voltage fundamental peak. Furthermore, the voltage differences between adjacent voltage levels in Fig. 16(a) and (c) are 750 V and 1500 V, respectively, demonstrating 7-L hybrid converter has smaller *dv*/*dt* caused by the ac output line voltage. It should be noted that the smaller *dv*/*dt* induces less EMI issues especially for some harsh conditions.

V. Prototype Validation

A. 3-L ANPC Power Stages Test

The ANPC has three typical current commutation loop (CCL) paths, i.e., as shown in Fig. 17, case 1: long CCL from DC+ or DC- to *O*; case 2: short CCL from DC+ or DC- to *O*; case 3: CCL from DC+ to DC-. To evaluate the switching performance in all three CCLs, the clamped inductive load (CIL) tests were conducted, where air-core inductor is connected between ac terminal and DC- terminal. In case 1, S_2 and S_4 are ON, S_3 is switching, and the other switches are OFF. In case 2, S_6 is ON, S_3 is switching, and the others are OFF. In case 3, S_1, S_4 are ON, S_5 is switching, and the others are OFF. The CIL test results of the three cases when using all-Si IGBTs in 3-L ANPC are shown in Figs. 18-20, respectively. The device is Infineon's 3.3 kV 450A half bridge

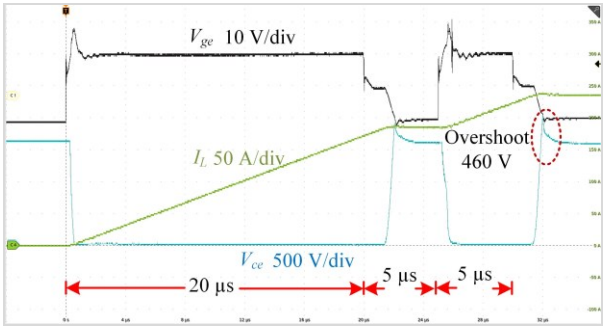


Fig. 18. CIL results of case 1.

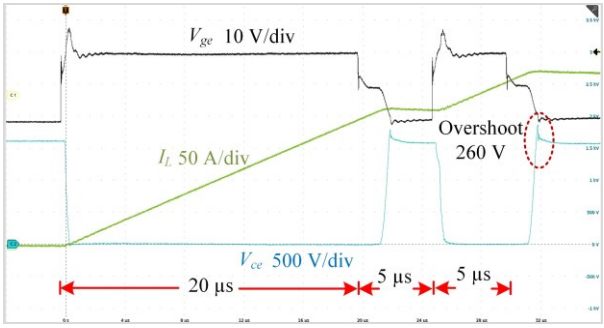


Fig. 19. CIL results of case 2.

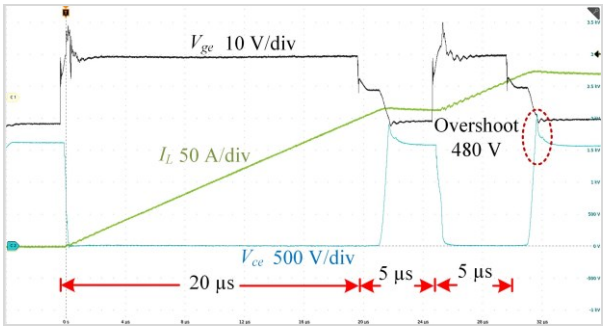


Fig. 20. CIL results of case 3.

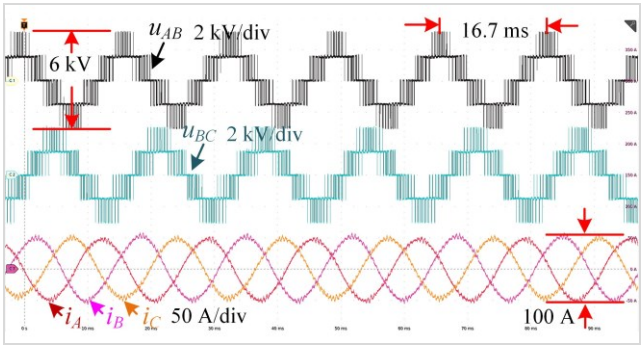


Fig. 21. ANPC output line voltage at 60Hz fundamental frequency.

IGBT modules in XHP-3 package [35]. The voltage overshoots of the switching devices in case 1, 2, 3 with the 1.6 kV dc link voltage 270 A load current turn-off are 460 V, 260 V and 480 V, respectively. Apparently, case 2 has the least device voltage overshoot attributed to its shortest CCL path.

The ANPC converter was tested as a three-phase inverter with 3 kV dc link voltage and 2 kHz switching frequency to generate a voltage with 60 Hz fundamental frequency. The S-

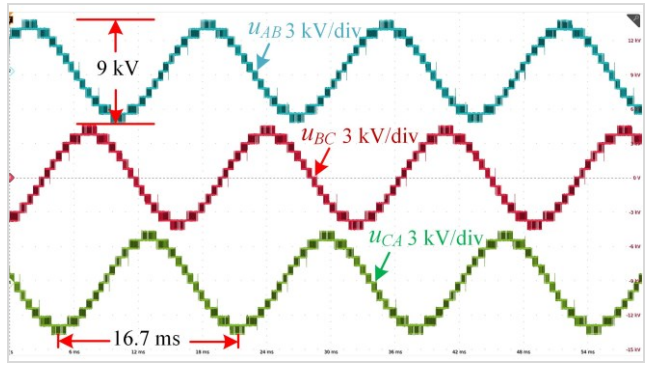


Fig. 22. 7-L ANPC-H output line voltage at 60Hz frequency.

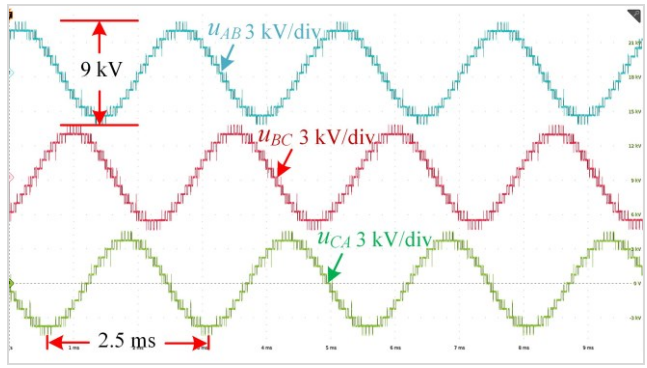


Fig. 23. 7-L ANPC-H output line voltage at 400Hz frequency.

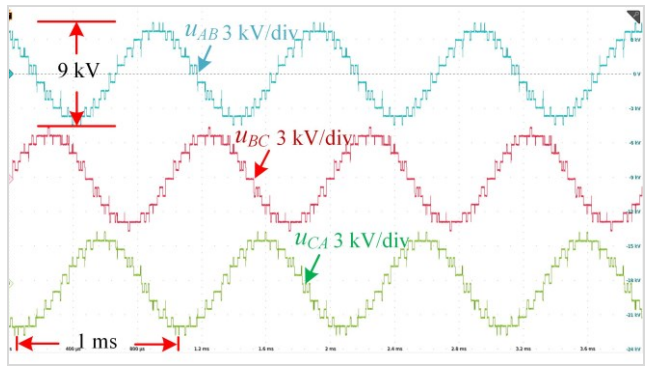


Fig. 24. 7-L ANPC-H output line voltage at 1kHz frequency.

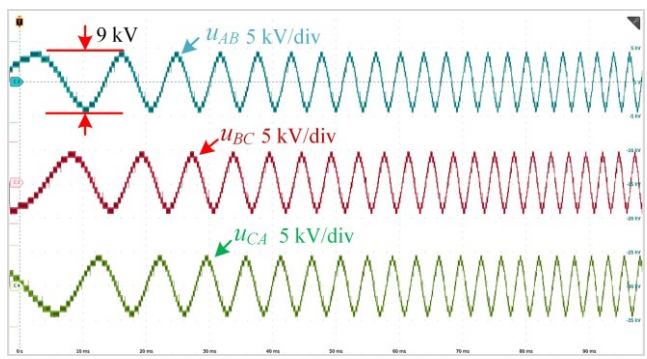
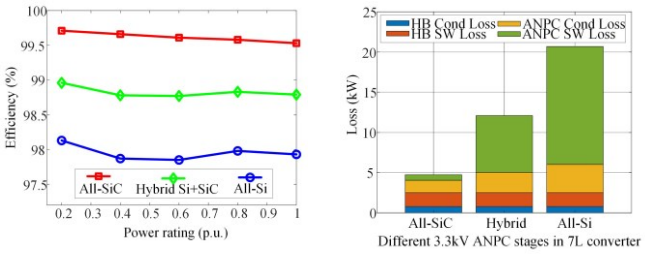


Fig. 25. 7-L ANPC-H output line voltage when frequency transiting from 60z to 400Hz.

PWM with modulation index 0.61 was adopted and converter ac terminals were connected to the Y-connection load. The load for each phase consists of series connected 10 mH induc-



(a) (b)

Fig. 26. 7-L ANPC-H converter with different structure in 3.3 kV ANPC stage (a) efficiency curve under different power ratings and (b) loss distribution at full power.

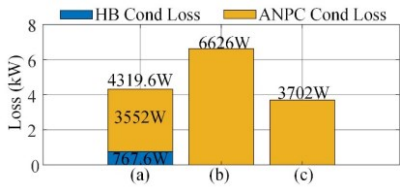


Fig. 27. Conduction loss breakdown in (a) 7-L ANPC-H converter, (b) single 1MW ANPC converter, (c) single ANPC with same current level with 1MW 7-L ANPC-H converter.

tor and 106 μF capacitor, whose equivalent impedance is 21.25 Ω at 60 Hz. Fig. 21 shows the experimental waveforms of ANPC output line voltages and phase currents.

B. 7-L ANPC-H Converter Proof-of-concept Test

To validate the proof-of-concept of 7-L ANPC-H converter, the assembled 7-L ANPC-H converter was tested in the three-phase inverter mode with 3-kV dc link, full modulation index, and same level of load current as shown in Fig. 21. Fig. 22 shows the experimental result in the low-frequency mode, e.g., 60 Hz, while Fig. 23 and Fig. 24 illustrate the high-frequency operation, i.e., 400 Hz and 1 kHz. Fig. 25 demonstrates the established 7-L ANPC-H converter prototype can smoothly operate from low frequency to high frequency range, e.g., transiting from 60 Hz to 400 Hz, which represents a typical speed ramp in propulsion applications.

C. 7-L Converter Efficiency Estimation

To compare the power efficiency of 7-L ANPC-H converter when its inner 3.3 kV ANPC stage adopts different structures, i.e., all-SiC, all-Si and hybrid Si+SiC, the converter switching losses and conduction loss are estimated by converter loss model based on SiC and Si devices loss data, under different converter power ratings. Fig. 26(a) shows converter efficiency comparison under the three cases, where the all-SiC case has the highest efficiency. Fig. 26(b) shows the switching loss and conduction loss breakdown both in 3.3 kV ANPC and 1.2 kV HB stages, when 7-L converter operates at 1 MVA rated load. The three cases have the same switching and conduction losses in 1.2 kV HB stage. Because SiC devices consume much smaller energy loss both in switching and conducting, the all-SiC case has the minimum switching/ conduction losses in 3.3 kV ANPC stage, the hybrid Si+SiC case has the medium values, and the all-Si case has the largest losses.

The 7-L converter has extra current baring H-bridges than the single ANPC converter. To demonstrate the conduction lo-

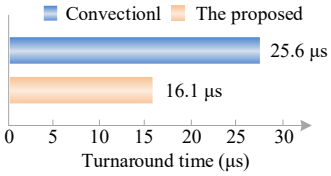


Fig. 28. Execution time comparison of the conventional and proposed SVM strategies.

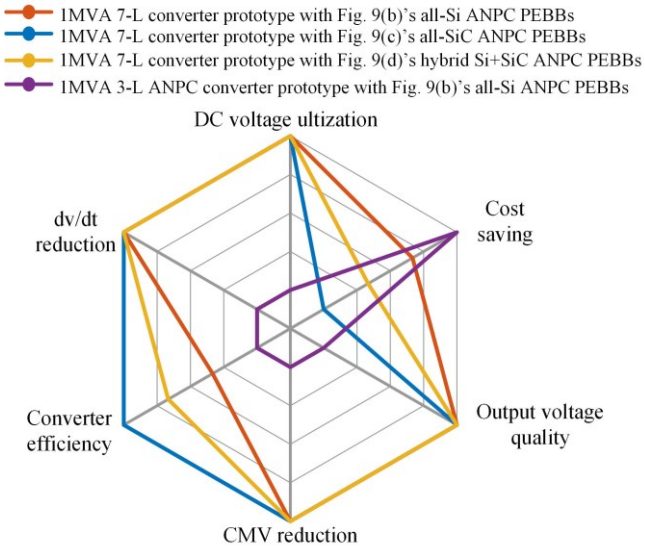


Fig. 29. Comparison of 7-L ANPC-H converter and 3-L ANPC converter.

ss penalty due to existence of H-bridges, three cases all with 3 kV dc link are compared, where Case (a): 1MW 7-L ANPC-H converter with all-Si devices in its inner ANPC stages, Case (b): Single 1MW 3-L ANPC converter with all-Si devices, Case (c): All-Si single ANPC operated by the same current level with Case a; The conduction loss breakdown of the three cases is shown in Fig. 27(a), (b) and (c), respectively. Because 7-L converter has higher ac voltage output than 3-L ANPC, current stress in 7-L converter is lower when they operate under the same dc link and power level, so that conduction losses in Case (a) are lower than Case (b). When considering 7-L converter's ANPC stage and the single ANPC have the same current level, the 7-L converter overall conduction loss is a little higher than the single ANPC, according to Fig. 27(a) and (c).

D. 7-L Converter Modulation Computation Efficiency

To further demonstrate the computational efficiency of the proposed SVM for the 7-L ANPC-H converter, both the conventional SVM [25] and the proposed SVM illustrated are implemented. The control algorithms in block of scheme 1 and block of scheme 2 shown in Fig. 11 were both implemented in dSPACE and their execution times are also measured in the real-time mode. The implemented discrete control frequency in dSPACE is 20 kHz, namely, the execution time of the strategies in every control iteration cannot exceed 50 μs. Fig. 28 exhibits the real-time mode execution times of the two strategies for the specific case when the modulation index is set to 1.05. As it can be seen, the execution time in conventio-

TABLE III.
SPECIFICATION COMPARISONS OF THE EXISTING MEGAWATT-SCALE CONVERTERS

References	Topology	Devices	dc link	Power	Efficiency	Power density	Volume	Weight
[36]	Boeing787 dc/ac, 2L-VSI	All-Si	270 V	8 kVA	87 %	2.15 kVA/kg 1.54 kW/L	5.18 L	3.72 kg
[37]	Five 2L-VSI in parallel	All-SiC	650 V	500kW	98.5 %	1.246 kW/L	401.41 L	-
[18]	3L-ANPC	Si+SiC	2.4 kV	1 MW	99 %	12kVA/kg 2.5 kW/L	400 L	98 kg
[38]	Three ANPC in parallel	Si+SiC	1 kV	1 MW	99.3 %	-	-	-
[39]	5L-ANPC	All-Si	6 kV	800kW	-	-	-	-
[40], [41]	Two 3L-ANPC in parallel	All-SiC	1 kV	1 MVA	99%	18 kVA/kg	-	55.6 kg
In this work	7-L ANPC-H	Si+SiC	3 kV	1 MW	98%	4.82 kW/L	207.48 L	-

nal SVM strategy is 25.6 μs versus 16.1 μs in the proposed SVM, which demonstrated over 1/3 turnaround time reduction when using the proposed SVM.

E. Summary of 7-L ANPC-H Converter Advantages

Fig. 29 compares the figure of merit of the 7-L ANPC-H converter and the conventional 3-L ANPC converter implemented by 3.3 kV IGBTs. The dc voltage utilization of 3-L ANPC and 7-L ANPC-H converter is 1.15 and 1.5, respectively, such that the present 7-L converter has much higher dc voltage utilization. To achieve the same converter ac output voltage THD, 7-L converter could generate less loss than 3-L converter because its switching actions are largely distributed to 1.2 kV low-voltage SiC H-bridge stages. Hence, 7-L converter could achieve higher power efficiency than 3-L IGBT implemented ANPC. Attributed to 7-level voltage output, 7-L converter has much smaller dv/dt in converter voltage output than 3-L converter, hence 7-L converter could have the less EMI issue and better output voltage quality than 3-L converter. The 7-L converter can have less CMV compared with 3-L converter. Although the IGBT based 3-L ANPC has lower cost than the presented 7-L converters with three kinds of ANPC PEBBs, the ac passive filtering and/or EMI filtering can be much simplified when using the proposed 7-L converter solution leading to higher power density and cost reduction at system level.

To make a fair comparison between the established 7-L hybrid ANPC-H converter the state-of-the-art technologies, several previously reported megawatt-scale converters are listed in Table III, including efficiency, power density, volume, and weight. Compared to 270 V low-voltage system, the higher dc voltage could have more weight/volume savings capability. With the increased dc voltage and by adopting "Si+SiC" solutions, power density has a rising trend, and the system could be weight-lighter regarding application-level packaging.

V. CONCLUSIONS

This paper presents the development of a hybrid 7-L ANPC-H converter prototype system with 3 kV dc link aiming at the next-generation MV electric aircraft propulsion applications. Implemented by ANPC PEBBs with 3.3 kV Si and/or SiC devices and H-bridge PEBBs with 1.2 kV SiC devices, the established 7-L ANPC-H converter demonstrates the MW-scale prototyping feasibility with hybrid converter concepts. Based on comprehensive simulation and experiment investigation, the established 1MW 7-L ANPC-H prototype embraces the following advantages when comparing with state-of-the-art MV converters especially 3-L ANPC converter:

1) With most of switching actions distributed into SiC-based low-voltage H-bridge stage with SiC devices, the 7-L ANPC-H converter has smaller switching losses that converter power efficiency is improved.
2) The established 7-L MV converter generates more ac output voltage levels, resulting in less harmonics and less EMI issues induced by dv/dt. Thus, ac passive filtering and/or EMI filtering can be weight-light and simplified, in turns, system level could achieve higher power density and cost reduction.
3) The established 7-L MV converter has higher dc voltage utilization and higher ac voltage output capability, so that conducting current could be lower to reduce wire weight for MV electric aircraft propulsion applications.
4) The established 7-L converter has less CMV with the proposed CMV reduction scheme in this work. With less CMV, ground to motor shaft voltage which induces bearing current could be smaller, so that lifetime of the motor could be prolonged.

Therefore, with the proven excellent advantages, the established 7-L ANPC-H converter can significantly advance the next-generation MV electric aircraft propulsion based on the up-to-date Si and SiC-based devices.

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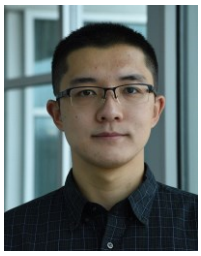

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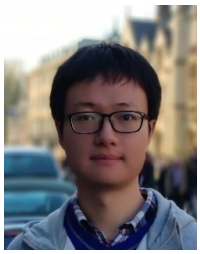

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