Observation of MOSFET-like behavior of a TFT based on amorphous oxide semiconductor channel layer with suitable integration of atomic layered deposited high-k gate dielectrics

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ABSTRACT

A series of different high κ dielectrics such as HfO_2, ZrO_2, and Al_2O_3 thin films were studied as an alternative material for the possible replacement of traditional SiO_2. These large areas, as well as conformal dielectrics thin films, were grown by the atomic layer deposition technique on a p-type silicon substrate at two different deposition temperatures (150 and 250 °C). Atomic force microscopic study reveals that the surface of the films is very smooth with a measured rms surface roughness value of less than 0.4 nm in some films. After the deposition of the high κ layer, a top metal electrode was deposited onto it to fabricate metal oxide semiconductor capacitor (MOSCAP) structures. The I–V curve reveals that the sample growth at high temperatures exhibits a high resistance value and lower leakage current densities. Frequency-dependent (100 kHz to 1 MHz) C–V characteristics of the MOSCAPs were studied steadily. Furthermore, we have prepared a metal oxide semiconductor field-effect transistor device with Al-doped ZnO as a channel material, and the electrical characteristic of the device was studied. The effect of growth temperature on the structure, surface morphology, crystallinity, capacitance, and dielectric properties of the high κ dielectrics was thoroughly analyzed through several measurement techniques, such as XRD, atomic force microscopy, semiconductor parameter analysis, and ultraviolet-visible spectroscopy.

INTRODUCTION

In the past decades, a very thick layer of silicon dioxide (SiO_2) film has been the most used gate-insulating dielectric material for many electronic devices, including metal–oxide–semiconductor field-effect transistors (MOSFETs), thin-film transistors, metal–oxide–semiconductor capacitors (MOSCAPs), and others. SiO_2 has been used extensively for its easy and large-area conformal growth. However, SiO_2 has several disadvantages, which led to active research to look for alternatives.[1–3] When SiO_2 reaches a thickness of a few tens of nanometers, a strong adverse effect arises in terms of its leakage current dominance because of the charge carrier flow across the films,[3–8] which hinders the device performance as well as consumes large power during operation.[9–13] Therefore, SiO_2 cannot withstand the downscaling requirements of modern electronic device technology.[14–16] One approach to scaling down electronics while sustaining adequate dielectric properties is incorporating high κ dielectric thin film. High κ dielectrics refer to materials with a high dielectric constant, which denotes the material's ability to sustain a higher applied electric field. High κ dielectrics can suppress the leakage current at a significantly lower film thickness than conventional SiO_2, which allows more room to scale down the device sizes with improved performance and low power consumption. SiO_2 generally has a dielectric constant of ~4, while high κ dielectrics show a much higher dielectric constant

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value lying between 20 and 30. Moreover, high κ dielectric materials including hafnium oxide (HfO_2), zirconium oxide (ZrO_2), and aluminum oxide (Al_2O_3) also show a larger bandgap (E_g). For instance, HfO_2 has a theoretical dielectric constant and bandgap value of 25 and 5.8 eV, respectively. Similarly, ZrO_2 exhibits a dielectric constant of 24 and a bandgap of 5.8 eV. However, Al_2O_3 has a lower theoretical dielectric constant of 9 but possesses a larger bandgap.

High κ dielectrics can be grown by various deposition techniques.[17–20] As the atomic ratio of most as-grown oxide thin films deviates from its stoichiometry, high κ dielectric films may similarly show non-stoichiometric elemental composition, and this leads to oxygen vacancy and defects in the lattice, strongly hindering their electrical properties.

In this work, we have fabricated and studied the behavior of MOSCAPs and MOSFETs by optimizing the growth condition and electrical properties of Al_2O_3, HfO_2, and ZrO_2 high κ dielectric films under different growth conditions.

EXPERIMENT

HfO_2, ZrO_2, and Al_2O_3 thin films were conformally grown by atomic layer deposition (ALD) using respective precursors of tetrakis(dimethylamido) hafnium (TDMAH), tetrakis(dimethylamido) zirconium, trimethylaluminum (TMA), and deionized (DI) water as an oxygen source. The high κ films have a thickness of 40 nm and were deposited on p-type silicon and glass substrates. Initially, the substrates were cleaned for 10 min each with acetone and isopropyl alcohol. The dielectric films were grown at two different ALD chamber temperatures of 150 and 250 °C with a flow rate of 20 SCCM of N_2 gas. Finally, aluminum-doped zinc oxide (AZO) is used as a channel material, grown through the electron beam evaporation technique. Thickness measurements of the films were performed using a profilometer (Bruker, DektakXT). The surface morphology of the films was obtained in tapping mode using an atomic force microscope (AFM) from Vecco. A Keithley 4200 semiconductor parameter analyzer was used to characterize the electrical properties of the devices, such as I–V, I_{DS}–V_{DS} performance, and capacitance-versus-voltage (C–V). Ultraviolet-visible spectroscopy (UV-VIS) was carried out to obtain the absorbance and transmittance data to calculate the bandgap of the prepared dielectric films using a Perkin Elmer Lambda 950 UV/Vis spectrometer.

Device fabrication

The schematic diagram of the fabricated MOSCAP is shown in Fig. 1(a). During the deposition using the ALD technique, we noticed that the dielectric films are also deposited underneath the substrate. We used hydrofluoric acid and DI water in a 1:10 ratio and a buffered oxide etchant (BOE) to remove any residual dielectric film present on the bottom surface of the substrates. Indium was used as a bottom contact for all electrical measurements. In the next step, samples were loaded into an AJA international DC sputtering system for the deposition of a platinum (Pt) electrode of 50 nm using a 200 μm diameter shadow mask. After the deposition of Pt, the dielectric samples were heated using a hotplate for 20 min at 150 °C for good interfacial contact between the Pt metal and the dielectric film.
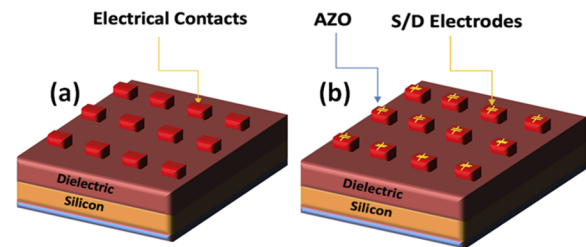

FIG. 1. (a) Schematic diagram of the MOSCAP structure and (b) schematic diagram of the MOSFET device.
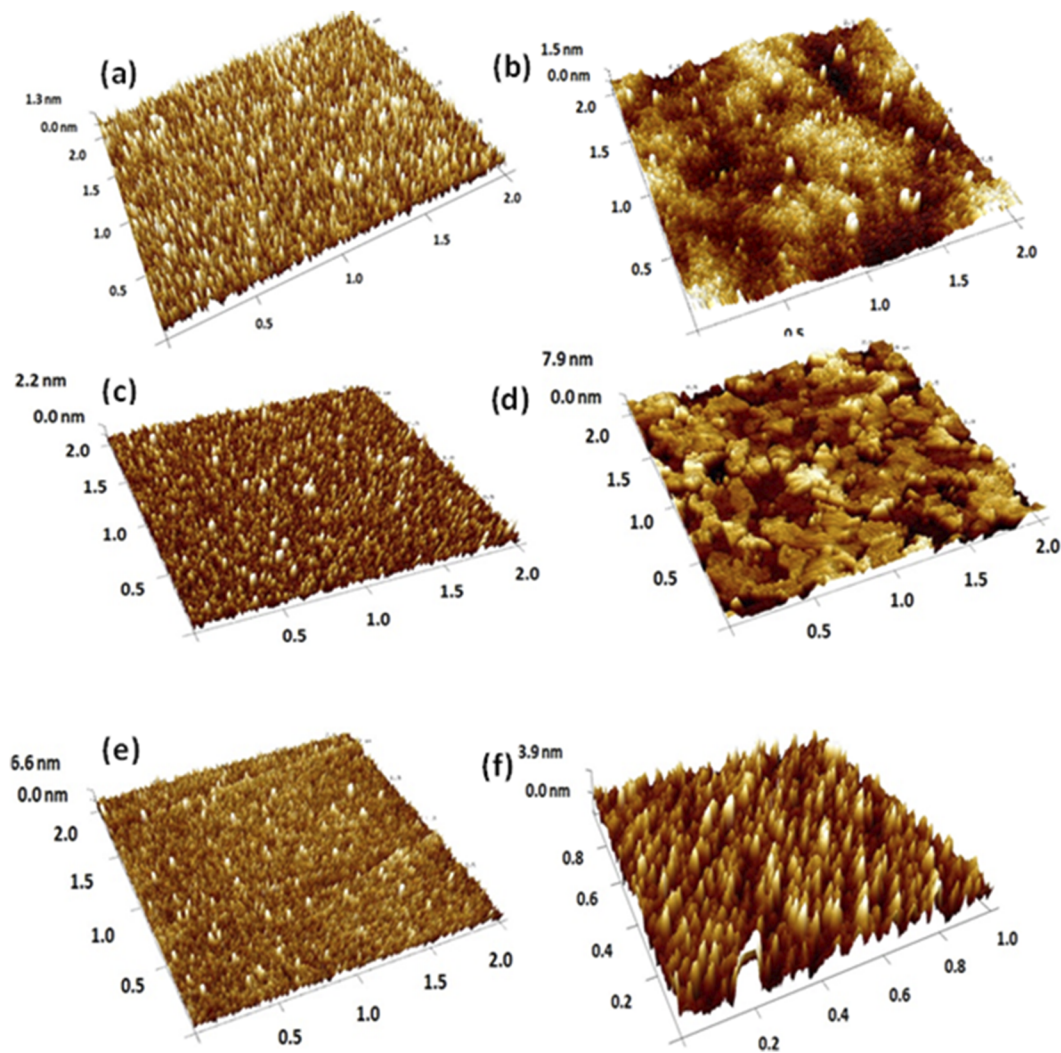
The schematic diagram of MOSFETs is shown in Fig. 1(b). Al_2O_3 is used as a dielectric gate layer deposited on p-type silicon. MOSFETs were fabricated after dielectric deposition. Al-doped ZnO was deposited using an appropriate mask for the active channel materials of the device. Subsequently, source and drain contacts were made using shadow mask technology, as shown in Fig. 1(b).

RESULTS AND DISCUSSIONS

Surface morphology

AFM surface morphology of the samples was carried out in the tapping mode (512 × 512 pixels) and with a scan rate frequency of 0.5 Hz. Figure 2 shows the 3D AFM surface morphology of all dielectric films prepared at different growth temperatures. We observed that the surface morphology of ALD-grown Al_2O_3 thin films was affected by the substrate deposition temperature. The root mean square (rms) roughness, defined as the standard deviation of the surface height profile from the mean height, is the most commonly reported measure of surface roughness. The samples deposited at 150 °C showed a relatively smoother surface with an average surface roughness (rms) value of 0.351 nm and grain size of 42.66 nm. By increasing the chamber deposition temperature to 250 °C, the surface roughness and the grain size of the Al_2O_3 films increased with distinctly visible grain boundaries. The film shows an rms value of 0.512 nm, and the grain size expanded to 56.03 nm. The increment in the surface roughness and grain size with the chamber/substrate temperature is attributed to an atomic rearrangement that takes place due to the increased mobility of atoms on the substrate surface at higher temperatures, which leads to the formation of larger grains.

The surface topography of the HfO_2 thin films measured according to the substrate temperature (150 and 250 °C) is shown in Figs. 2(c) and 2(d), respectively. The HfO_2 films showed regular and conformal growth on the substrate. It can visually be seen that for the 150 °C growth film, the surface consists of small, close-packed, and nearly uniform structures. The film shows an rms value of 0.218 nm and a grain size of 57.98 nm with a smoother thin film surface.[21,22] When increasing the chamber deposition temperature to 250 °C, the surface structures appear to be larger and clustered. This indicates that at higher temperatures, the particles get elongated and form highly interconnected surface structures and hence the densification of bigger particles on the surface. The higher roughness and grain growth are recorded on the thin films deposited at 250 °C with a value of 2.86 and 107.52 nm, respectively.

FIG. 2. 3D AFM surface morphology images of Al_2O_3 films were deposited at (a) 150 °C and (b) 250 °C, HfO_2 films were prepared at (c) 150 °C and (d) 250 °C, and ZrO_2 films were grown at (e) 150 °C and (f) 250 °C.

The AFM surface morphology of ZrO_2 thin films is shown in Figs. 2(e) and 2(f). The deposition of ZrO_2 films shows a conformal, more compact, and fine-grained structure. It is observed that the deposition temperature has some remarkable effects on the film topography. The thin film grown at 150 °C shows a smoother surface with an rms surface roughness value of 0.176 nm and a uniform grain size of ≈27.42 nm distributed on the substrate surface. As the deposition temperature increased to 250 °C, the crystallite size and grain growth of the film increased further and subsequently enhanced the surface roughness. The 250 °C grown film shows an rms surface roughness value of 0.737 nm and a grain size of ≈37.35 nm. Details about the grain size and rms surface roughness of the various thin films grown at different temperatures are shown in Table I.
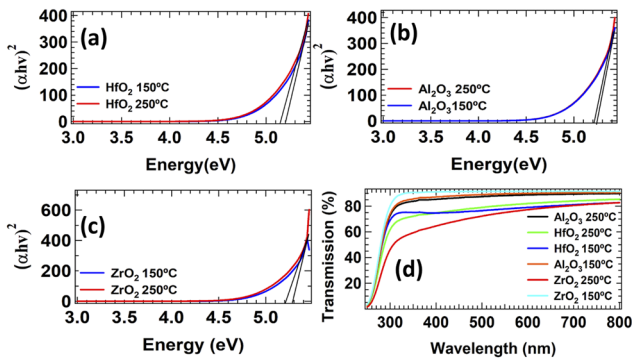
Optical properties

The optical absorption edge is a significant parameter for describing solid-state materials. The optical bandgap (E_g) is related

TABLE I. Summary of the rms and grain size of the different thin films at different growth temperatures.

Film	rms (nm) 150 °C	rms (nm) 250 °C	Grain size (nm) 150 °C	Grain size (nm) 250 °C
Al_2O_3	0.351	0.512	42.66	56.03
HfO_2	0.218	2.860	57.98	107.52
ZrO_2	0.176	0.737	27.42	37.35

FIG. 3. Optical bandgap of high κ dielectric films: (a) HfO$_2$, (b) Al$_2$O$_3$, and (c) ZrO$_2$. (d) Transmission spectra as a function of wavelength of ZrO$_2$, Al$_2$O$_3$, and HfO$_2$ films deposited at various growth temperatures.
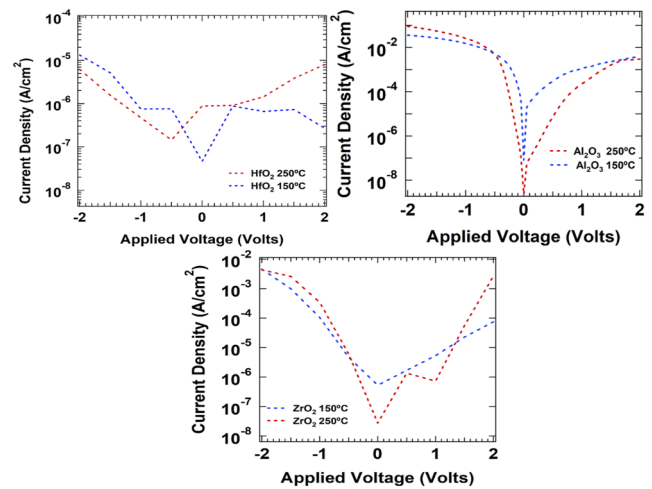

FIG. 4. Current density as a function of applied voltage of the films grown at 150 and 250 °C: (a) HfO$_2$, (b) Al$_2$O$_3$, and (c) ZrO$_2$.

to the absorption coefficient (α) and photon energy (hν) through the Tauc relation. Figure 3 shows the plots of (αhν)^2 as a function of hν to obtain the optical bandgap of the high dielectric films deposited at 150 and 250 °C growth temperatures. E$_g$ can be extracted through the onset of the optical transitions of the films near the band edge, which is equal to the value of the fitting line intercepts. The extrapolated to zero values of the absorption edge calculation of all the samples show very wide optical bandgaps. The calculated value of E$_g$ for Al$_2$O$_3$, HfO$_2$, and ZrO$_2$ thin films grown at a temperature of 150 °C is 5.46, 5.26, and 5.61 eV, respectively. It is worth noting that the deposition temperatures significantly do not affect the optical bandgap of Al$_2$O$_3$, HfO$_2$, and ZrO$_2$, as shown in Figs. 3(a)–3(c).[23–26] Furthermore, similar optical bandgap values are reported for the ALD-grown Al$_2$O$_3$, HfO$_2$, and ZrO$_2$ thin films by other research groups.[27–29] The transmission spectra of the films deposited at different growth temperatures are shown in Fig. 3(d). The transmission spectra of all the samples show similar behavior, with a transmission value of up to 91% in the visible to the near-infrared (NIR) region ranges from 780 to 2500 nm on the wavelength spectrum.

Current density–voltage characteristic

Figure 4 shows very stable current density–voltage (J–V) characteristics of the high κ dielectric films. All films show changes in magnitudes of the J–V curve under different temperature growth conditions, indicating that the grain boundaries in the films can be altered with the growth temperature. The films show an improved performance and a decreased leakage current with increasing deposition temperature due to the improvement in the crystallinity properties of the films. HfO$_2$, ZrO$_2$, and Al$_2$O$_3$ show improved leakage current densities, as shown in Figs. 4(a)–4(c), respectively, indicating that the ALD deposited high κ dielectric films are of very good quality and are more suitable to be used as gate dielectric layers for electronic devices.
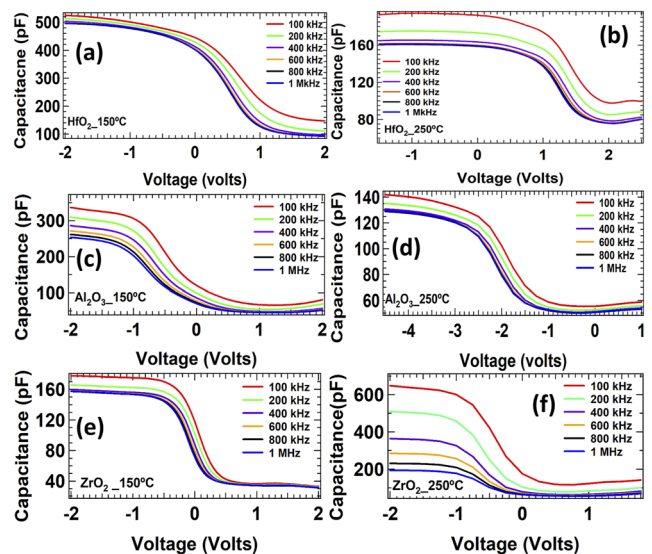
Capacitance–voltage characteristic

The capacitance of a MOS capacitor is not constant. When varying the applied voltage across the MOS structure, the capacitance values are varied, which is different from those of a traditional double-layer capacitor having only constant capacitance regardless of the applied voltage. The relationship between the capacitance of an ideal MOS capacitor and the applied voltage can be typically divided into an accumulation region, depletion region, and inversion region. The measured capacitance data are plotted as a function of voltage at high and low frequencies (100 kHz up to 1 MHz) of HfO$_2$ films at different growth temperatures, as shown in Figs. 5(a) and 5(b), respectively. A small frequency dispersion is observed at the flat-band voltage V$_{FB}$ region of the C–V curve. The capacitance value in the accumulation region decreases with the increase in the

FIG. 5. Capacitance–voltage results of HfO$_2$ at (a) 150 °C and (b) 250 °C, Al$_2$O$_3$ deposited at (c) 150 °C and (d) 250 °C, and ZrO$_2$ films grown at (e) 150 °C and (f) 250 °C.

applied voltage frequency region. This can be attributed to the interface state charges. It is worth noting that when C–V is measured at lower frequencies, the interface state charges can easily follow the AC signal, which increases the capacitance value. This implicates the presence of charge traps in the dielectric film, i.e., shallow traps that keep up with the signal's frequency. On the other hand, in the C–V measurements at a high frequency of 1 MHz, the surface state charges cannot follow the AC signal. Hence, they could not have any significant impact on the accumulation capacitance due to their higher lifetime than $1/2\pi f$. Moreover, the V_{FB} values of the C–Vs of the MOSCAP devices with lower growth temperature (150 °C) films are smaller (in absolute values) than those of the higher growth temperature (250 °C) films. This is related to the development of a positive charge in the dielectric layer.[30]

Figures 5(c) and 5(d) show the C–V characteristics measured for Al_2O_3 thin films grown at two different temperatures. The C–V characteristics show three distinct regions as the applied voltage is swept from −ve to +ve voltage where a clear distinction between the accumulation, inversion, and depletion regions can be observed.

The 150 °C-grown Al_2O_3 film shows higher capacitance than the 250 °C grown film. The frequency applied to the device may be too high for the interface traps or defects to follow, indicating that the traps or defects do not influence the increase in capacitance. Since the traps or defects cannot follow the alternating frequencies, they can follow the DC biasing. This causes the last region, inversion, to slightly increase with the voltage rather than reaching equilibrium as compared to the Al_2O_3 grown at 250 °C. The Al_2O_3 film grown at 250 °C exhibits a shorter accumulation region, indicating a lower concentration in hole carriers and a larger presence in the minority carriers as the device transitions from inversion to depletion at a negative voltage. This lower concentration of hole carriers could be fixated in the interface due to a polycrystalline structure. Similar to the HfO_2 film, the V_{FB} voltage values of the C–Vs of MOSCAP devices with lower growth temperature (150 °C) films are smaller (in absolute values) than those of the higher growth temperature (250 °C) film, and the maximum capacitance is 366 pF.

The C–V curves of the ZrO_2 dielectric film are depicted in Figs. 5(e) and 5(f) where there is a clear transition between C–V regions as the voltage increases. The ZrO_2 dielectric film grown at 250 °C shows a higher capacitance value and more frequency dispersion than the 150 °C grown film. However, the 250 °C grown film had a right shift in V_{FB} with lower frequencies. The shift in V_{FB} is mostly due to the changes in the interface and fixed oxide charges.[31,32] As the films were grown using H_2O as the oxygen source, the oxygen present in the ZrO_2 film diffuses toward the interface and favors the growth of the native SiO_2 layer on the Si substrate. Hence, the existence of the SiO_x layer implements a series capacitance. Subsequently, the capacitance of the ZrO_2-based MOSCAP was impacted, which can reduce the defects at the interface and improve interface quality.[14,31] The maximum capacitance value measured for the 250 °C grown ZrO_2 film-based MOSCAP is 698 pF.

MOSFET characteristics

For the MOSFET development, Al_2O_3 was used as the dielectric with a thickness of 40 nm, while that of the active layer, AZO, was 20 nm. Chromium was used for the source and drain electrodes with
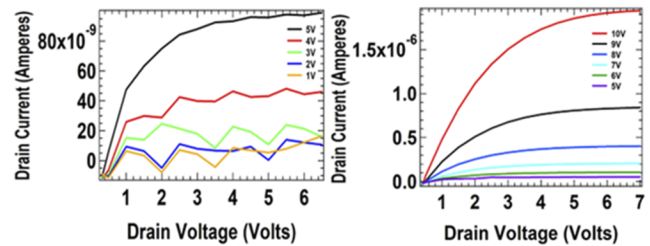

FIG. 6. Electrical characteristics of the MOSFET device made up of Al_2O_3 as the gate insulating layer and AZO as the channel layer.

a thickness of 30 nm. The electrical characteristic of the MOSFET device showing the drain current I_d vs V_d, at a variable gate voltage of 10–5 V, is depicted in Fig. 6.

The MOSFET is operating on enhancement mode, and the back-gate voltage is set from 1 to 10 V with a step of 1 V. We applied the drain and source voltage scans from 0 to 7 V. The drain current is increased gradually within 1 V between the drain and the source, and a clear saturation region was observed. This behavior demonstrates the rapid switching ability from off-state to on-state of the transistor device. Figure 6 shows that the saturation current exceeds 1.5 µA at a low back-gate voltage of 10 V, demonstrating the current driving ability in the AZO-based MOSFET device. However, a nonlinear correlation between V_{DS} and I_{DS} was also observed at lower V_{DS}. This behavior may be due to the parasitic resistance induced by the trap states around the source and drain regions, which leads to the occurrence of the current crowding phenomenon and reduces the drain voltage.[33] All the electrical characteristic measurements of the devices were performed under ambient conditions because of the limitation of our setup. We are also expecting that oxygen may be adsorbed on the top of the channel and form a depletion layer. This can also cause the current crowding phenomenon.

CONCLUSIONS

In this work, we have studied the influence of growth temperature on the performance of different types of high κ dielectrics such as HfO_2, ZrO_2, and Al_2O_3 thin films deposited by the ALD technique. Atomic force microscopic study reveals that the topography of the film surfaces grown at 150 °C looks very smooth with an rms roughness value of less than 1 nm. However, the surface roughness values of the films increase with higher growth temperatures around 250 °C. The J–V curve reveals that films show improved leakage current densities. Frequency-dependent C–V curves of all MOSCAP devices show very stable electrical behavior with clear formation of accumulation, depletion, and inversion regimes during the voltage sweep. Finally, the fabricated MOSFET device based on the Al-doped ZnO channel layer shows excellent electrical characteristics, and it is observed that the drain current of the device saturates at low voltage, which leads to the consumption of low power during its operation.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Kelsea A. Yarbrough: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Project administration (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Makhes K. Behera**: Conceptualization (equal); Data curation (equal); Investigation (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Jasmine Beckford**: Conceptualization (equal); Investigation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Sangram K. Pradhan**: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Messaoud Bahoura**: Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] S. De Gendt, C. Adelmann, A. Delabie, L. Nyns, G. Pourtois, and S. Van Elshocht, ECS Trans. **13**, 3 (2008).

[2] A. Duba, V. Jaggi, A. Verma, A. Mishra, and B. Scholar, Int. J. Eng. Res. **2**, 732 (2013).

[3] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature **406**, 1032 (2000).

[4] A. A. Demkov, Phys. Status Solidi B **226**, 57 (2001).

[5] Y.-C. Yeo, T.-J. King, and C. Hu, Appl. Phys. Lett. **81**, 2091–2093 (2002).

[6] R. B. van Dover, M. L. Green, L. Manchanda, L. F. Schneemeyer, and T. Siegrist, Appl. Phys. Lett. **83**, 1459 (2003).

[7] E. Atanassova and D. Spasov, Microelectron. Reliab. **42**, 1171 (2002).

[8] D. Nirmal, P. V. Kumar, D. Joy, B. K. Jebalin, and M. Kumar, in *IEEE 5th Nanoelectronics Conference (INEC)* (IEEE, 2013), pp. 12–19.

[9] K. Yim, Y. Yong, J. Lee, K. Lee, H.-H. Nahm, J. Yoo, C. Lee, C. S. Hwang, and S. Han, NPG Asia Mater. **7**, e190 (2015).

[10] N. K. Patel and A. Toriumi, Appl. Phys. Lett. **64**, 1809 (1994).

[11] K. F. Schuegraf and C. Hu, Semicond. Sci. Technol. **9**, 989 (1994).

[12] H. C. Card, Solid State Commun. **14**, 1011 (1974).

[13] S. Zafar, Q. Liu, and E. A. Irene, J. Vac. Sci. Technol. A **13**, 47 (1995).

[14] J. Liu, J. Li, J. Wu, and J. Sun, Nanoscale Res. Lett. **14**, 154 (2019).

[15] J. Robertson and R. M. Wallace, Mater. Sci. Eng., R **88**, 1–41 (2015).

[16] W. Chen, W. Ren, Y. Zhang, M. Liu, and Z.-G. Ye, Ceram. Int. **41**, S278–S282 (2015).

[17] C. S. Hwang and H. J. Kim, J. Mater. Res. **8**, 1361 (1993).

[18] P. Singh, R. K. Jha, R. K. Singh, and B. R. Singh, J. Vac. Sci. Technol. B **36**, 04G101 (2018).

[19] T. J. Bright, J. I. Watjen, Z. M. Zhang, C. Muratore, and A. A. Voevodin, Thin Solid Films **520**, 6793 (2012).

[20] S. Pandey, P. Kothari, S. Verma, and K. J. Rangra, J. Mater. Sci.: Mater. Electron. **28**, 760–767 (2017).

[21] S. Pandey, P. Kothari, S. K. Sharma, S. Verma, and K. J. Rangra, J. Mater. Sci.: Mater. Electron. **27**, 7055–7061 (2016).

[22] A. Obstarczyk, D. Kaczmarek, M. Mazur, D. Wojcieszak, J. Domaradzki, T. Kotwica, and J. Morgiel, J. Mater. Sci.: Mater. Electron. **30**, 6358–6369 (2019).

[23] X. Cui, K. Tuokedaerhan, H. Cai, and Z. Lu, Coatings **12**, 439 (2022).

[24] M. Liu, Q. Fang, G. He, L. Li, L. Q. Zhu, G. H. Li, and L. D. Zhang, Appl. Phys. Lett. **88**, 192904 (2006).

[25] Z. Li, Y. Xin, Y. Liu, H. Liu, D. Yu, and J. Xiu, Coatings **11**, 389 (2021).

[26] R. Mroczyński and R. B. Beck, Microelectron. Reliab. **52**, 107 (2012).

[27] B.-E. Park, I.-K. Oh, C. Mahata, C. W. Lee, D. Thompson, H.-B.-R. Lee, W. J. Maeng, and H. Kim, J. Alloys Compd. **722**, 307–312 (2017).

[28] K.-M. Kim, J. S. Jang, S.-G. Yoon, J.-Y. Yun, and N.-K. Chung, Materials **13**(9), 2008 (2020).

[29] M. L. Huang, Y. C. Chang, Y. H. Chang, T. D. Lin, J. Kwo, and M. Hong, Appl. Phys. Lett. **94**, 052106 (2009).

[30] S. Uthana and G. Rao, Appl. Phys. Lett. **1451**, 242 (2012).

[31] N. P. Maity, A. Kumar, R. Maity, and S. Baishya, Procedia Mater. Sci. **5**, 1198 (2014).

[32] V. Fomenko, E. P. Gusev, and E. Borguet, J. Appl. Phys. **97**, 083711 (2005).

[33] J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, J. Electrochem. Soc. **155**, H873 (2008).