Characterizing losses in InAs two-dimensional electron gas-based gatemon qubits

William M. Strickland,[1] Lukas J. Baker,[1] Jaewoo Lee,[1] Krishna Dindial,[1] Bassel Heiba Elfeky,[1] Patrick J. Strohbeen,[1] Mehdi Hatefipour,[1] Peng Yu,[1] Ido Levy,[1] Jacob Issokson,[1] Vladimir E. Manucharyan,[2] and Javad Shabani[1]
[1]*Center for Quantum Information Physics, Department of Physics, New York University, New York, New York 10003, USA*
[2]*Institute of Physics, École Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland*

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The tunneling of Cooper pairs across a Josephson junction (JJ) allows for the nonlinear inductance necessary to construct superconducting qubits, amplifiers, and various other quantum circuits. An alternative approach using hybrid superconductor-semiconductor JJs can enable superconducting qubit architectures with all electric control. Here we present continuous-wave and time-domain characterization of gatemon qubits and coplanar waveguide resonators based on an InAs two-dimensional electron gas. We show that the qubit undergoes a vacuum Rabi splitting with a readout cavity, and we drive coherent Rabi oscillations between the qubit ground and first excited states. We measure qubit relaxation times to be $T_1 = 100$ ns over a 1.5 GHz tunable band. We detail the loss mechanisms present in these materials through a systematic study of the quality factors of coplanar waveguide resonators. While various loss mechanisms are present in III-V gatemon circuits, we detail future directions in enhancing the relaxation times of qubit devices on this platform.

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I. INTRODUCTION

The superconducting qubit is a hallmark solid-state system that displays quantum coherence and strong light-matter coupling [1–4]. Recently, the coherence times of planar transmon qubits have exceeded 300 μs [5], and further improvements are expected with improved materials and fabrication [6]. A common design choice is to introduce flux tunability of a qubit or coupler for fast, high-fidelity single-qubit control and two-qubit gates [7,8], almost exclusively realized by flux-sensitive superconducting quantum interference devices (SQUIDs) [9–12]. An architecture based on flux-biased SQUIDs may lead to future complications, however. The heat load induced by milliampere-level currents flowing through resistive wires can impose substantial cooling requirements as the scale of superconducting qubit chips increases. Stray magnetic fields in higher-density qubit arrays can also cause irremediable crosstalk. In addition, low-frequency $1/f$-type flux noise can limit the dephasing times of flux-tunable qubits, and its origin and mitigation is an active area of research [13–17]. An all-electric tunability scheme may prove to be beneficial in large-scale quantum processors, and JJs based on hybrid superconductor-semiconductor (S-Sm) materials are one interesting candidate to realize this.

A hybrid S-Sm Josephson junction device has current flow facilitated by Andreev bound states in the semiconductor weak-link. By biasing with an applied gate voltage, one can tune the Fermi level in the semiconductor and the occupation of Andreev bound states, effectively controlling the conduction through the junction. It was shown that InAs makes an excellent candidate for the semiconductor in a hybrid S-Sm junction because it makes an Ohmic contact with superconducting metals such as Al [18]. It was discovered later that thin films of Al (111) can grow epitaxially on InAs (100) by molecular beam epitaxy [19–21], enabling a high-quality contact [22–24] on a wafer-scale. The incorporation of an S-Sm junction in a superconducting qubit was first demonstrated in Refs. [25,26] using an InAs nanowire, and voltage tunable Josephson junctions have since made many appearances in qubits [25–36], couplers [37–44], and other elements, such as an amplifiers and nonreciprocal elements [45–47]. Of note, a wafer-scale architecture was implemented in the form of an InAs two-dimensional electron gases (2DEG) in Ref. [27], making the qubit processing more amenable to bottom-up fabrication. Since the work in Ref. [27], enhancements in coherence times of gatemon qubits based on an InAs 2DEG has been slow in recent years, mainly due to difficulties in device fabrication. For this reason, it is useful to consider new ways to fabricate InAs 2DEG-based gatemon qubits using simplified fabrication procedures and analyze their effects on fabrication yield and device performance. While this has significantly prevented the wider adoption of the 2DEG-based gatemon qubit architecture, the prospect of using the voltage tunable junction in tunable couplers between qubits to implement low power, fast two-qubit gates could lead to a near-term potentially useful and interesting material platform to study and integrate with state-of-the-art superconducting qubits.

We report on the progress in developing qubits based on hybrid S-Sm materials. The article is organized as follows: In Sec. II we report on coherent manipulation of InAs 2DEG-based gatemon qubits. The observed qubit frequency is tunable over 1.5 GHz and the qubit undergoes a vacuum Rabi

splitting with the readout resonator. Coherent Rabi oscillations are driven between the ground and first excited states of the qubit, and by fitting the decay of these oscillations we find that the characteristic timescale of the decay T_2^{Rabi} is 97 ns. The energy relaxation times T_1 of gatemon qubits over a wide gate voltage range are found with a maximum $T_1 = 102$ ns, where T_1 generally increases with decreasing qubit frequency. In Sec. III, a systematic study of the various loss mechanisms in gatemon circuits, such as dielectric loss from two-level systems and inductive loss, is performed by analyzing quality factors of coplanar waveguide (CPW) resonators. We measure a variety of samples with varying Al film thicknesses, and we find that the highest measured quality factor at low power is 4×10^4, suggesting that current qubit devices are limited by inductive loss in the superconductor. Finally in Sec. IV, we outline future steps to enhance gatemon T_1 times.

II. QUBIT MEASUREMENTS

A detailed outline of the fabrication procedure can be found in Fig. 1, and further details are outlined in Appendix A. The InAs quantum well is grown by molecular beam epitaxy and capped with a 30 nm Al layer *in situ*. Patterning is done by electron beam lithography, and chemical wet etching defines the circuit. The qubit chip consists of four isolated qubits, each with a readout resonator, drive line, and gate. the resonators are coupled to a common feedline. Details of the device design can be found in Appendix B. We note that there are a number of changes made in the fabrication procedure here that greatly improve device yield and consistency, including the blanket gate dielectric layer, including the III-V buffer layers under the qubit capacitor, and using a thin Al layer in qubit capacitor. A more detailed comparison is provided in Appendix A.

Measuring the complex transmission $|S_{21}|$ across the feedline as a function of frequency, four sharp dips in magnitude at distinct frequencies can be seen, as shown in Fig. 2(a), corresponding to each of the four readout resonators on the chip labeled according to their placement on the chip from left to right. We focus our study on the qubit coupled to resonator R3. Sweeping the top gate voltage V_G, and measuring the transmission near the frequency of resonator R3, we find that the qubit and readout resonator modes exhibit a vacuum Rabi splitting, where the splitting in frequency is equal to $2g/2\pi$. This can be seen in Fig. 2(b), where the minimum detuning of the two modes is noted. The bare frequencies of the two modes as a function of gate voltage are shown as white dashed lines. Extracting the measured coupling strength, we find that $g/2\pi = 95$ MHz, within 15% of the value expected from finite-element simulations.

We then perform dispersive measurements of the qubit state [4]. In a coupled qubit-resonator system in the dispersive regime, with large coupling and detuning $g/\Delta \ll 1$, we expect the readout resonator frequency to have a qubit state-dependent frequency, $f_r \pm \chi$, where χ is the dispersive shift. Thus, for a sufficiently small linewidth $\kappa \lesssim \chi$, a measurement of the transmission through the resonator would allow for the unique determination of the qubit state.

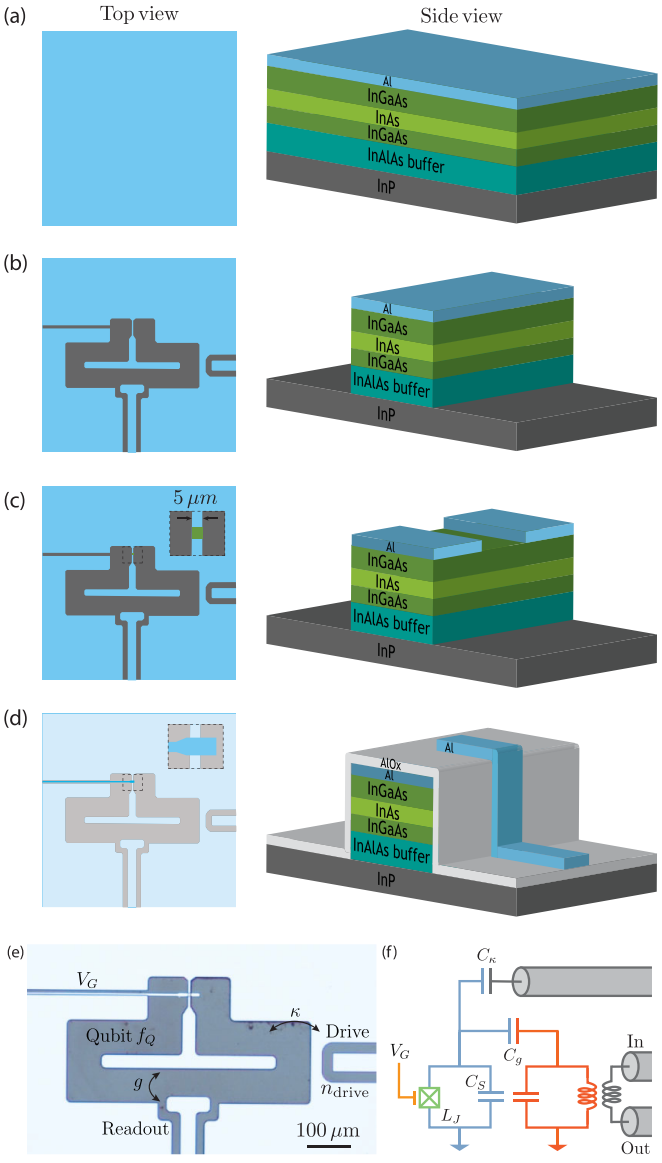

FIG. 1. Fabrication procedure and optical image: The left column shows a top view of the surface, while the right column shows the side view, where each layer is clearly visible and noted. The layer structure is shown in (a) where layers of InAlAs (teal), InAs/InGaAs (green/dark green), and Al (blue) are grown on an InP substrate (gray). The Al and III-V layers are etched in order to define the microwave circuit as shown in (b). The Josephson junction shown in (c) is then defined with an Al etch. The width of the superconducting electrodes is nominally 5 μm, and they are separated by 100 nm (not to scale). We then blanket deposit a layer of AlO_x (white), pattern the gate electrodes, and deposit an Al gate electrode, as shown in (d). An optical image of the device after fabrication is shown in (e). The qubit has a characteristic frequency f_Q controlled by the gate voltage V_G and is coupled to a readout resonator with a coupling strength g, set by the coupling capacitance C_g. An external drive line is coupled with a strength of κ, set by the capacitance C_κ, which drives transitions in the qubit. The equivalent circuit diagram is shown in (f). The Josephson inductance L_J is shunted to ground by a capacitance C_S. Input and output lines are coupled inductively to the readout resonator (orange).

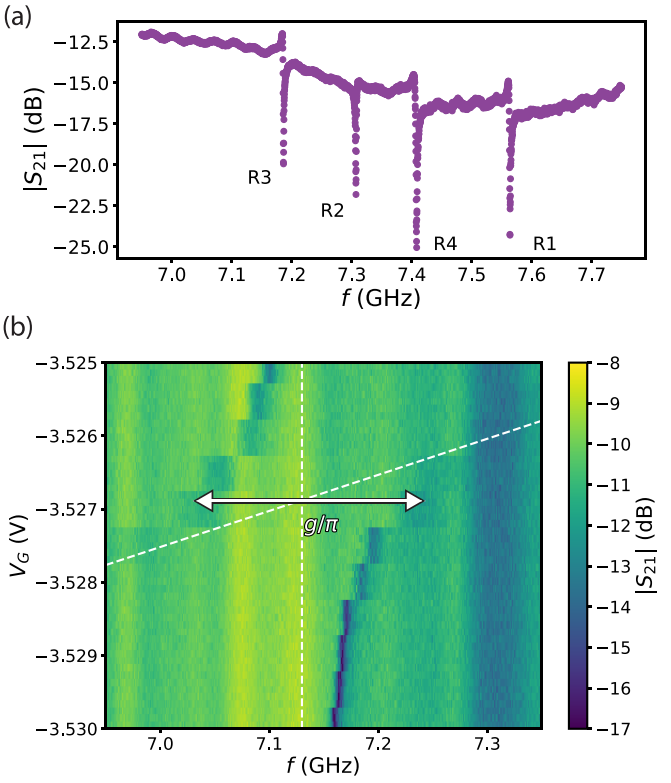

FIG. 2. Continuous-wave measurement. (a) Measuring $|S_{21}|$ across the transmission line, we find absorption at four distinct frequencies corresponding to the resonant frequencies of the readout resonators. (b) The junction gate voltage V_G tunes the qubit frequency, and near the readout resonator frequency a vacuum Rabi splitting is observed. We find that this corresponds to a coupling strength of $g/2\pi = 95$ MHz.

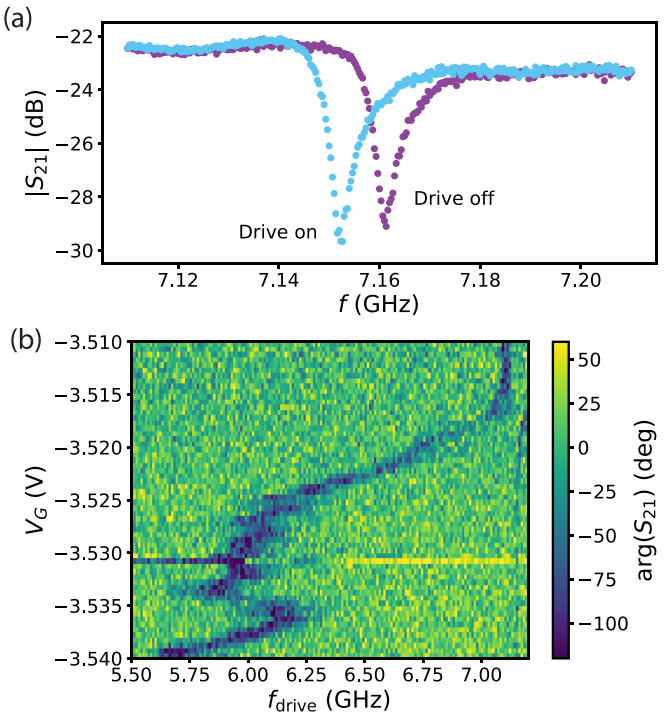

FIG. 3. Two-tone spectroscopy. (a) Applying a drive tone on the qubit at a frequency of $f_Q = 6.55$ GHz, detuned from the readout resonator by $\Delta = 610$ MHz, the readout resonator dispersively shifts when the drive is turned on. (b) Sweeping the top gate voltage V_G and applying a drive tone with varying frequency f_{drive}, we find that two-tone spectroscopy reveals the qubit response to gate voltage.

The qubit is detuned from the readout resonator by applying a gate voltage of $V_G = -3.535$ V and the transmission across the feedline at the resonant frequency of R3. Sweeping the frequency of the drive tone at a power of $P_{\text{drive}} = -36$ dBm, we find that at a frequency $f_{\text{drive}} = 5.62$ GHz, the readout resonator exhibits a shift down in frequency corresponding to the excitation of the qubit $|0\rangle$ to $|1\rangle$ transition. This can be seen in Fig. 3(a), where we measure a shift of 8.66 MHz between the resonator frequency when the drive is on. The continuous microwave tone incoherently drives the qubit $|0\rangle$ to $|1\rangle$ transition, therefore shifting the readout resonator by less than 2χ.

We then repeat this measurement while sweeping the gate voltage, modifying the current through the junction and thus the qubit frequency. As shown in Fig. 3, we find that the observed qubit frequency generally decreases with gate voltage, which is expected for decreasing critical current with decreasing gate voltage. We find wide tunability > 1 GHz of the qubit frequency via gate voltage. Furthermore, the qubit response to gate voltage is nonmonotonic and is similar to what has been observed in the past for gatemon qubits in Refs. [25–27,32,36]. It was discussed in Ref. [32] that in an InAs nanowire device, at very small junction critical currents on the order of 10 nA, the junction becomes subject to universal conductance fluctuations.

A two-level quantum system undergoes Rabi oscillations when driven at the transition frequency between the two levels, where the final qubit state depends on the width of the drive pulse τ_{Rabi}. We measure the dynamics of the qubit in the time domain by coherently driving Rabi oscillations and measuring the characteristic lifetime.

Shown in Fig. 4(a) is the homodyne detection voltage measured as pulses of varying widths are sent to the drive line of the qubit. The qubit is set to a frequency of $f_{01} = 6.56$ GHz with the gate voltage set to $V_G = -3.530$ V. As we vary the drive pulse width, V_H oscillates, periodic in the pulse width τ_{Rabi}. We find that the frequency of these oscillations decreases with decreasing power, as is expected for Rabi oscillations. Fitting the data at $P_{\text{drive}} = -52.5$ dBm with the method of least squares, we extract a time constant of $T_2^{\text{Rabi}} = 97$ ns. There are four free parameters in the fits to Rabi oscillations: the time constant characterizing the exponential decay T_2^{Rabi}, the oscillation frequency, and the slope and y-intercept of the decaying contribution. This linear contribution to the signal V_H was identified in Ref. [36] and could possibly be due to leakage into higher levels [48]. In Fig. 4(c) we plot the extracted Rabi frequency in blue markers versus the square root of the drive power. It is seen that at the low power regime, the frequency follows $\sqrt{P_{\text{drive}}}$, shown as an orange line.

By calibrating the pulse width to half a Rabi period, the qubit is coherently driven to the $|1\rangle$ state. By then measuring the decay to the $|0\rangle$ state averaged over many

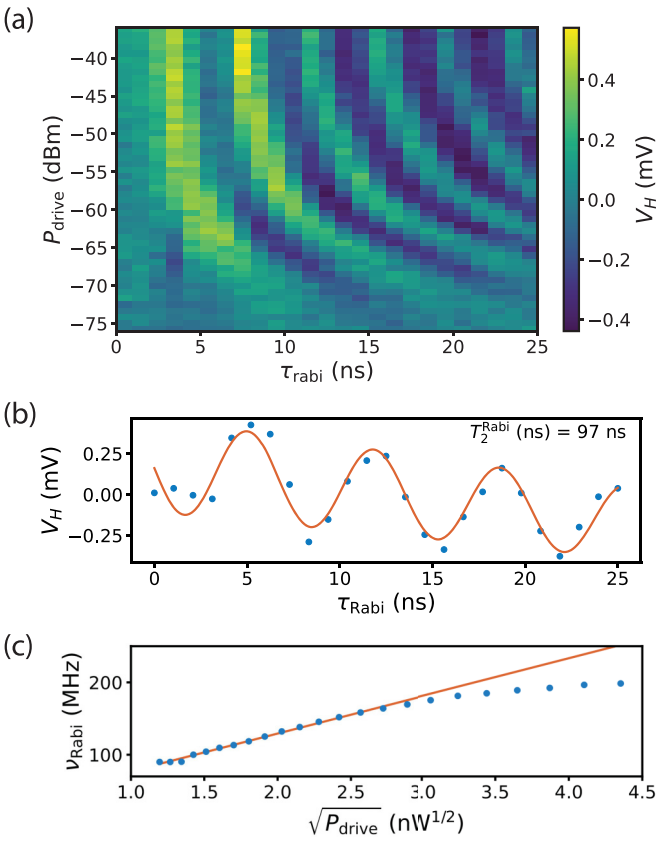

FIG. 4. Rabi oscillations: (a) Homodyne detection voltage V_H as a function of Rabi pulse width τ_{Rabi} with the drive power P_{drive} varied. (b) Fitting a line cut of the data in (a) at a power of −52.5 dBm to a decaying sinusoid. We find a time constant $T_2^{\text{Rabi}} = 97$ ns characterizing the coherence. (c) Extracting Rabi oscillation frequency ν_{Rabi} at different drive powers, we find at low power that the data fit roughly to $\sqrt{P_{\text{drive}}}$. At high power, the data deviate from the expected square root dependence, possibly due to high-power nonlinearities.

runs, the characteristic time of this decay T_1 can be extracted. At a qubit frequency of $f_Q = 6.51$ GHz, we apply a 10-ns-wide pulse with a drive power of $P_{\text{drive}} = -41$ dBm and average over 2×10^5 runs. The decay of the measured signal V_H is fit to a decaying exponential, and we extract a time constant of $T_1 = 102 \pm 18$ ns as shown in the inset of Fig. 5(a).

We measure T_1 over a range of gate voltages and qubit frequencies. As shown in Fig. 5(a), the qubit frequency f_Q again exhibits a nonmonotonic tuning between 6.5 and 5.2 GHz over the gate voltage range $-3.545 < V_G < -3.535$ V, similar to the two-tone measurement in Fig. 3(b). We note that inconsistencies between qubit frequency dependence on gate voltage are primarily due to hysteresis in the applied gate voltage. This behavior has been studied in detail in Ref. [49], where it was found that the cause is from charge traps at the semiconductor-metal oxide interface. We find that the measured T_1 also vary over this range, generally increasing with decreasing qubit frequency. To understand further the spread of T_1 versus frequency, we measure CPW resonators as a proxy for qubit lifetime.

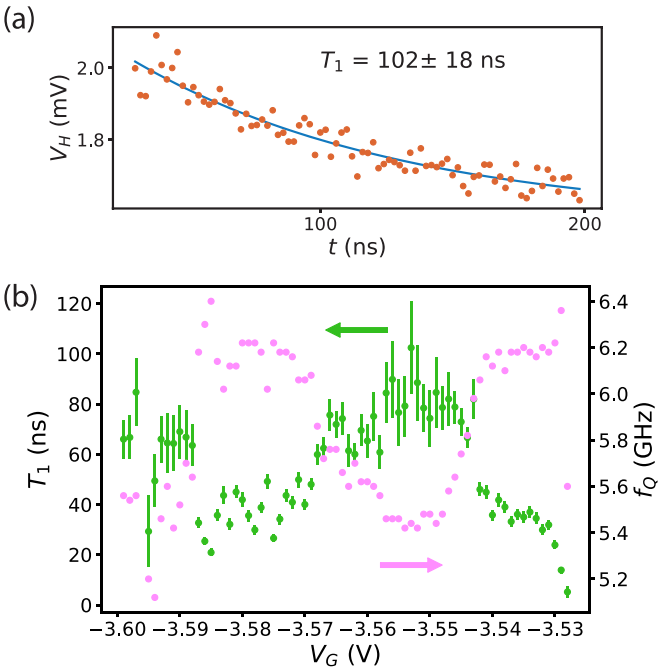

FIG. 5. T_1 measurements. (a) Applying a pi pulse and measuring in time t we find that the decay of the qubit state can be fit to an exponential to extract the time constant for qubit decay $T_1 = 102$ ns. The T_1 measurement is repeated over a range of gate voltages. (b) Qubit T_1's (green) and frequencies (pink) as a function of gate voltage.

III. LOSS MECHANISMS

Qubit and resonator loss can be decomposed into a sum of contributions from various loss mechanisms, including dielectric, inductive, quasiparticle, and radiative losses [50]. In the following section, we detail a systematic study of loss in CPW resonators in order to understand the role of inductive and dielectric loss in our qubit devices.

We consider a loss model that takes into account inductive and dielectric losses

$$\frac{1}{Q_{\text{int}}} = \sum_i p_i \tan\delta_i + \alpha \frac{1}{Q_S} + \frac{1}{Q_0}. \tag{1}$$

The first term is due to dielectric loss, where for a given interface or volume i, p_i is the participation ratio of that layer, being the integral of the electric field squared in each layer normalized to the integral over all space of the electric field squared. The dielectric loss of that layer is $\tan\delta_i$. The second term characterizes inductive losses. The prefactor α is the kinetic inductance fraction, which is related to the London penetration depth λ and the ratio of the surface-to-volume magnetic field energy p_{mag} through $\alpha = \lambda p_{\text{mag}}$. The surface quality factor Q_S is related to dissipative conduction in the superconductor,

$$Q_S = \frac{\omega\mu\lambda}{R_S} = \frac{X_S}{R_S}, \tag{2}$$

where R_S, the surface resistance, and X_S, the surface reactance, are the real and imaginary parts of the surface impedance, respectively. These quantities are both functions of the

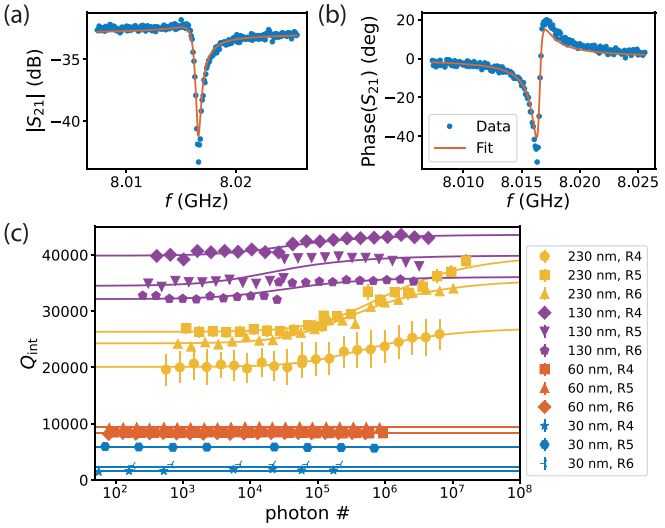

FIG. 6. Internal quality factors and power dependence. The amplitude and phase of the transmission S_{21} are shown in (a) and (b) as well as fits shown as solid lines. From the fits we are able to extract f_r and Q_{int}. (c) Internal quality factors vs number of photons in the cavity for resonator devices with varying Al thicknesses. Devices on thick Al films (130 and 230 nm) can be seen to exhibit some power dependence, and are fit to a model of loss following two-level systems (solid lines), while thin Al films (30 and 60 nm) show power-independent loss, suggesting that the total loss is dominated by power-independent loss mechanisms, such as inductive loss.

temperature T. This loss model is applied to measurements of the internal quality factor Q_{int} of CPW resonators. Six resonators are fabricated on each chip in a hanger style with a common feedline. In certain devices, some resonators are unable to be identified in large range transmission measurements due to errors in fabrication, such as the presence of scratches or contaminants. Figures 6(a) and 6(b) show the magnitude and phase of S_{21} at a frequency near the resonant frequency of R6 from the 130 nm sample. Fits are conducted using the circle fitting method detailed in Ref. [51].

A. Dielectric losses

Two-level systems (TLSs) have been known to limit device performance in many high coherence qubits, and the microscopic origin of TLSs in superconducting devices is an active area of research. We fit power dependence of the quality factor to the noninteracting TLS model [52],

$$\frac{1}{Q_{\text{int}}(n)} = \frac{1}{Q_0} + \frac{1}{Q_{\text{TLS}}} \frac{\tanh\left(\frac{\hbar\omega}{2k_B T}\right)}{\sqrt{1+\frac{n}{n_c}}}. \tag{3}$$

Here Q_0 takes into account power-independent loss mechanisms, $1/Q_{\text{TLS}}$ is the associated TLS loss, and the ratio n/n_c is the average number of photons in the cavity over some critical photon number at which TLSs start to get saturated.

The results are shown in Fig. 6, where we include data from three devices (R4, R5, and R6) from four different samples (Al thicknesses of 30, 60, 130, and 230 nm). We find that the samples with thicker Al have larger internal quality factors, consistent with the expectation that thicker films mitigate inductive loss, as will be expanded on in the next subsection. We also find that in samples with 130- and 230-nm-thick Al, Q_{int} decreases with the number of photons in the cavity, which is consistent with the expectation from two-level system loss. By fitting this data to Eq. (3), we are able to extract Q_0, Q_{TLS}, and n_c. These results are featured in Table I. Samples with thinner Al show power-independent loss, which indicates that other power-independent loss mechanisms, such as inductive loss, dominate the total measured loss. The plotted traces for the 30- and 60-nm-thick films are simply the average Q_{int} measured over the whole power range.

We find that the samples with 130 and 230 nm Al have Q_0 in the range of 2.7–4.4 $\times 10^4$. This is consistent with loss measurements on GaAs substrates, where the limits to coherence were shown to be due to the piezoelectricity of III-V substrates [50,53]. The values extracted for Q_{TLS} varied between the samples, being around 1.4–2.4 $\times 10^3$ for the 130 nm Al sample, and 4.0–6.0 $\times 10^2$ for the 230 nm sample. The lower Q_{TLS} observed for the 230 nm sample is possibly due to insufficient cleaning of the sample surface after the III-V buffer layer etch.

B. Inductive losses

As the temperature is varied, the real and imaginary components of surface impedance cause changes to the resonant frequency and quality factor of a CPW resonator [54]. The complex impedance $Z_S = R_S + j\delta X_S$ follows:

$$Z_S(T) = \frac{\omega\mu_0\lambda}{p_{\text{mag}}}\left(\frac{1}{Q} + 2j\frac{\delta f}{f}\right). \tag{4}$$

We apply a similar procedure to fit temperature dependence data as is described in Refs. [55,56], and a description of the fitting procedure can be found in Ref. [56].

Using this equation for the fractional frequency shift, it is possible to fit the data as a function of temperature in order to extract the kinetic inductance fraction α and the superconducting gap Δ.

We measure S_{21} at varying temperatures and study the resonant frequency and the quality factor change as a function of temperature. The data were taken with the sample at the base temperature of 15 mK and increased to a maximum temperature of 800 mK. Before the data were taken at each temperature, a 30 min dwell time was applied to allow the temperature to equilibrate. The results can be seen in Figs. 7(a) and 7(b). We show one resonator (R6) from three devices with varying Al film thicknesses: 60, 130, and 230 nm. Data from a fourth CPW are included with a different resonant frequency and coupling to the feedline, but identical center width and gap. We then fit the change in resonant frequency to the Mattis-Bardeen theory detailing the change in the complex surface impedance as a function of temperature. It can be seen that the measured Q_{int} of R6 for the 130-nm-thick Al sample is lower than that in Fig. 6(c), possibly because the temperature dependence measurement was conducted on a different cooldown, and between the power and temperature sweeps the sample was kept in ambient conditions for approximately one month.

In all devices a decrease in frequency with temperature is seen, consistent with the Mattis-Bardeen theory. We also

TABLE I. Summary of the results for CPW resonators with varying thicknesses of Al. On each chip, the resonators identified in a broad frequency scan are included. The Al thickness denotes the sample, being 30 nm of epitaxial Al plus an additional thickness of sputtered Al. The measured frequency f_r is shown for the given devices indexed as R1 for the lowest frequency resonator by design, for example. Fits to the TLS model allow us to extract the power-independent quality factor Q_0, the quality factor associated with two-level system loss Q_{TLS}, as well as the critical photon number n_c. Fits to the Mattis-Bardeen theory for the temperature dependence of f_r allow us to extract the kinetic inductance fraction α, and subsequently the London penetration depth λ.

Al thickness	Resonator	f_r (GHz)	Q_0 ($\times 10^3$)	Q_{TLS}($\times 10^3$)	n_c ($\times 10^4$)	α (%)	$L_k^{\square}$ (pH)	λ (nm)
30 nm		8.304	3.48			7.60	1.2248	164
30 nm	R1	5.835	7.45					
	R2	6.107	1.70					
	R3	6.306	1.55					
	R4	6.737	5.87					
	R6	7.412	2.36					
60 nm	R1	6.140	7.52			5.29	0.853	137
	R2	6.396	8.37			4.24	0.683	122
	R4	7.061	8.39			4.85	0.782	131
	R5	7.413	9.39			4.24	0.683	122
	R6	7.808	8.30			4.69	0.756	129
130 nm	R4	7.244	43.6	2.43	1.30	1.29	0.208	66
	R5	7.605	39.9	1.40	0.733	1.30	0.210	66
	R6	8.017	36.1	1.70	1.20	1.36	0.219	68
230 nm	R1	6.278	31.5	0.547	13.0	1.24	0.200	65
	R2	6.551	34.8	0.606	12.9	1.39	0.224	69
	R4	7.215	27.1	0.404	14.7	1.38	0.222	69
	R5	7.587	40.0	0.421	22.5	1.32	0.213	67
	R6	7.972	35.6	0.438	8.83	1.31	0.211	67

find that the temperature at which the frequency starts to change decreases with decreasing film thickness. We fit each data set to the Mattis-Bardeen theory in order to extract the kinetic inductance fraction α while simultaneously fitting for the superconducting gap Δ where we consistently find

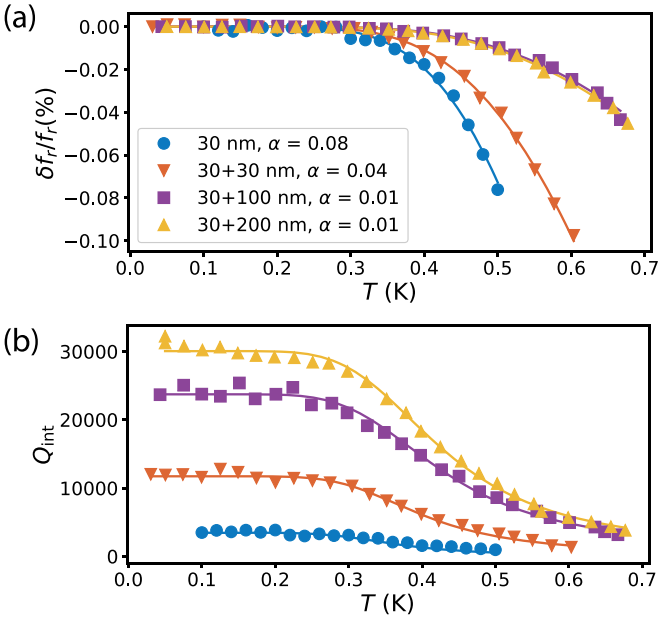

FIG. 7. Temperature dependence. Percent change in frequency in (a) and Q_{internal} in (b) as a function of temperature with fits to the Mattis-Bardeen model (solid lines) for the four different Al thicknesses.

$\Delta \approx 210\,\mu$eV for all films, similar to what has been seen in the past for thin Al films [23]. The fit results show that α systematically decreases as the thickness increases. For the epitaxial Al film, $\alpha = 7.6\%$. For the film 60-nm-thick Al, the kinetic inductance decreases to around 4.2–5.3%. For the 130 nm film and the 230 nm film, the kinetic inductance saturates at around 1.2–1.4%. Multiple resonators on the same sample show similar results for α to within 20% of each other for the 60 nm sample and within 10% of each other for the 130 and 230 nm samples.

Most notable are the measured internal quality factors versus Al film thickness. CPWs on the thinnest Al film had the lowest measured $Q_{\mathrm{int}} = 3.5 \times 10^3$. The sample with 60-nm-thick Al had internal quality factors between 1.6 and 7.5×10^3, while the 130 nm sample had Q_{int} in the range of 35–45 $\times 10^3$. The 230 nm sample showed similar Q_{int} to that of the 130 nm sample between 27 and 40 $\times 10^3$. The results are summarized in Table I.

As the film thickness of aluminum decreases, the London penetration depth increases from its bulk value of 50 nm [57]. In the regime where the film thickness becomes less than the London penetration depth, the kinetic inductance becomes significantly enhanced, as seen in our devices. As detailed in Refs. [58,59], one is able to relate the kinetic inductance per square $L_k^{\square}$ of a thin film to the London penetration depth through

$$L_k^{\square} = \mu_0 \lambda \coth\left(\frac{d}{\lambda}\right), \tag{5}$$

where d is the film thickness. With an accurate measure α and the characteristic impedance of the CPW, we are able to find $L_k^{\square}$ and thus the London penetration depth. The results

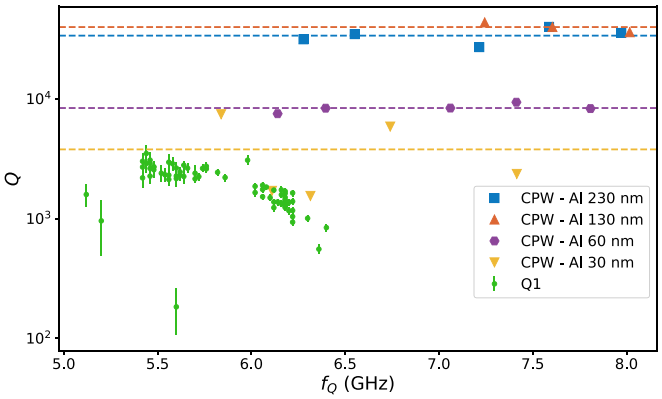

FIG. 8. Quality factors of CPW resonators and qubits: The qubit quality factor $Q = 2\pi f_Q T_1$ and the low power resonator quality factor is plotted vs frequency. Dashed lines are the average quality factor over each sample on each chip.

are shown in Table I. We find that for the 230 and 130 nm films, the London penetration depths are close to the expected bulk value of aluminum, being between 65 and 70 nm for all devices. For the 60 nm sample, the penetration depth increases to around 125 nm, making $\lambda > d$ for this film. Finally, for the 30 nm Al film, we find that the penetration depth is 160 nm, even further in the $\lambda > d$ regime, with λ more than five times larger than the film thickness.

IV. DISCUSSION

In this section, we compare the measured loss of CPWs to the gatemon qubit presented in the earlier section of this article. In Fig. 5(b) we plot the measured T_1 values in terms of an equivalent qubit quality factor, $Q = 2\pi f_Q T_1$, as a function of qubit frequency f_Q. We compare the measured qubit quality factors to low power measurements of Q_{int} of the CPWs. It is clearly seen that the observed qubit Q is lower than all measured CPWs, and closest to Q_{int} measured for the 30-nm-thick Al sample.

We believe there are two main differences in the fabrication procedure of the highest Q CPW resonators and that of gatemon qubits that decrease the measured qubit Q (see Fig. 8). The first reason is the thin 30 nm Al used in the gatemon qubit, which, as we have shown, could introduce a considerable amount of inductive loss. The second difference is the use of a blanket AlOx layer, which is known to have loss tangents in the $\tan\delta \sim 1 \times 10^3$ range. In a separate measurement we found that a sample with thick Al and blanket AlOx had Q reduced to around 1.2×10^4. This suggests that the limit set by inductive loss of a thin Al film dominates the observed qubit loss, but is enough to substantially decrease the Q of CPWs with thick Al. These two aspects would account for the differences in measured T_1 between our work and that in Ref. [27] as well. We note that while the presence of a buffer layer under the resonator central conductor did not affect internal quality factors, and the effective T_1, it may still be detrimental for T_2 due to the presence of background impurities causing charge noise dephasing.

The CPW measurements presented here detail immediate next steps to enhance gatemon relaxation times by reducing inductive and capacitive losses. Dielectric loss from the blanket AlO_x layer can be reduced by patterning and lifting off the gate dielectric, or by using hexagonal boron nitride, a low-loss, small form factor gate dielectric [60,61]. To reduce inductive losses, a thicker *in situ* Al layer can be deposited, or a thick, low-loss superconducting layer can be deposited *ex situ* via sputtering, given sufficient cleaning before the deposition. Decreasing inductive losses in the superconducting film will also manifest as decreased Purcell loss through the readout resonator. We note that inductive loss in the junction, radiative loss through the gate line, and quasiparticle loss may also play a role in limiting qubit quality factors [56].

We believe that further surface preparation optimization can be done in order to reduce TLS loss in future devices. It has been shown in the past that various etching recipes yield different device performance results [62]. We plan to investigate different types of acid etching in order to passivate the surfaces both before deposition and during the patterning of the devices. It is also unclear what the effect of the ion milling is on the sample surface, and whether a shorter or longer ion mill will lead to higher quality factor devices.

In making devices with coherence times greater than 1 μs, it may be necessary to develop new techniques to reduce the participation in the III-V layers. These can include flip-chip techniques [39], epitaxial liftoff [63], and wafer bonding to a low loss substrate such as silicon or sapphire, as well as growing III-V semiconductors directly on silicon [64].

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APPENDIX A: GROWTH AND FABRICATION

The 2DEG is realized by an InAs quantum well grown near the surface by molecular beam epitaxy. A schematic of the heterostructure is shown in Fig. 1(a). An epiready, 500-μm-thick, Fe-doped, semi-insulating InP substrate is loaded into an ultrahigh-vacuum molecular-beam-epitaxy chamber. The native oxide is thermally desorbed, followed by the growth of an $In_{0.53}Al_{0.47}/In_{0.52}Al_{0.48}$ superlattice, a 100-nm-thick $In_{0.52}Al_{0.48}As$ layer, and a 400-nm-thick $In_xAl_{1-x}As$ graded buffer layer. The composition is graded from $x = 0.52$ to 0.81. The quantum well is then grown, consisting of layers of InGaAs, InAs, and InGaAs with thicknesses of 4, 4, and 10 nm, respectively. The temperature is then lowered and a 30-nm-thick layer of Al is deposited *in situ*. Details of the growth are expanded on in detail in [65–67].

Schematics of the device fabrication process are also shown in Fig. 1, with a view of the surface shown in the left-hand panel, and a tilted, side view of the layers shown on the right panel. The process starts by dicing a 7×7 mm piece from the wafer. We use electron beam lithography to define the patterns, and polymethyl methacrylate is used as

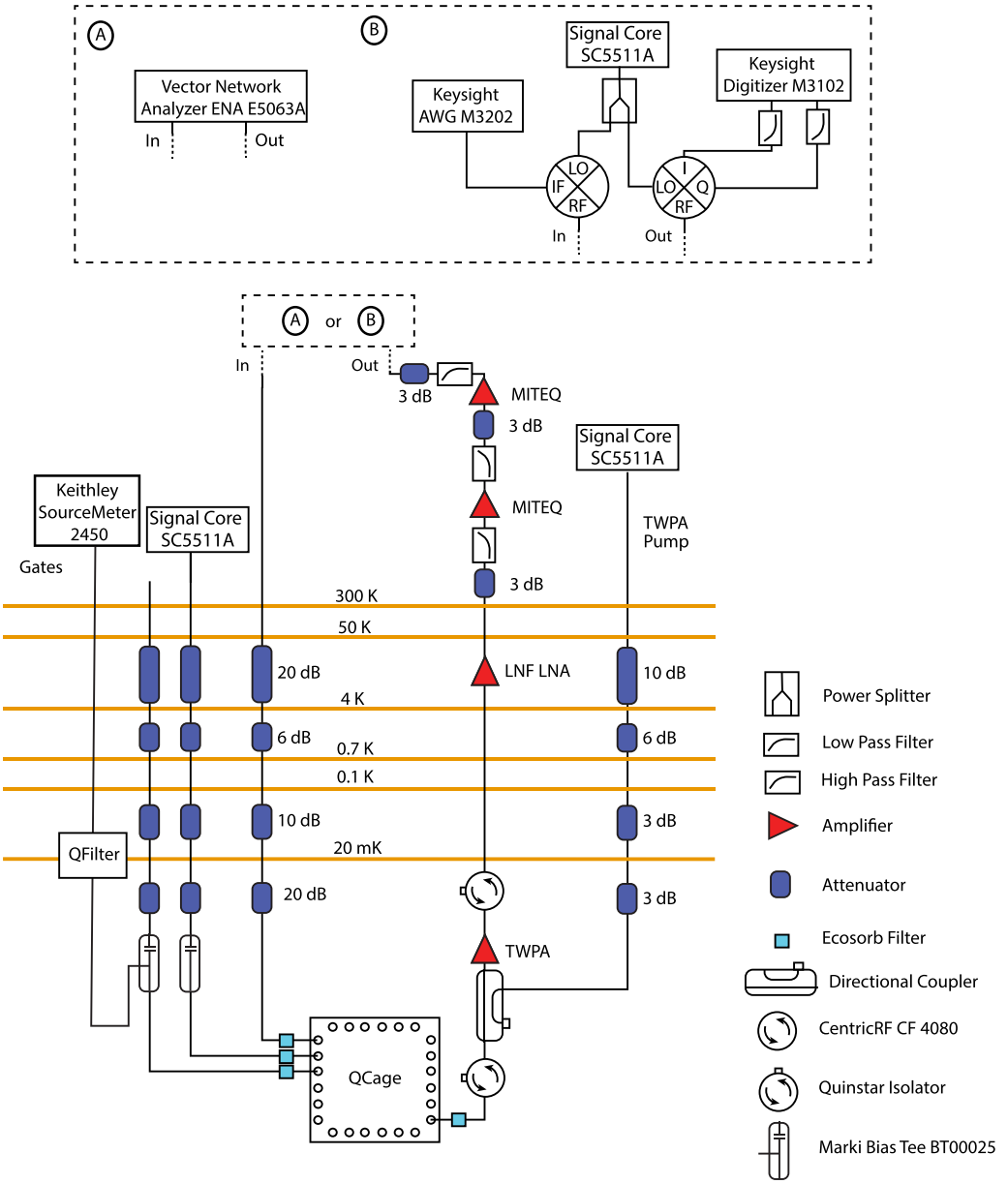

FIG. 9. Measurement setup.

electron beam resist. To etch the native Al layer, we use a wet chemical etchant Transene Type D, and to etch the epitaxial III-V layers, we use a solution consisting of phosphoric acid (H_3PO_4, 85%), hydrogen peroxide (H_2O_2, 30%), and deionized water in a volumetric ratio of 1:1:40. The first lithography and etching step defines the microwave circuit, where we etch the native aluminum layer and the III-V layers in successive steps. The resulting pattern (to scale) can be seen in Fig. 1(b). We next expose and etch a thin 100-nm-long (separation of the two aluminum leads), 5-μm-wide strip to define the planar Josephson junction. This can be seen in Fig. 1(c), where the inset of the left panel shows a zoomed-in image of the junction area (exposed semiconductor region enlarged for visibility). Following the deposition of a 40 nm blanket layer of AlO_x to serve as a gate dielectric, we pattern the gates and deposit a 50-nm-thick Al layer for the gate electrodes either by thermal evaporation or by sputtering. The AlO_x gate dielectric can be seen in Fig. 1(d) as an opaque white layer over the whole chip.

CPW devices are fabricated using the first lithography and etching step as described above, but they do not undergo the subsequent processing steps. The CPW devices differ from each other in the fact that an additional Al layer of varying thickness was deposited on three of the samples. Sputtering is done on the MBE-grown Al after an argon plasma ion milling of the sample surface at 25 W with 3 mTorr flow for 5 min prior to the deposition. We deposit Al by dc magnetron sputtering at 80 W at a rate of about 5 nm/min.

The device here can be contrasted with that in Ref. [27] in the following ways. The first is the etching of the III-V buffer layers everywhere except the junction region, whereas in our device we have included the buffer layer under the capacitor pads of our qubit. We see in our analysis of resonator quality

factor data that including the buffer layer in CPW resonators does not decrease the internal quality factor, but this could adversely affect qubit dephasing times. The second difference is the thickness of Al used for the qubit capacitors, being 100 nm in the case of Ref. [27], and 30 nm in our case. The last difference is in the gate dielectric, where we deposit a blanket layer over the whole chip, while in Ref. [27] the gate dielectric is lifted off every where except for a 1×1 μm square over the Josephson junction.

APPENDIX B: QUBIT DESIGN

We report on two chips containing four qubits and six CPW resonators, respectively. On the qubit chip, each qubit is coupled capacitively to a readout resonator, drive line, and gate electrode. The readout resonators are coupled inductively to a common feedline. An optical image of one such qubit is shown in Fig. 1(e) with an equivalent circuit diagram shown in Fig. 1(f). We use an Ansys Q3D extractor to calculate the Maxwell capacitance matrix. We find that the qubit shunt capacitance is $C_S = 62.7$ fF, giving an estimated charging energy of $E_C/h = e^2/2C_S = 309$ MHz, where e is the elementary charge and h is Planck's constant. The Josephson junction provides a nonlinear inductance L_J in parallel with a shunt capacitance. By virtue of tuning the current through the junction, the top gate electrode sets a voltage V_G which controls the qubit frequency f_Q. At a qubit frequency of $f_Q = 6$ GHz, the qubit is detuned from the readout resonator by >1 GHz, allowing for dispersive readout of the qubit state. The Josephson energy at this frequency would be $E_J = 16$ GHz, giving a ratio of $E_J/E_C = 52$, satisfying the transmon condition $E_J \gg E_C$. We note that the critical current through the Josephson junction at this frequency is $I_C = 30$ nA. A $\lambda/4$ readout resonator with a frequency of $f_r = 7.14$ GHz is coupled capacitively to the qubit with an estimated coupling strength $g/2\pi = 109$ MHz. We note that the readout resonator frequency is shifted down due to an appreciable kinetic inductance of the thin film Al from a frequency of $f_r^0 = 7.56$ GHz expected by design [68], leading to a kinetic inductance fraction of 10%. We will discuss the implications of this large kinetic inductance later in this article. An external drive line is coupled to the qubit by a coupling strength of $\kappa/2\pi = 396$ kHz.

The CPW device design consists of six $\lambda/4$ coplanar waveguide resonators inductively coupled to a common feedline. Each resonator has a varying external coupling quality factor Q_{ext} determined by the spacing of the resonator from the feedline c and expected resonant frequency depending on the length l. Based on the geometry of each resonator, we perform finite-element simulations using Ansys [69]. A summary of the calculated resonant frequency and the external coupling quality factor is detailed in Table I. Each coplanar waveguide has a center trace width of 35 μm and a spacing to ground of 20 μm.

APPENDIX C: MEASUREMENT SETUP

A schematic of the measurement setup is found in Fig. 9. Measurements are conducted in a Triton, a cryogen-free dilution refrigerator from Oxford Instruments. The device chip is placed in a QCage, a microwave sample holder from QDevil, and connected to the printed circuit board by aluminum wirebonds. RF signals are sent from a vector network analyzer or a microwave signal generator and attenuated by -56 dB with attenuation at each plate as noted. The signal then passes through an Eccosorb filter, made from cured castable epoxy resin. The signal is then sent through the sample, returned through another Eccosorb filter, and passed through a Quinstar isolator with 20 dB isolation and 0.2 dB insertion loss. A traveling wave parametric amplifier then amplifies the signal, which is then passed through another isolator, and then amplified with a low-noise amplifier mounted to the 4 K plate and two room-temperature amplifiers (MITEQ) outside the fridge.

Pulsed signals are generated by an arbitrary waveform generator with a 1 GSa/s sampling rate and mixed with a continuous microwave source. Simultaneously, a continuous probe tone set to the readout resonator frequency is used to dispersively measure the qubit state. The outgoing signal is then demodulated, and a homodyne detection voltage V_H is measured by a digitizer with a 500 MSa/s sampling rate.

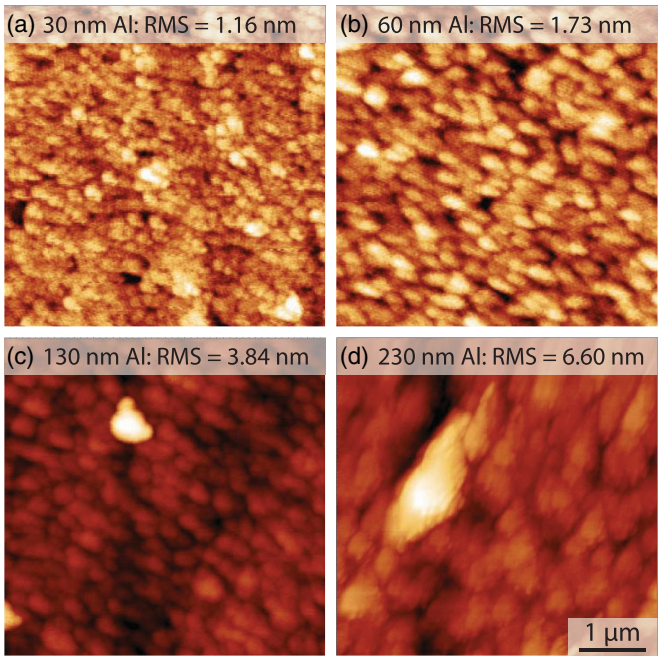

FIG. 10. Atomic force micrographs of four aluminum films varying thicknesses of aluminum: (a) 30 nm, (b) 60 nm, (c) 130 nm, and (d) 230 nm. The root-mean-squared roughness is noted for each.

APPENDIX D: ALUMINUM SURFACE MORPHOLOGY

The aluminum film morphology depends on the thickness of the film, which leads to noticeable changes in transport properties. In Fig. 10 we show atomic force microscopy images of samples with varying thicknesses of aluminum. The images are 5×5 μm. The aluminum grains can clearly be seen. We find that the thinnest sample of 30 nm thickness has the smallest Al grain sizes, and the grain sizes increase as the thickness of the film increases. This is consistent with the rf measurements of resonators on these samples: as the film thickness decreases and the Al grain size decreases, the

mean free path in the superconductor l decreases, increasing the London penetration depth in the dirty limit where the coherence length $\xi_0 \gg l$. This leads to an increase in the kinetic inductance and in turn an increase in inductive loss.

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