

A GaN-Based DC–DC Multistage Hybrid Converter for Step-Up Applications

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Abstract—This paper presents a multistage hybrid converter (MS-HC) designed for step-up applications, utilizing a combination of switched-inductor and switched-capacitor techniques. The proposed converter takes advantage of the controllability offered by switched-inductors and the multiplicity provided by switched-capacitors. To enhance efficiency and reduce size, Gallium Nitride (GaN) switches are employed in the design. The inductor's current frequency is increased to twice the switching frequency, resulting in a smaller inductor size. By incorporating multiple stages, the converter achieves a high step-up voltage gain. Additionally, the converter ensures low voltage stress on switches, limited to one-fourth of the output voltage. A comprehensive analysis is conducted to illustrate the operating principle of the converter. Finally, a practical implementation of a 300W two-stage converter is presented, demonstrating 95.7% efficiency and confirming the effectiveness of the proposed design.

Keywords—multistage hybrid converter, DC-DC converter, step-up Converter, Gallium Nitride (GaN).

I. INTRODUCTION

The DC-DC converters that provide high voltage gain utilized in various applications such as photovoltaic systems, fuel cells, electric vehicles, battery backup systems for uninterruptible power supplies and etc [1][2]. For instance, the output voltage of PV modules varies from 12 to 45 V, which is significantly lower than the common dc link value. The step-up converter can be classified into two categories: isolated and non-isolated converters.

Isolated converters offer a straightforward approach to achieving high voltage gain by adjusting the turns ratio of the high-frequency transformer. Common examples of isolated converters include the full bridge converter, half-bridge converter, and flyback converter [3][4]. However, a notable drawback of isolated converters is the presence of leakage inductance in the transformer, which is directly related to the winding turns. Increased leakage inductance results in high voltage spikes across semiconductor devices [5].

Non-isolated step-up DC-DC converters can be categorized into various conventional converter types, including boost converters, Cuk/SEPIC/Zeta converters, multi-level converters, coupled-inductor converters, switched-capacitor converters, and hybrid converters. The conventional boost converter, in theory, has the potential to achieve a high voltage gain by increasing the

duty cycle of its switch. However, practical limitations arise due to the high voltage stress on components and parasitic elements, which restrict the maximum attainable voltage gain to around 4 or 5 [6]. Additionally, challenges such as low conversion efficiency, reverse-recovery issues, and electromagnetic interference further impact the performance of the converter [7].

Coupled inductor converters have the capability to achieve a significant voltage gain by adjusting the turns ratio of the coupled inductor, eliminating the need for galvanic isolation [8]. However, it should be noted that despite their ability to achieve high voltage gain, coupled inductor converters may encounter voltage spikes across semiconductor devices [9]. In an attempt to mitigate this issue, active or passive clamp circuits have been introduced in previous studies [10]. While these clamp circuits help reduce stress on the semiconductors, they also introduce additional complexity and increase the number of semiconductor components required.

Switched-capacitor converters (SCCs) offer the ability to achieve a significant voltage gain using only switches and capacitors. These converters store energy in capacitors during one half-cycle and release it during the other half-cycle. The primary advantages of this converter type include its simple structure, high voltage gain, high power density, compact size, lightweight design, cost-effectiveness, and compatibility with integrated circuits [11][12]. However, traditional switched-capacitor converters encounter challenges such as a lack of output voltage regulation, low efficiency, current spikes, and electromagnetic interference [1]. To address these issues, resonant switched-capacitor converters have been introduced, operating under zero current switching (ZCS) conditions [13][14]. These converters aim to mitigate the aforementioned drawbacks and enhance performance.

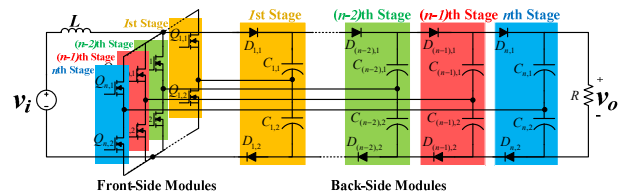


Fig. 1. Proposed multistage hybrid converter (MS-HC).

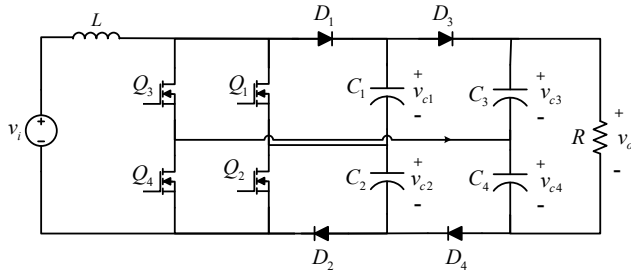


Fig. 2. Proposed MS-HC with two stages.

Multi-level converters are capable of achieving a substantial voltage gain by increasing the number of converter levels. This configuration also leads to a notable reduction in the stress placed on semiconductor devices [15]. While these converters exhibit a wide voltage-gain range in [16][17], it is important to note that they require a larger number of components. This increase in components not only contributes to higher losses but also raises the overall cost of the system.

This paper introduces a proposed multistage hybrid converter (MS-HC) for step-up applications, depicted in Fig. 1. The multistage design significantly enhances the voltage gain of the converter while the voltage stress across the switches is decreased. By combining switched-capacitor and switched-inductor techniques, the converter benefits from the controllability and high gain [18][19]. Furthermore, the switched-capacitor section amplifies the converter's gain, making it well-suited for step-up applications. Additionally, as a non-isolated converter, it eliminates leakage current and minimizes stress on the switches.

The operating principle and analysis of the proposed converter are presented in Section II. In Section III, the voltage stress across the component is described. Finally, the experimental results are discussed in Section IV.

II. PROPOSED CONVERTER AND OPERATION PRINCIPLES

The basic dual-phase dc-dc converter has low voltage gain and increasing voltage with cascading method increase the voltage stress on the switches [20]. In this paper, a multistage hybrid converter (MS-HC) for step-up application has been proposed by applying front-side and back-side modules to the converter, as shown in Fig. 1. By doing so, the stress voltage on the switches will be reduced to one-fourth of the output voltage. The gate signal of the $Q_{(2n-1),1}$ and $Q_{(2n),2}$ has 180° phase-shift to $Q_{(2n-1),2}$ and $Q_{(2n),1}$. Because of the phase-shift on the voltage ripple of the capacitors in each leg, the output voltage ripple is low.

In order to analysis the steady state operation of the converter, the capacitors and inductor are considered large enough that the voltage and current ripple can be ignored, and the converter operates in continuous conduction mode (CCM). According to the duty cycle, the operating modes of the converter changes when duty cycle be under 50 percent. Both operation of the converter in above and below the 50% of the duty cycle is described, respectively. In this paper, a two-stage MS-HC is discussed, as shown in Fig. 2.

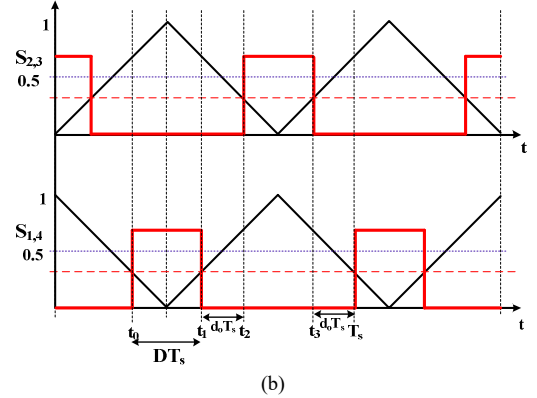
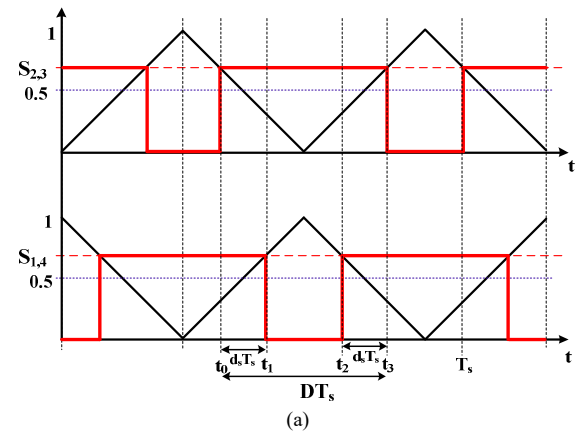


Fig. 3. Switching state (a) $D > 0.5$; (b) $D < 0.5$.

A. Mode operation when D is above 50 percent

The switching waveform of the converter when duty cycle is more than 50 percent is shown in Fig. 3(a). The converter operates in three different modes that are shown in Fig. 4.

Mode I ($t_3 < t < T_s$): The time duration of this mode is $(1-D)T_s$. The equivalent circuit of this mode is shown in Fig. 4(a). In this mode, Q_1 and Q_4 are ON and D_3 and D_2 are forward bias. Thus, capacitors C_3 and C_2 are being charged while C_1 is being discharged.

By applying KVL in this mode, the input and output voltage can be derived as (1)-(3).

$$-V_{in} + V_L - V_{c1} + V_{c3} = 0 \quad (1)$$

$$-V_{in} + V_L + V_{c2} = 0 \quad (2)$$

$$V_{c3} + V_{c4} = V_o \quad (3)$$

Mode II ($t_0 < t < t_1$): The time duration of this mode is $(2D-1)T_s$. The equivalent circuit of this mode is shown in Fig. 4(b). In this mode, all Mosfets are ON, and no diodes conduct. During this mode, the inductor is being charged by input voltage. In each switching period time, this mode repeats twice. As a result, the frequency of the inductor current is as twice as switching

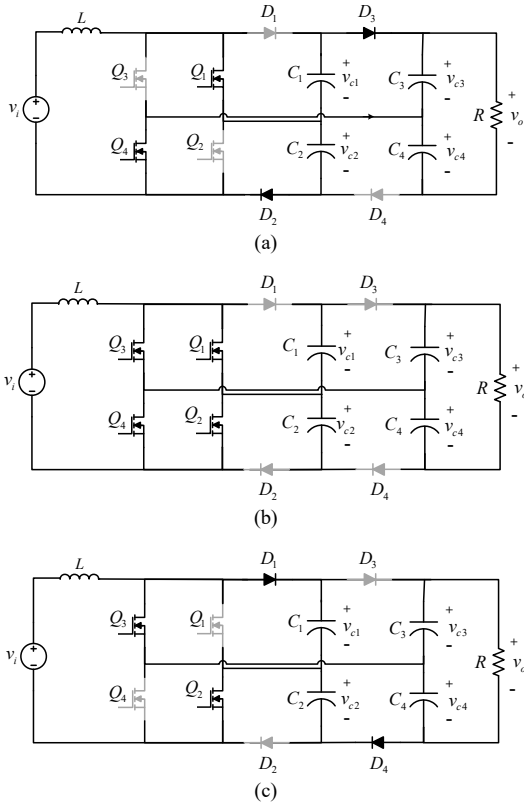


Fig. 4. Mode operation when $D > 0.5$ (a) Mode I; (b) Mode II; (c) Mode III.

frequency. Also, C_1 and C_2 neither being charged nor discharged. By applying KVL in this mode, the input and output voltage can be derived as (4)-(5).

$$-V_{in} + V_L = 0 \quad (4)$$

$$V_{c3} + V_{c4} = V_o \quad (5)$$

Mode III ($t_1 < t < t_2$): The time duration of this mode is time duration $(1-D)T_s$. The equivalent circuit of this mode is shown in Fig. 4(c). In this mode, switches Q_2 and Q_3 are ON and diodes D_1 and D_4 start conducting. In this time interval C_2 is being discharged while C_1 and C_4 are being charged. By applying KVL in this mode, the input and output voltage can be derived as (6)-(8).

$$-V_{in} + V_L + V_{c4} - V_{c2} = 0 \quad (6)$$

$$-V_{in} + V_L + V_{c1} = 0 \quad (7)$$

$$V_{c3} + V_{c4} = V_o \quad (8)$$

From (1)-(8) and due to the symmetric behavior of the converter the voltage of capacitors can be written as:

$$V_{c1} = V_{c2} = \frac{V_o}{4} \quad (9)$$

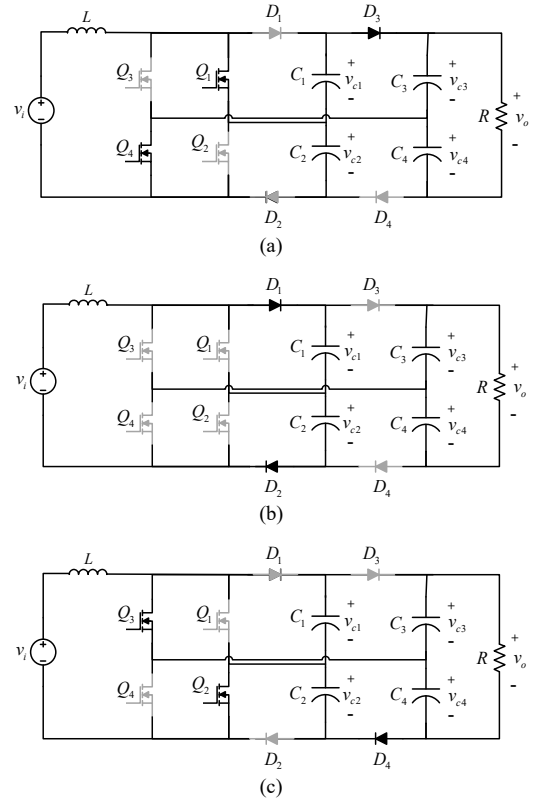


Fig. 5. Mode operation when $D < 0.5$ (a) Mode I; (b) Mode II; (c) Mode III.

$$V_{c3} = V_{c4} = \frac{V_o}{2} \quad (10)$$

The output voltage is driven by applying Volt-second balance on inductor:

$$\langle V_L \rangle = (V_{in})d_s T_s + (V_{in} - V_{c1})\left(\frac{T_s - 2d_s T_s}{2}\right) + (V_{in})d_s T_s + (V_{in} - V_{c2})\left(\frac{T_s - 2d_s T_s}{2}\right) = 0 \quad (11)$$

$$\frac{V_o}{V_{in}} = \frac{4}{(1-2d_s)} \quad (12)$$

Where,

$$d_s = \frac{2D-1}{2} \quad (13)$$

Thus, the gain of the converter is equal to:

$$\frac{V_o}{V_{in}} = \frac{2}{1-D} \quad (14)$$

B. Mode operation for D below 50 percent

The switching waveform of the converter when duty cycle is less than 50 percent is shown in Fig. 3(b). The converter operates in three different modes that are shown in Fig. 5.

Mode I ($t_0 < t < t_1$): The time duration of this mode is DT_s . The equivalent circuit of this mode is shown in Fig. 5(a). In this mode, Q_1 , Q_4 and D_3 are ON and C_1 is being discharged by inductor current. By applying KVL and KCL (15)-(19) are derived.

$$-V_{in} + V_L - V_{c1} + V_{c3} = 0 \quad (15)$$

$$V_{D2} = V_{c3} - V_{c1} - V_{c2} \quad (16)$$

$$V_{c3} + V_{c4} = V_o \quad (17)$$

$$\Delta V_{c1} = \frac{i_{c1}}{c} \Delta t = \frac{-i_L}{c} DT_s \quad (18)$$

$$|\Delta V_{c1}^{discharging}| = \frac{i_L}{cf_s} DT_s \quad (19)$$

Mode II ($t_1 < t < t_2$): The time duration of this mode is $(1-2D)T_s$. The equivalent circuit of this mode is shown in Fig. 5(b). In this mode, all Mosfets are OFF, and just D_1 and D_2 flow the current through themselves. Now, C_1 and C_2 are being charged by inductor's current via D_1 and D_2 .

$$-V_{in} + V_L + V_{c1} + V_{c2} = 0 \quad (20)$$

$$V_{D3} + V_{D4} = V_{c1} + V_{c2} - V_{c3} - V_{c4} \quad (21)$$

$$V_{c3} + V_{c4} = V_o \quad (22)$$

$$\Delta V_{c1}^{charging} = \Delta V_{c2}^{charging} = \frac{i_L}{cf_s} (1 - 2D)T_s \quad (23)$$

Mode III ($t_2 < t < t_3$): The time duration of this mode is DT_s . The equivalent circuit of this mode is shown in Fig. 5(c). In this mode, Q_3 , Q_2 and D_4 are ON and C_2 is being discharged by inductor current.

$$-V_{in} + V_L + V_{c4} - V_{c2} = 0 \quad (24)$$

$$V_{D1} = V_{c4} - V_{c1} - V_{c2} \quad (25)$$

$$V_{c3} + V_{c4} = V_o \quad (26)$$

$$|\Delta V_{c2}^{discharging}| = \frac{i_L}{cf_s} DT_s \quad (27)$$

By applying Volt-second balance on inductor:

$$V_{in} + (V_{c1} + V_{c2})(3D - 1) - D(V_{c3} + V_{c4}) = 0 \quad (28)$$

If the converter operates in steady state mode, then the charge and discharge voltage of capacitors (like C_1) should be equal. In mode I, C_1 is discharged by inductor's current ($|\Delta V_{c1}^{discharging}| = \frac{i_L}{cf_s} DT_s$). In mode III, it is neither being

charged nor discharged, and in modes II, it is charged by inductor's current ($\Delta V_{c1}^{charging} = \Delta V_{c2}^{charging} = \frac{i_L}{cf_s} (1 - 2D)T_s$). Thus, the below equations could be written for steady state condition:

$$\begin{cases} |\Delta V_{c1}^{discharging}| = |\Delta V_{c1}^{charging}| \\ \frac{i_L}{cf_s} DT_s = \frac{i_L}{cf_s} (1 - 2D)T_s \end{cases} \rightarrow D = \frac{1}{3} \quad (29)$$

It means for $D < 0.5$ the converter operates in steady state only when the duty cycle is exactly 1/3. Now Consider $1/3 < D < 0.5$; In this case, the charging voltage of C_1 , and similarly for C_2 , is less than the discharging voltage (based on (19), (23) and (26)) which means the voltage across C_1 and C_2 decrease gradually. This will continue until $V_{c4} = V_{c1} + V_{c2}$ which means at this moment D_1 in mode III starts conducting (The similar description can be used for D_2 in mode I and then having equation $V_{c3} = V_{c1} + V_{c2}$). According to this description, the relation between capacitors and output voltage can be written as:

$$V_{c4} = V_{c3} = V_{c1} + V_{c2} = \frac{V_o}{2} \quad (30)$$

It should be mentioned that by conducting D_1 and D_2 in modes I and III, volt-second balance of inductor (28) will not be changed. By considering (30), the output voltage can be derived as (31), which is similar to $D > 0.5$.

$$\frac{V_o}{V_{in}} = \frac{2}{1 - D} \quad (31)$$

Now, consider $D < 0.3$. In this case the charging voltage of C_1 , and similarly for C_2 , increases gradually until the sum of C_1 and C_2 voltages reaches the sum of C_3 and C_4 voltages (V_o) and the diodes D_3 and D_4 starts conducting. Although nothing changes in volt-second balance equation, we can add and use the following equation:

$$V_{c1} + V_{c2} = V_{c3} + V_{c4} = V_o \quad (32)$$

The output voltage is driven by mixing (28) and (32):

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - 2D} \quad (33)$$

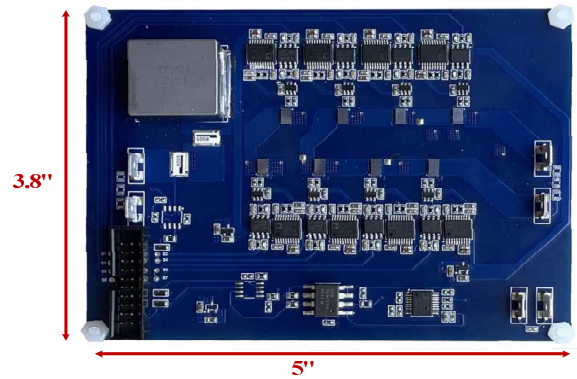


Fig. 6. Experimental prototype.

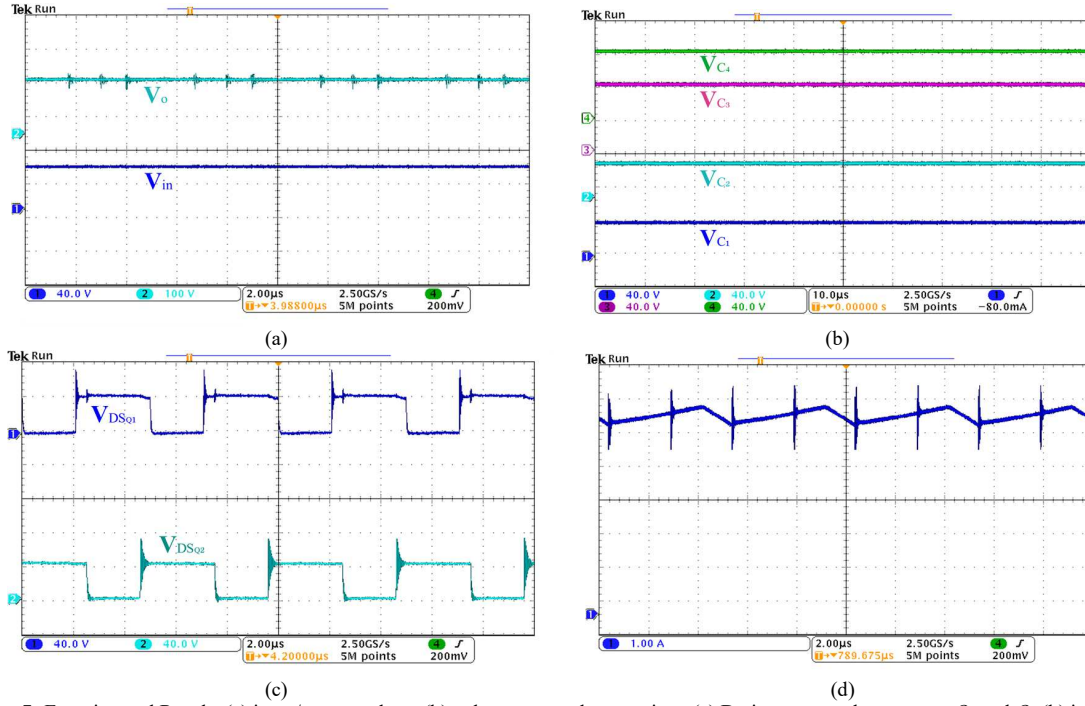


Fig. 7. Experimental Results (a) input/output voltage (b) voltage across the capacitors (c) Drain-source voltage across Q_1 and Q_2 (d) inductor current.

III. VOLTAGE STRESS OF THE DEVICES

In order to calculate the voltage stress on semiconductors, consider the duty cycle is more than 50 percent. According to circuit analysis and Fig. 4, it is evident that the voltage across D_1 and D_2 when they are OFF equals the voltage across C_1 and C_2 , which is one-fourth of output voltage. For D_3 and D_4 in modes I and III when they are OFF, they face the half voltage of output but in modes II when both of them are OFF, the sum of the voltage across them equals $V_o/2$. Also, because of the symmetry feature of the circuit, each of them should tolerate one-fourth of output voltage. By analyzing the equivalent circuit of the converter, the voltage across all of Mosfets equals $V_o/4$. The inductor current frequency is as twice the switching frequency, which means the size of the inductor will reduced twice in compare to the conventional boost converter.

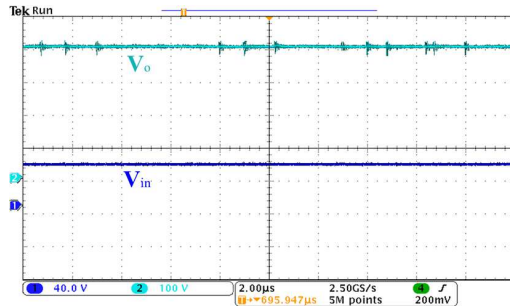


Fig. 8. input/output voltage with $D=0.75$.

IV. EXPERIMENTAL RESULTS

A 300W two-stage experimental prototyped has been built to verify the operation of the proposed converter. The converter is designed based on GaN switches to reduce the size of the converter as shown in Fig. 6. Because of the low raising and falling time of the GaN, the switching losses will be

low. Thus, the switching frequency of the system is increased to 100kHz. By increasing the switching frequency, the size of the passive components is reduced, and the power density is increased. The EPC 2034C GaN FETs have been used as the power switches, and they were driven by Texas instrument gate driver, LM5114. The capacitors that transfer energy storage in the converter are TDK, multilayer ceramic capacitors with high energy density, and the size of these capacitors are 30 μ F. The operation of the converter when input voltage is 50V and output voltage is 160V is investigated to verify the theoretical analysis as shown in Fig. 7. Two gate signals with 40% duty cycle are applied to the Q_1 , Q_4 , Q_5 , Q_7 and Q_2 , Q_3 , Q_6 , Q_8 . Also, there is a phase-shift 180° between the Q_1 , Q_4 , Q_5 , Q_7 and Q_2 , Q_3 , Q_6 , Q_8 . There is a capacitor leg in each stage (C_1 , C_2 and C_3 , C_4), and the voltage across the capacitors of each stage is the same. Also, this voltage is half of the voltage of the next stage as shown in Fig. 7 (b). According to the Fig. 7 (c) and theoretical analysis, the stress voltage across the power switches in two-stage converter is one-fourth of the output voltage. This feature is crucial for designing the converter with GaN switches since low-voltage GaNs have low price and conduction resistance, R_{on} . In this converter PA4349.473ANLT inductor, 90 μ H, is used series with input sources, and the frequency of the inductor current is twice of the switching frequency as shown in Fig. 7 (d). To evaluate the wide output voltage capability of the proposed

converter, the duty cycle of the converter is increased to 0.75 to change the output voltage from 160 to 400 as shown in Fig. 8. The YOKOGAWA PZ4000 power analyzer is used to measure the efficiency of the converter, and the maximum efficiency of the converter in 300W is obtained 95.7%.

V. CONCLUSION

A GaN based two-stage hybrid dc-dc converter is proposed in this paper. The proposed converter can be used as a multistage converter by adding front-side and back-side module to the converter. Because of the increasing frequency based on the GaN operation, and double frequency of the inductor current, the size of the passive components is reduced. The high power-density with wide voltage range operation makes the converter appropriate for different applications. Moreover, the low voltage stress on the power switches give advantage to the converter to be used for high voltage applications.

ACKNOWLEDGMENT

This work is partially supported by NSF grant: NSF ECCS-2103442.

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