

Scalable GaN-Based EV Charging Station with Energy Storage

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Abstract—Electric Vehicle (EV) charging stations with integrated energy storage are gaining increased attention because they reduce the negative impact of EV penetration on the electric grid. This work leverages the attractive flying capacitor multilevel (FCML) topology as a building unit referred to in this paper as a cell to develop a scalable DC-DC stage of an EV charging station that integrates energy storage (ES). It is scalable because it is constructed of points that interface EVs and ESs that can be increased for future upgrades. These points have two interfaces: one interface of each point is linked to the DC-link and the other interfaces are linked to respective EV or ES interfaces. Each point may contain a single cell (FCML) or several parallel cells to scale up the power rating of a point. This architecture has been verified by building a prototype using Gallium Nitride (GaN) switches consisting of a 2 kW single cell point for EV charging and a 2 kW single cell point for ES integration. Experimental results are provided in this paper, which shows the promising potential of this architecture thanks to the FCML coupled with the GaN switches.

Keywords—Electric vehicle, EV, scalable charging stations, energy storage, gallium nitride, GaN, flying capacitor multilevel, FCML

I. INTRODUCTION

The growing concerns about climate change that has already affected the environment negatively in many ways call for immediate actions to keep global warming below the limit set out in the Paris agreement of 1.5 degrees Celsius above the pre-industrial level [1]. The transportation sector is considered one of the main sources of greenhouse gas emissions that cause global warming. Therefore, the electrification of this sector and making it environmentally friendly should be prioritized.

The existing internal combustion engine vehicles accounted for about 27 % of Greenhouse gas emissions in the US in 2020, the largest among all other sources of Greenhouse gas emissions in the US [2]. Therefore, the transportation sector should be electrified because it has the highest possible chances of success among other global warming solutions to fight global warming and reverse its already existing negative climate changes.

Consequently, the Electric Vehicle (EV) worldwide rate from car sales is projected to increase significantly by 2040 to reach more than 50% as a result of their promising potential to slow down global warming [3]. As a result, the research in the field of EV applications is dramatically increasing [4]–[6].

Moreover, there is an increasing demand for charging infrastructure for EVs, which needs a considerable amount of energy that has negative impacts on the electric grid, such as transformer overloading and distribution lines congestion [7]. One way to alleviate these negative impacts is to integrate local energy storage (ES) with the charging stations that can be charged at low grid load demand. These ES charge the EVs at the time of high EV load demand or grid peak load. Moreover, this local storage can provide ancillary services to the grid when no EVs are charging [8], [9].

Isolation in the DC-DC stage of the off-board EV chargers is required; however, a non-isolated DC-DC stage can be employed if isolation is provided in the front-end AC-DC rectifier stage. Therefore, the DC-DC stages of the off-board EV chargers can be isolated or non-isolated. This paper proposes a non-isolated DC-DC stage of an off-board charging station. Recent work in [5] reviews the DC-DC power stages of EV charging infrastructure for the off-board dc fast charger; it can be seen that the proposed DC-DC stage in this paper has a promising potential compared to the existing solutions.

This work proposes employing the flying capacitor multilevel (FCML) topology as a cell to construct a modular and scalable DC-DC stage of off-board charging stations that integrate ES locally. The FCML topology is chosen to derive our proposed scalable DC-DC stage for its high figures of merit, such as achieving high efficiency and power density [10]–[12]. The proposed DC-DC stage's modularity and scalability facilitate upgrading the EV charging stations for any future EV increase smoothly by adding more points for interfacing EV and ES as needed. Moreover, the power range can be increased for any future upgrade by adding more cells in parallel within each point. The proposed charging station architecture is explained in section II. Then, the design and operation principles are provided in section III. The experimental hardware prototype is presented in section IV. Section V demonstrates the experimental results, and the conclusion is drawn in section VI.

II. THE PROPOSED CHARGING STATION ARCHITECTURE

As seen in the generalized charging station block diagram in Fig. 1, the front-end AC-DC converter is out of the scope of this work. However, the proposed non-isolated DC-DC stage of the charging architecture can be linked to the DC-link with any isolated front-end AC-DC converter.

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The proposed scalable DC-DC stage architecture

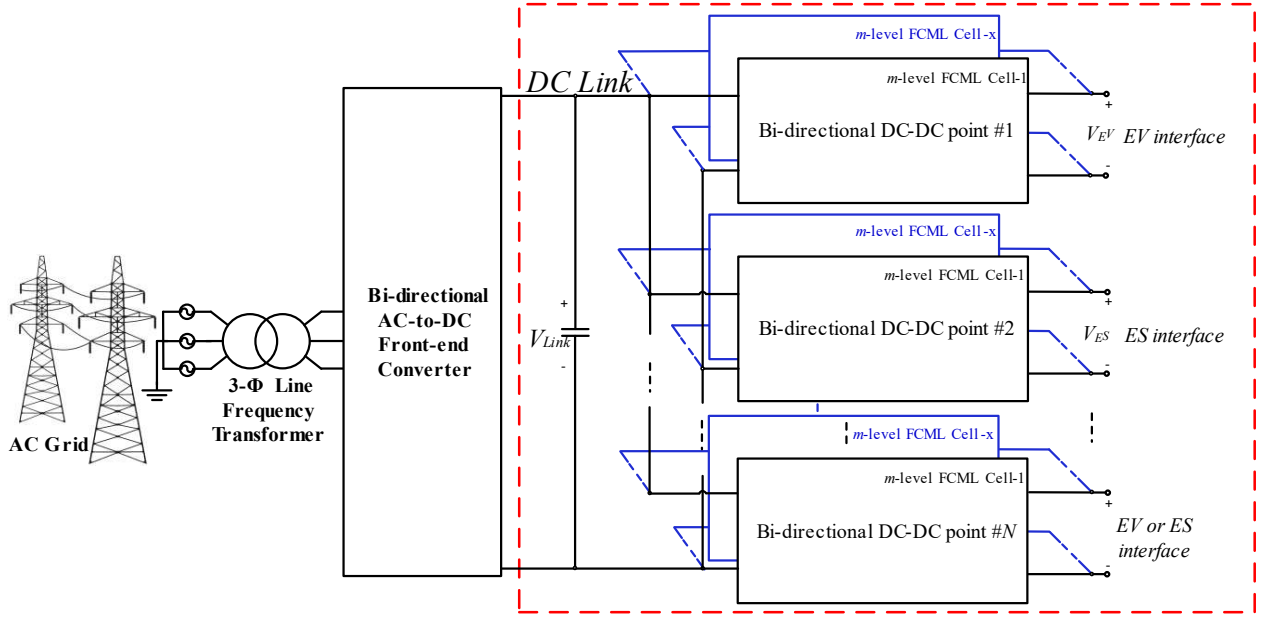


Fig. 1. Generalized block diagram of the proposed charging station architecture.

The main building block is the FCML, referred to in this paper as a cell. Each cell is a FCML that can be designed to have any number of levels, m , depending on the DC-link voltage (V_{Link}) and the charging station specifications. This charging station can have any number of points, N , for EV and ES interfaces. Each point has two interfaces: one interface of each point is connected to the DC-Link and the other interfaces of each point are connected to the respective EV or ES. A careful design allows more points to be added easily to accommodate new EV or ES interfaces for future upgrades. Moreover, each point can be designed to have a single cell or any number of cells, x , connected in parallel to scale up the power rating for a specific point for future upgrades.

To verify the proposed non-isolated DC-DC stage of the charging architecture, a charging station containing two points, one point for EV interface and one point for ES interface, is designed using a four-level FCML topology as a cell, and its schematic is shown in Fig. 2.

III. DESIGN AND OPERATION PRINCIPLE

As can be seen in Fig. 2, the charging station contains two points, each with a single four-level FCML cell. Each cell contains $2(m-1)$ switches; that is, six switches when the number of levels m equals four. Three top switches TS_{11} , TS_{12} , TS_{13} , and three bottom switches BS_{11} , BS_{12} , BS_{13} for point#1 cell-1. Three top switches TS_{21} , TS_{22} , TS_{23} , and three bottom switches BS_{21} , BS_{22} , BS_{23} for point#2 cell-1. Gallium Nitride (GaN) switches are used for all these twelve switches for their low losses and small size compared to MOSFET switches, and in this design, they switch at a switching frequency (f_s) that is equal to 120 kHz and block only a fraction of the DC Link voltage of $V_{Link} / (m-1)$ or 141 V for this design because $V_{Link} = 425$ V.

The switches of each cell are controlled using the Phase Shifted

Pulse Width Modulation (PSPWM) [13], [14], whose scheme is simulated in Fig. 3 for point #1 cell-1. There are $(m-1)$ or three triangular carriers (V_{t11} , V_{t12} , and V_{t13}) which are shifted from each other $360^\circ / (m-1)$ or 120° and compared with a dc reference (V_{ref}) to generate the PSPWM signals of the three top switches that are shifted 120° from each other and have fixed duty cycle D . The other three bottom switches are working in a complementary way to the top ones with a duty cycle of $(1-D)$.

The switching voltage V_{sw1} which is before the inductor L_1 , annotated in Fig. 2 and shown in Fig. 4, has a frequency that is $(m-1)$ times more than the switching frequency of each switch because of the frequency multiplication feature of the FCML topology. The gain of each cell can be found by applying the volt-second balance concept using the inductor voltage waveform (V_{L1}) across the inductor L_1 shown in Fig. 4 over an entire period that is equal to the phase shift between the PWM signals of the switches or $T_s / (m-1)$ as implemented in (1). It is clear from Fig. 4 that the inductor voltage V_{L1} is equal to $(V_{Link} / (m-1)) - V_{EV}$ for DT_s of the inductor's voltage waveform periodic time, and V_{L1} is equal to $-V_{EV}$ for $(T_s / (m-1)) - (DT_s)$ of its voltage waveform periodic time.

$$\left(\frac{V_{Link}}{m-1} - V_{EV} \right) (D \cdot T_s) + (-V_{EV}) \left(\frac{T_s}{m-1} - (D \cdot T_s) \right) = 0 \quad (1)$$

Simplifying (1) gives the gain of each cell as

$$V_{EV} = D V_{Link} \quad (2)$$

Each point contains $(m-2)$ or two flying capacitors: C_{f11} and C_{f12} for point#1 cell-1, and C_{f21} and C_{f22} for point#2 cell-1. The voltages across the flying capacitors are passively balanced at their desired values by controlling the switches using the PSPWM [13], [14]. The desired voltages across the flying

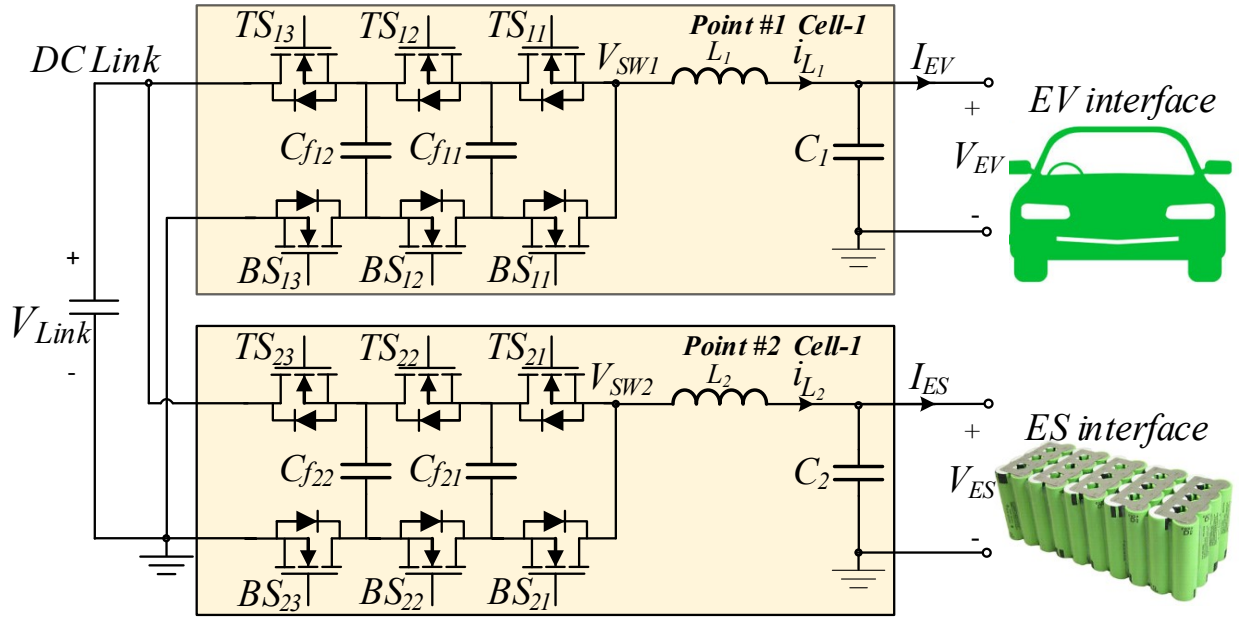


Fig. 2. The schematic of the proposed non-isolated DC-DC stage of the charging station contains two points, each with a single 4-level FCML cell.

capacitors V_{Cfyn} are found as

$$V_{Cfyn} = \frac{n}{m-1} V_{Link} \quad (3)$$

where y is the point number which is 1 or 2 in this design and n is the flying capacitor number which is 1 or 2, which are found to be $V_{Cf11} = V_{Cf21} = \frac{V_{Link}}{m-1} = 141\text{V}$, and $V_{Cf12} = V_{Cf22} = \frac{2V_{Link}}{m-1} = 283\text{V}$.

The maximum filtering inductance value required to keep the inductor current ripple (Δi_L) within its limit that is specified by the design is calculated for each point as [11]

$$L = \frac{0.25 \cdot V_{Link}}{(m-1)^2 \cdot \Delta i_L \cdot f_s} \quad (4)$$

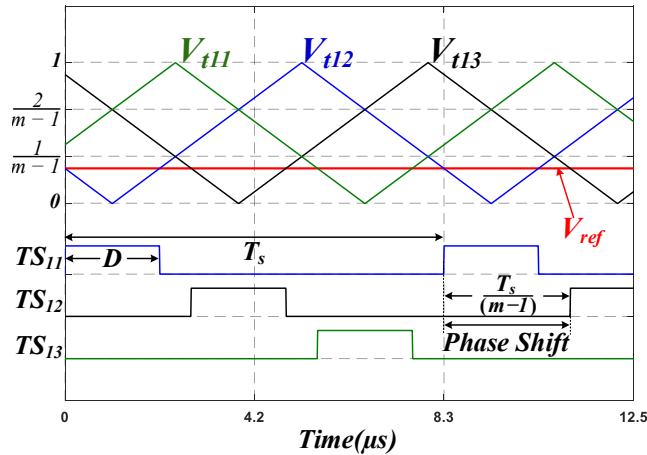


Fig. 3. The PSPWM Scheme of the four-level FCML cell for $D = 0.25$, the triangular carriers and the dc reference V_{ref} (top), and the generated PSPWM signals of the top switches (bottom).

It is clear from (4) that as the number of levels m increases, the filtering inductance value decreases accordingly by a factor of $(m-1)^2$. This inductance reduction resulted from the frequency multiplication effect seen by the inductor and the voltage swing reduction across the inductor, which are two very beneficial features of the FCML topology[11], [15].

The flying capacitors in each cell are the main power transfer elements, and their value can be determined as

$$C_f = \frac{I_{load}}{\Delta V_{Cf} f_s (m-1)} \quad (5)$$

where ΔV_{Cf} is the flying capacitor voltage ripple and I_{load} is the DC current for the EV or the ES interfaces [11], [16].

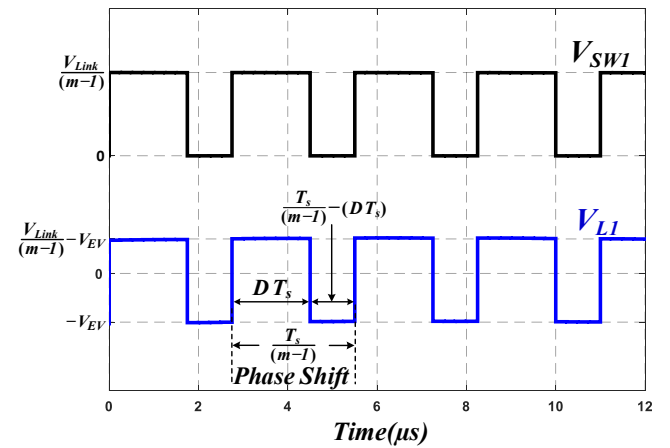


Fig. 4. The switching voltage V_{SW1} (top) and the voltage across the inductor L_1 , V_{L1} .

The switching voltages V_{SW1} and V_{SW2} (annotated in Fig. 2) are pulsed width modulated waveforms that are switching at 360 kHz, which is seen by the inductors L_1 and L_2 . These switching node voltages are filtered by the LC filters of each point to produce a clean DC voltage at the EV and ES interfaces.

IV. EXPERIMENTAL HARDWARE PROTOTYPE

An annotated photo of the hardware prototype is shown in Fig. 5. It is designed to process a maximum power of 4 kW through two bi-directional points. Each point is constructed of a single 2 kW four-level FCML cell. The printed circuit board contains four layers and is designed carefully to achieve a compact size.

The switches used in this prototype are EPC2034C GaN switches. A high switching frequency of 120 kHz is used, resulting in 360 kHz seen by the inductors. Small decoupling capacitors are placed close enough to the complementary switches in parallel with the flying capacitors to minimize the ringing during the switches' transition between ON and OFF states. The GaN gate drivers that have been used are LM5114 low-side gate drivers. Isolated DC-DC converters, ADUM5210, have been used to supply the required floating source to each gate driver and SI8423BB-D-IS is used as digital isolators for each switch PSPWM signal [11], [16].

The two inherent properties of the frequency multiplication and the reduced voltage across the inductor in the FCML cell enabled the use of 33 μ H off-the-shelf composite inductors. Multilayer ceramic capacitors are used for the flying capacitors for their high energy density [17], [18] and are located on the bottom side of the PCB. The capacitor voltages are stabilized at the desired voltage values passively using PSPWM modulation [13], [14], [16]. All switches' PSPWM signals are generated using TI C2000 Microcontroller, TMS320F28379D LaunchPad.

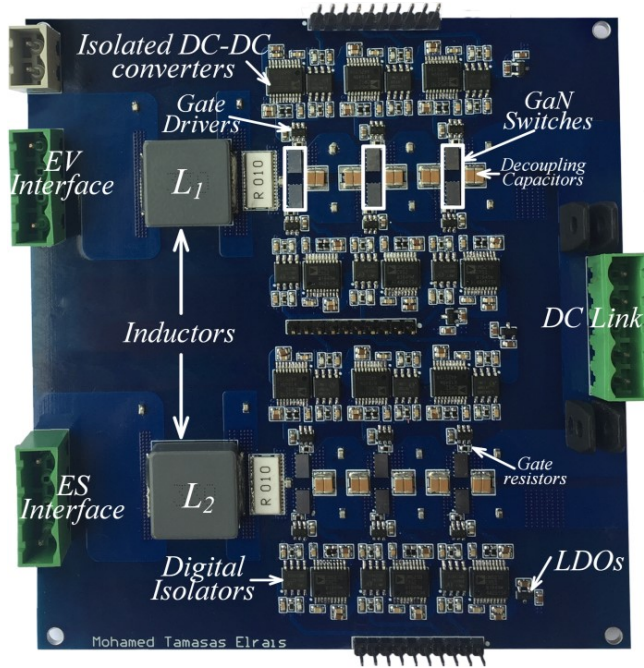


Fig. 5. Annotated photo of the experimental hardware prototype.

V. EXPERIMENTAL RESULTS

The DC-link voltage of 425 V and the energy storage voltage of 100 V are shown in Fig. 6 during step-up operation. In other words, during energy storage discharging, as indicated by the negative polarity of the inductor current. The switching voltage V_{SW2} is also shown in Fig. 6 and has a frequency of 360 kHz with equal pulse heights of 141 V, indicating a well-balanced voltage across the flying capacitors of point#2 cell-1.

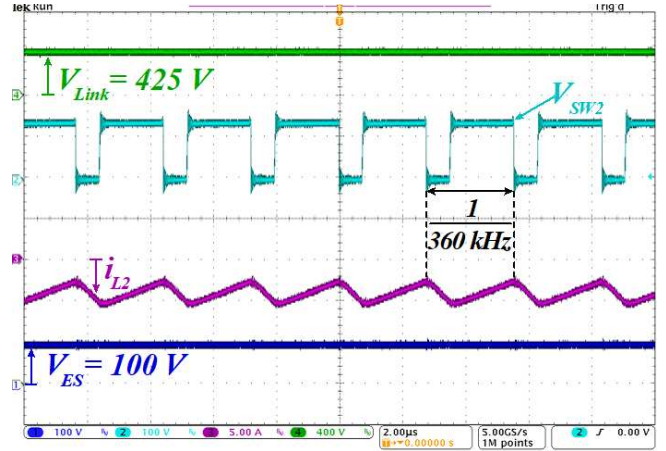


Fig. 6. The DC-Link voltage V_{Link} , the energy storage voltage V_{ES} , the inductor current i_{L2} , and the switching voltage V_{SW2} of point#2 cell-1 during step-up operation, discharging the ES.

The dynamic response is verified during the EV interface charging through point#1 cell-1 by stepping up the current from 2 A to 5 A, as shown in Fig. 7. During this EV interface load step-up, the two flying capacitor voltages V_{cf11} and V_{cf12} are stable and balanced at their 141 V and 283 V values, respectively.

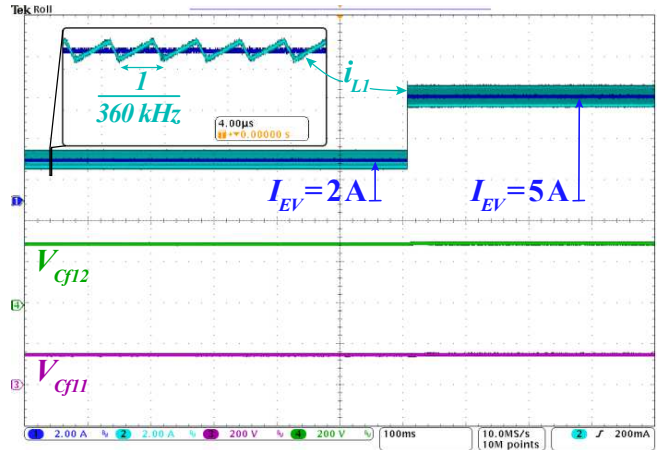


Fig. 7. The EV charging current I_{EV} , the inductor current i_{L1} , and the flying capacitor voltages V_{cf11} and V_{cf12} of point#1 cell-1 during the EV interface charging.

A photo of the YOKOGAWA PZ4000 power analyzer screen is shown in Fig. 8, which shows the readings of the EV interface's voltage, current, and power; the power received from the DC-Link; and point #1 cell-1 peak efficiency of 99.23 % which occurred at 1.489 kW when operating in the step

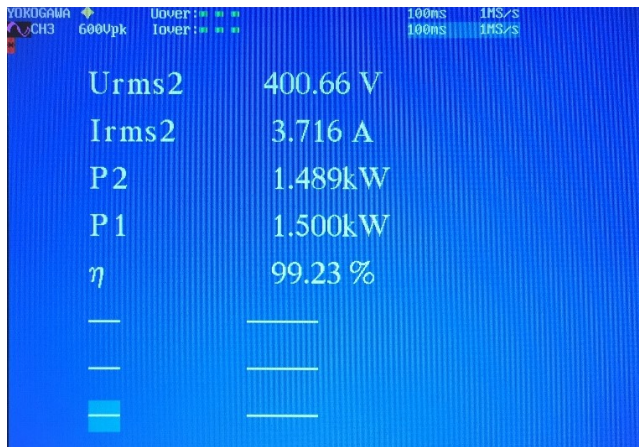


Fig. 8. Udc2, Idc2, and P2 are the EV interface voltage, current, and power; P1 is the power received from the DC-Link; η is the efficiency of point #1 from the DC-Link to the EV interface.

down mode of 425 V at the DC-Link to 400 V at the EV interface.

The hardware prototype dimensions are 12.2 cm $\times$ 10.5 cm $\times$ 1.27 cm, resulting in a box volume of 162.7 cm³. Therefore, with 4000 W for the two points, the power density is 24.59 W/cm³, excluding the heatsink and the Microcontroller.

VI. CONCLUSIONS

A scalable and modular bidirectional DC-DC stage of a charging station is developed in this paper by employing the flying capacitor multilevel topology as a building block or cell. This proposed structure can be designed to contain any number of points for EV and ES interfaces. Each point can have any number of parallel cells for future power upgrades. A 4 kW hardware prototype using GaN switches has been developed and built to verify the functionality of the proposed charging architecture; it is constructed of two 2 kW single cell points for EV and ES interfaces. The experimental results have been reported, showing the high figures of merit of the developed charging station. It has achieved a high power density of 24.59 W/cm³, saving room for future upgrades. Each point has achieved a peak conversion efficiency of 99.23 %.

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