

Silicon Carbide MOSFETs Aging Testing Platform for EV Chargers Using Power Cycling

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Abstract—As the widespread adoption of electric vehicles (EVs) keeps increasing, EV charger reliability is becoming critical to provide a satisfactory charging experience for EV users. Wide-bandgap semiconductors such as silicon Carbide (SiC) MOSFETs have been widely deployed in EV chargers for high efficiency, high power density, and thermal capabilities. However, the aging of SiC MOSFETs has not been fully studied with available aging data lacking significantly in the literature. This paper addresses the EV charger reliability problem by developing a new aging test platform for SiC MOSFETs that are commonly used in various EV chargers, collecting aging data with analysis to provide a new understanding of SiC MOSFET aging, and providing new insights into online EV charger health monitoring system design and development.

Index Terms—Accelerated lifetime testing, remaining useful lifetime.

I. INTRODUCTION

The reliability of EV chargers plays an important role in the charging experience and the widespread adoption of EVs. Unreliable EV charging equipment affects both owners and customers through unscheduled downtime which causes inconvenience, range anxiety, and loss of revenue. To minimize equipment downtime, health monitoring and reliability analysis will be necessary to bring about remaining useful lifetime (RUL) estimation technology. To achieve EV charging equipment health monitoring, reliability analysis, RUL estimation, and other preventative maintenance enabling technologies, it is essential to understand the aging behavior of power converters, and therefore the semiconductor devices commonly used in those EV charger power converters [1]. In order to perform the reliability analysis and RUL estimation at system level for the power converters consisting of many various components, it is critical to understand the behavior on the component or device level. For EV chargers, SiC MOSFETs are becoming increasingly desired due to properties such as high efficiency, high power density, and high-temperature capabilities [2]–[5]. However, the aging and reliability of SiC MOSFETs, and therefore EV chargers, has not been explored enough to achieve the required understanding.

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In an EV charger, the SiC MOSFETs may undergo frequent high-stress operating cycles from the various charging patterns and use cases. In any case, device wear down is inevitable and can present itself in many ways. One of the main driving sources of semiconductor aging has been found to be thermal cycling, which occurs in power converters with short, fast, high power cycles [6]. The result of thermal cycling on semiconductors is expansion and contraction, which can corrupt the physical integrity of the device, eventually resulting in complete failure of the device. In these power converters in the EV charging equipment, devices are subjected to varying charging power levels and charging patterns, as well as ambient temperature and weather profiles. Due to this, breakdown of EV chargers can be extremely variable and unpredictable.

In [7], it is shown that failure modes in SiC MOSFETs can be identified as chip-level failures, which include the body diode and gate oxide, or they can be identified as package-level failures, which include bond wire, and solder layers. Over time, physical indicators corresponding to each failure mode can have undesired drift. It is common to see the use of monitoring of physical indicators to get an understanding of device health. In the literature, Si devices, including MOSFETs and IGBTs, have been researched in terms of reliability. It is shown that through a combination of data-driven modeling and Physics of Failure (PoF) modeling, RUL technology can be developed [8]–[11]. Accelerated lifetime testing (ALT) is used to obtain the data for a specific physical parameter over the aging cycle of a device [7], [12].

Many approaches to ALT have been developed including thermal shock, thermal cycling, power cycling, high-temperature gate bias, and high-temperature reverse bias [7]. In the established reliability research on Si devices, it was found that the best method of ALT is known as power cycling while monitoring the increase of on-resistance ($R_{DS_{on}}$) [13], [14]. Existing data is given by the NASA Ames Research Center showing the validity of this method [15]. In more recent research, power cycling is starting to be explored as an ALT for SiC MOSFETs [9], [10]. However, there is lack of existing data from these tests, and $R_{DS_{on}}$ is only measured at room temperature to observe the gradual increase, which is insufficient.

To address the lack of available aging data for SiC MOS-

FETs, address the existing technical gaps in understanding better the aging behavior of SiC MOSFETs, and contribute to the development of high-reliability EV charging equipment, this paper presents a SiC MOSFETs aging testing platform using power cycling. The new contributions of this paper include: (1) the development of a new testing platform for power cycling ALTs on SiC MOSFETs with R_{DS_on} consistently measured at each temperature in a synchronous way, and (2) the presented work and data show that R_{DS_on} increases differently at different temperatures, concluding that R_{DS_on} variations at high operating temperatures may need to be monitored to accurately evaluate the health status of the SiC MOSFETs.

The remainder of this paper is organized as follows. The system design and analysis are presented in Section II. Hardware validation and results are provided in Section III, while conclusions are discussed in Section IV.

II. SYSTEM DESIGN AND ANALYSIS

The proposed aging testing platform applies thermal stress for ALT by delivering dc current for intermittent periods. To accomplish this, the system follows the structure shown in Fig. 1, where MATLAB is used to interface with a field-programmable-gate-array (FPGA) controller, which simultaneously controls the state of the MOSFETs, external cooling, and reads sensed values of voltage, current, and temperature. To apply thermal stress through power cycling, this work uses a circuit as shown in Fig. 2, where a current source provides power for the thermal cycling of a SiC MOSFET. The system is designed to be fully autonomous for the duration of the power cycling test. The hardware in this system consists of two SiC MOSFETs, one voltage sensing circuit, one temperature sensor and associated circuit, one current sensing circuit, and two brush-less DC fans.

A. System Operation/Control

The first SiC MOSFET, known as the device under test (DUT), as shown in Fig. 2, is the device to undergo power cycling. This device will undergo thermal stress to the junction

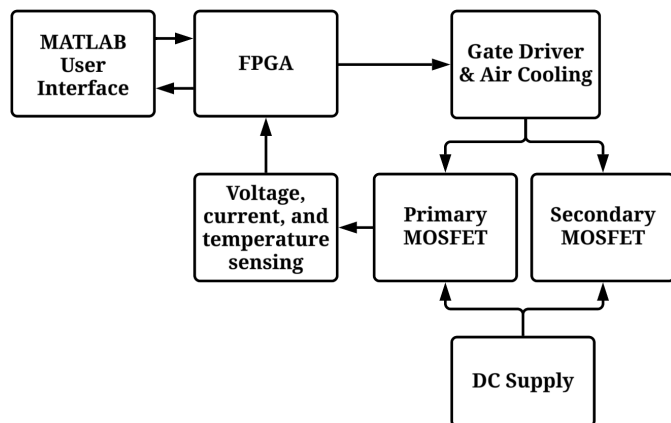


Fig. 1. System Block Diagram

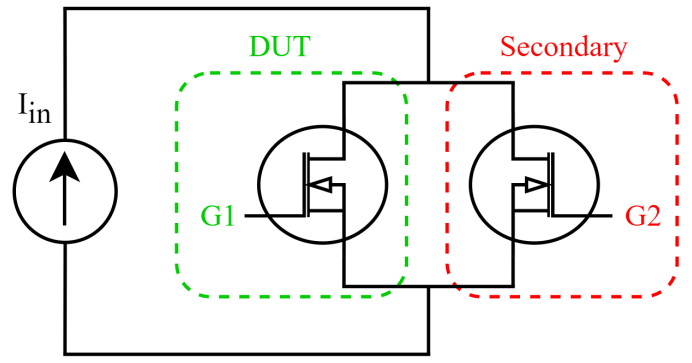


Fig. 2. System Circuit

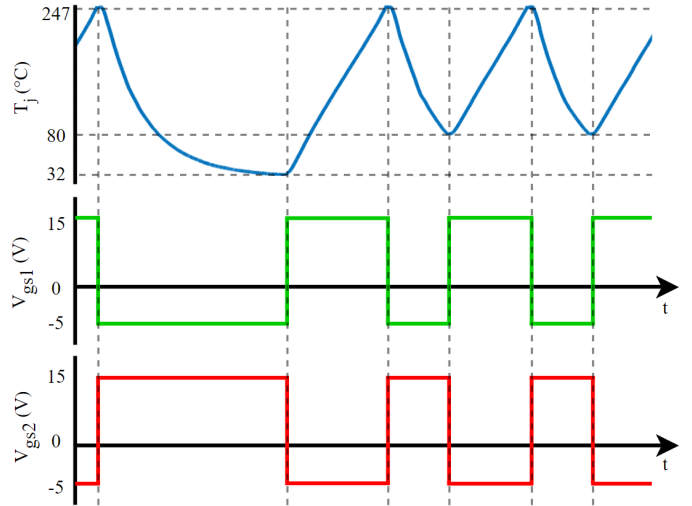


Fig. 3. Thermal cycling pattern

as illustrated in the blue (top) plot of Fig. 3. To increase the junction temperature (T_j), the device is turned on to allow current flow. To cool the device, it is turned off, and external air cooling is applied. If the DUT in the circuit needs to turn off, there still needs to be a path for the current to flow to avoid the need for power supply control. To do this, the system requires the use of a second SiC MOSFET. This secondary device is placed in parallel to the DUT and is to have the opposite state of the DUT. The secondary device is maintained at a lower temperature through heat sink and cooling to avoid breakdown. The switching sequence of the parallel devices is illustrated in Fig. 3 where T_j of the DUT is shown in the blue (top) plot and the gate-to-source voltages (V_{gs}) of each device is shown in green (middle) and red (bottom) for V_{gs1} and V_{gs2} respectively. Since switching is dependent on T_j , the switching frequency varies over time. It is important to note that there exists a small overlap time of the gate signals, as to avoid disruption of the constant current flow from the supply.

B. Sensing and Calibration

To develop the proposed autonomous SiC MOSFET aging testing platform, it is necessary to collect synchronized drain-

to-source voltage (V_{DS}), drain current (I_D), and case temperature (T_c) to obtain an accurate representation of $R_{DS_{on}}$ at all points of a temperature cycle. To find $R_{DS_{on}}$, V_{DS} and I_D are used. Since it is not practical to directly measure T_j , equation (1) is used from the sensed T_c . In (1), $R_{\theta JC}$ is the junction-to-case thermal resistance given by the device datasheet.

$$T_j = V_{DS} * I_D * R_{\theta JC} + T_c. \quad (1)$$

To get accurate $R_{DS_{on}}$ data, it is crucial to get accurate current and voltage data. To achieve this, the voltage and current sensing circuits both utilize the fully differential amplifier (FDA), as shown in Fig. 4 and Fig. 5. The input terminals to the FDA in the voltage sensing circuit are connected in series with resistors to the drain and source of each DUT. The current sensing circuit uses a Hall Effect sensor. In this case, the FDA is used to perform a single-ended to differential signal conversion. The output of each FDA is then connected to a differential analog-to-digital converter (ADC), which converts each voltage to a digital format and sends it to the FPGA system controller. Temperature sensing is performed by using a type-T thermocouple attached to the case of the DUT. The thermocouple leads have an induced voltage depending on the temperature seen at the tip. However, traditional voltage sensing circuits cannot be used because the output is in a micro-volt range. In this work, a cold-junction compensated ADC (MAX31855TASA+) specifically made for type-T thermocouples has been used, to achieve fast and accurate temperature sensing.

To ensure accuracy over all ranges of sensing, rigorous calibration needed to occur. To calibrate the voltage and current sensing circuits, a digital multimeter was used. In current calibration testing, three measurements were taken every 0.5 A up to 20 A then averaged. Once the full range was measured, a linear line of best fit was found and tested in implementation to ensure accuracy. In voltage calibration testing, three measurements were taken every 0.05 V up to 2 V then averaged. Once again, a linear line of best fit was found and tested on the hardware. Though the given resolution from the MAX31855TASA+ is 0.25°C , the ADC values

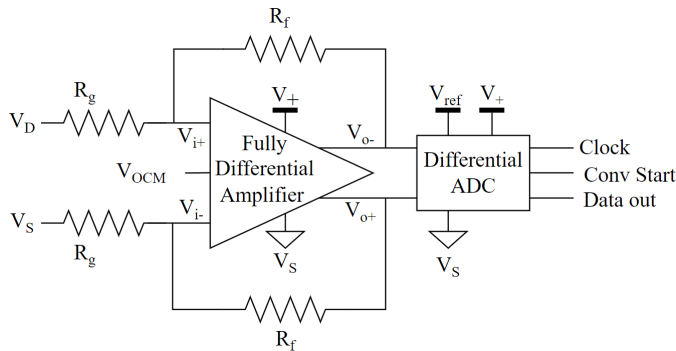


Fig. 4. Drain to source voltage sensing circuit

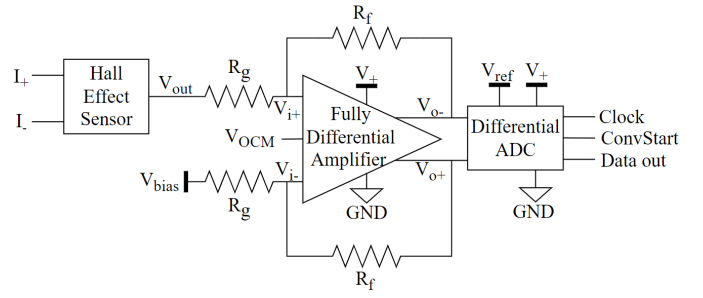


Fig. 5. Drain current sensing circuit

were compared to another type T thermocouple connected to a thermometer, as well as a FLIR T5590 thermal camera to ensure accuracy.

C. Control and Communication

The autonomous system is achieved by a UART interface between the FPGA controller and the PC. The signals transmitted to the FPGA from MATLAB are the SiC MOSFET gate signals and the fan control signals. Control of gate signals is based on the temperature of the DUT as described before. The system controls the fan's on/off state by use of a MOSFET. When the DUT is in the heating portion of the cycle, that gate signal is high and the signals to the secondary device and both fans are low. When the DUT is in the cooling portion of the cycle, that gate signal is low and the signals to the secondary device and both fans are high. The system cycles through these two states until device breakdown occurs, which can present as a short circuit or an open circuit fault.

The SiC MOSFET fault signals and voltage, current, and temperature sensed signals are all sent from the FPGA to MATLAB. Protection is implemented and recorded in a fault register which includes DUT fault, secondary fault, over voltage fault, over current fault, and over temperature fault. If any faults occur, testing is either halted or finished. Once the test has been completed, the system sends a message to indicate DUT failure, then the system automatically shuts down.

III. HARDWARE VALIDATION AND RESULTS

To validate this design, a hardware prototype has been developed and tested. A picture of the developed hardware platform is shown in Fig. 6, and the system setup for collecting SiC MOSFET aging data using the developed hardware platform is presented in Fig. 7.

A. Initial testing

To validate the accuracy of measuring $R_{DS_{on}}$ at different temperatures, initial testing of the platform was performed for a SiC MOSFET that is being used in a megawatt wireless charging system [3]. The SiC MOSFET (NVH4L020N120SC1) has a typical $R_{DS_{on}} = 20 \text{ m}\Omega$, and $I_{D_MAX} = 102 \text{ A}$. To validate V_{DS} and I_D sensing, $R_{DS_{on}}$ on a range from 25°C to 175°C is compared to the given on-resistance variation with temperature plot from the datasheet

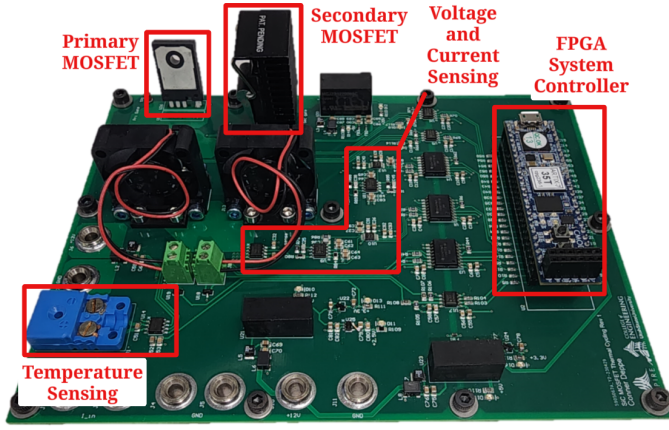


Fig. 6. Hardware picture of the developed SiC MOSFET aging testing platform

under the condition of $V_{GS} = 20\text{ V}$. As shown in Fig. 8, where the blue line was extracted from the datasheet and the red line came from developed platform testing results, the measured on-resistance matches with the datasheet figure nicely, which validates the performance of the developed hardware platform.

B. Power cycling results

Following the conclusion of the initial testing of this system, the power cycling tests were chosen to follow temperature swing characteristics as follows: $T_{j_min} = 80^\circ\text{C}$, $T_{j_max} = 245^\circ\text{C}$, and therefore $\Delta T_j = 165^\circ\text{C}$. As shown in the pattern given by Fig. 3, T_{j_min} is also set to decrease to 32°C every 10 cycles. Cycles between 80°C and 245°C take over 4 minutes at a dc current of 18 A , while cycles that decrease to 32°C take almost 7 minutes.

In each test, data including I_D , V_{DS} , T_j , R_{DS_on} , and cycle count is written to a comma-separated value file. Resulting R_{DS_on} from testing on devices one and two are shown in Fig. 9 and Fig. 10, respectively. The first device took 132 hours or 1562 cycles to fail, and the second took 159 hours or

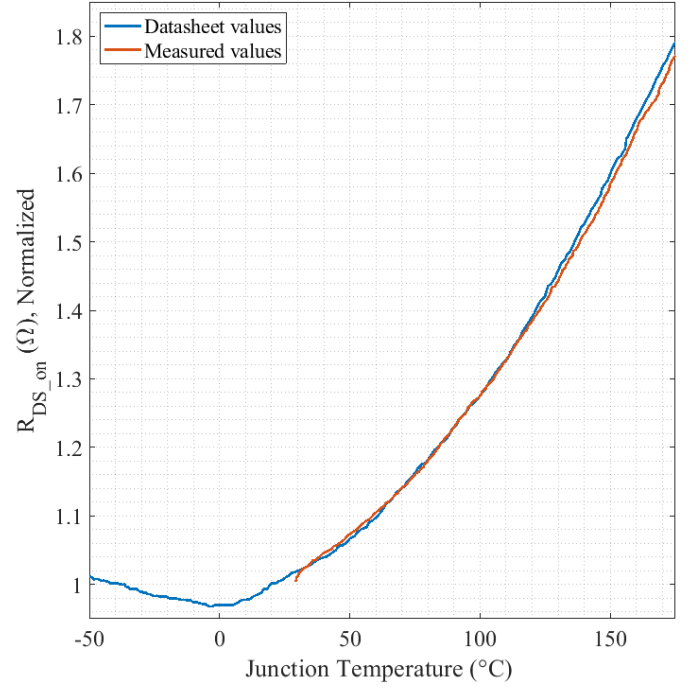


Fig. 8. On-resistance variation

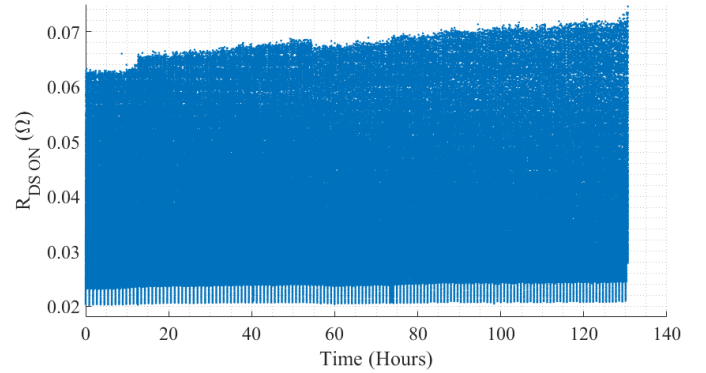


Fig. 9. On resistance data of device 1

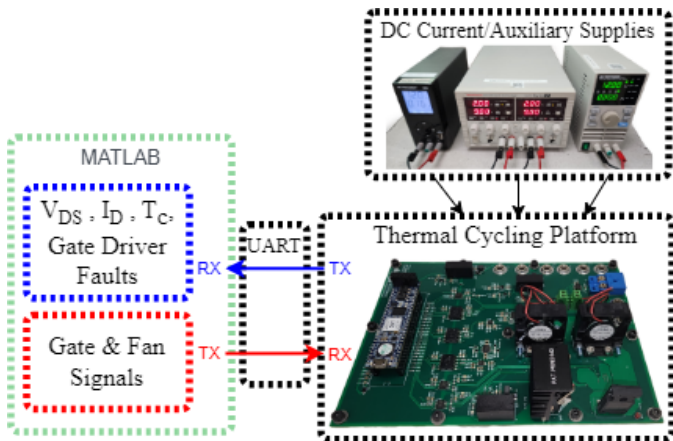


Fig. 7. System diagram for SiC MOSFET aging testing setup using the developed hardware platform

1841 cycles to fail. An average initial R_{DS_on} is found to be $0.0208\ \Omega$ at $T_j = 32^\circ\text{C}$ and $0.0559\ \Omega$ at $T_j = 245^\circ\text{C}$. An average final R_{DS_on} is found to be $0.0215\ \Omega$ at $T_j = 32^\circ\text{C}$ and $0.0656\ \Omega$ at $T_j = 245^\circ\text{C}$.

To better understand the collected aging data, it is critical to analyze the resistance values separately over several temperature ranges. In Fig. 11 and Fig. 12, resistance is plotted over time for 10 different temperatures. From an analysis of the collected data, resistance over each range has a positive, but different slope. It is seen that the increase in resistance at higher temperatures is significantly greater than the increase at lower temperatures. For example, in device 1, the slope for R_{DS_on} in the range between 34 and 35°C is $2.253\ \mu\Omega/\text{hour}$, while the slope in the range between 230 and 231°C is $57.43\ \mu\Omega/\text{hour}$, which is about 25.5 times larger. To compare

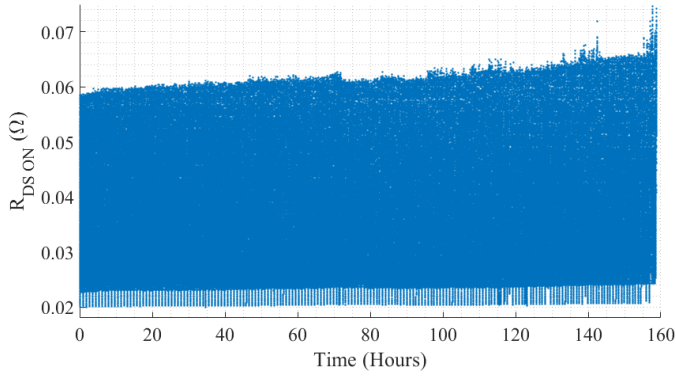


Fig. 10. On resistance data of device 2

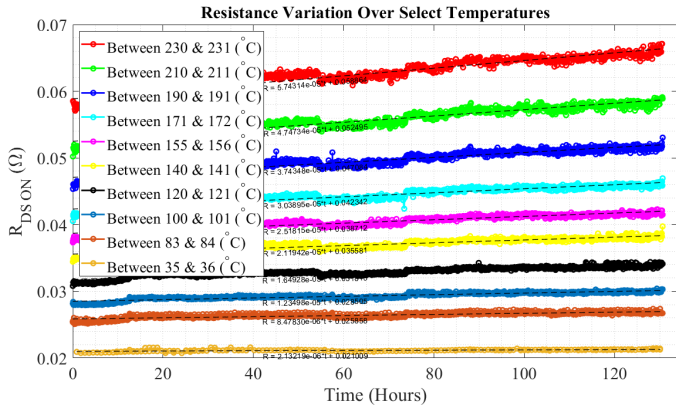


Fig. 11. Resistance variation of device 1

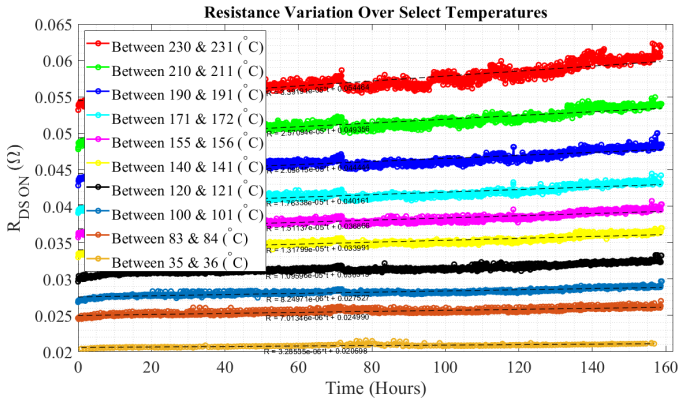


Fig. 12. Resistance variation of device 2

these resulting resistances, Fig. 13 and Fig. 14 show the percent variation of each plot of temperature range.

C. Discussion

Table I has been included as a summary of the results. Though the duration and number of cycles varies widely between the two tests, the change in $R_{DS(on)}$ in each device is very similar. From analysis of the slopes across each temperature range, it is clear that significant increase is seen

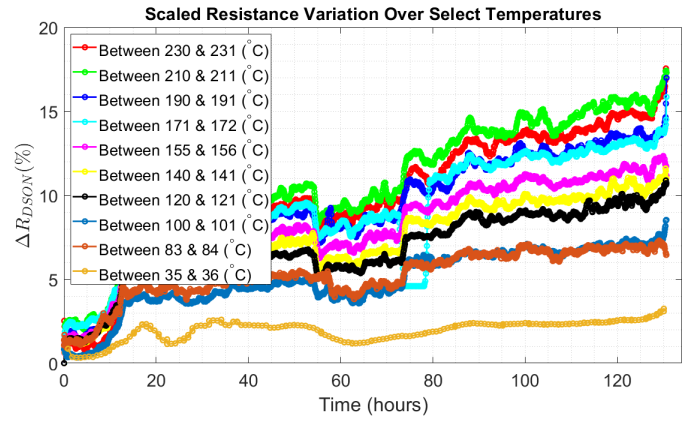


Fig. 13. Relative resistance variation in device 1

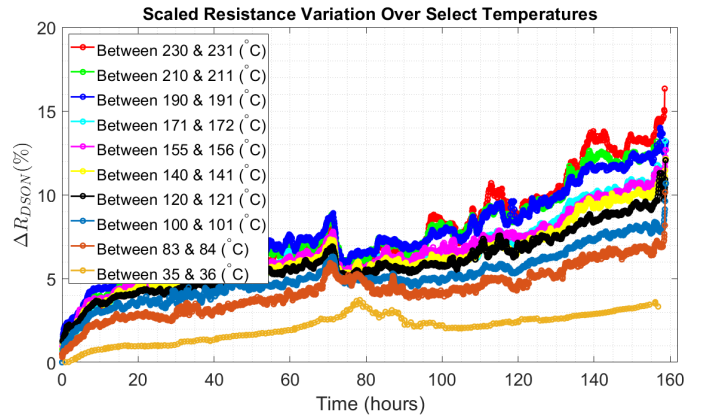


Fig. 14. Relative resistance variation in device 2

in the higher temperature testing conditions. In Fig. 13 and 14, it is shown that there also is a trend in higher $\Delta R_{DS(on)}$ as temperature increases.

Between the two devices, there is significant deviation in terms of test time and slopes. However, the normalized $R_{DS(on)}$ validates the fact that the two tests had similar effects on the physical device, which caused them both to fail in an open circuit around the same percent change from the initial measurements.

The hardware results proved the developed system can successfully run power cycling for accelerated lifetime testing of the SiC MOSFET. The resulting data proves that resistance variation is different over the whole temperature range, and therefore all ranges need to be monitored. More importantly, the $R_{DS(on)}$ data collected at higher temperatures is more meaningful and accurate than at low temperatures in indicating the aging or failure of the SiC MOSFETs. From the collected data shown in Fig. 13, 14, and Table I, it can be seen that a 10%-15% increase in the tested SiC MOSFET's $R_{DS(on)}$ might be used as a threshold to indicate the failure or end-of-life (EOL) of the device for RUL estimation.

TABLE I
DEVICES 1 & 2 RESULTS COMPARISON

Parameter	Units	Test 1	Test 2	Average
Test Time	hours	132	159	145.5
Cycles	-	1562	1841	1701.5
Slope at 35° C	$\mu\Omega/\text{hr}$	2.51	3.29	2.90
Slope at 140° C	$\mu\Omega/\text{hr}$	21.11	13.18	17.15
Slope at 230° C	$\mu\Omega/\text{hr}$	57.27	33.92	45.60
$\Delta R_{DS_{on}}$ at 35° C	%	3.50	3.50	3.50
$\Delta R_{DS_{on}}$ at 140° C	%	11.0	12.1	11.55
$\Delta R_{DS_{on}}$ at 230° C	%	18.25	16.50	17.375

IV. CONCLUSION

In conclusion, a single-module power cycling platform for SiC MOSFETs has been designed and successfully implemented. The results from the devices tested under thermal stress given by $\Delta T_j = 165^\circ \text{C}$ show a consistent increase in $R_{DS_{on}}$ as intended.

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