An mm-Wave CMOS/Si-Photonics Reconfigurable Hybrid-Integrated Heterodyning Software-Defined Radio Receiver

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***Abstract*— This article presents a re-configurable hybrid millimeter-wave (mm-wave) software-defined radio (SDR) receiver that integrates silicon photonics (SiPhs) and complementary metal–oxide–semiconductor (CMOS) chips. The SDR system leverages a programmable photonic integrated circuit (PIC) with high-Q filters, enabling versatile channel selection, image rejection, and jammer rejection capabilities over a tunable frequency range of 30–45 GHz and a bandwidth of 3–5 GHz. It is also capable of autonomously detecting and simultaneously rejecting up to four out-of-band (OOB) blockers, providing >80-dB rejection for two blockers (45 dB from the bandpass filter (BPF) and >35 dB from the notch filter) and >65 dB for four blockers (the notch filter provides >20 dB) for blockers as close as 1.25 GHz to the desired signal to enhance SDR robustness in crowded spectral environments. Moreover, signal downconversion and compensation for photonics-based losses yield an in-band spurious-free dynamic range (SFDR) of 50 dB over 5-GHz bandwidth (BW) and an error vector magnitude (EVM) measurement of −30 dB when processing a 100-MSymbol/s 64-QAM signal under the influence of two −10-dBm OOB blockers at 5- and 10-GHz offsets. Based on the agreement between simulation and measurement results, this article discusses link optimization and provides a recommendation for improvements in SFDR.**

***Index Terms*— Coherent detection, millimeter-wave (mm-wave) wideband radio receivers, optical heterodyning, programmable silicon photonic (SiPh) filters, reconfigurable radio frequency, SiPh integration, software-defined radio (SDR).**

I. Introduction

GROWING demand for millimeter-wave (mm-wave) wideband receivers, which operate beyond 30 GHz, arises from the increasing need for wireless access and enhanced data throughput. However, they face a significant challenge in maintaining performance, especially when dealing with both in-band and out-of-band (OOB) blockers. Blocker signals, often generated by powerful nearby transmitters, present a substantial issue as they not only diminish receiver sensitivity but also introduce unwanted in-band interference, notably third-order intermodulation distortion (IM_3), which can severely degrade received signal quality. Conversely, a reconfigurable software-defined radio (SDR) receiver provides operational flexibility by aggregating multiple contiguous frequency bands for adaptability to diverse modulation schemes. This SDR excels at handling in-band signals and reducing OOB blockers, enabling multichannel wideband operation. Consequently, the spurious-free dynamic range (SFDR) has become a main system performance indicator as it encompasses both noise and distortion effects. Nevertheless, implementing SDR receivers for mm-wave frequencies with high constant SFDR and robust interference mitigation is a challenging task that often requires either limiting the bandwidth of operation or developing effective means to reject blockers.

A direct analog SDR receiver front end, as shown in Fig. 1(a), comprises a band-select filter [1], an mm-wave low noise amplifier (LNA), and an analog-to-digital converter (ADC). This front end directly processes the mm-wave band in the range of 30–45 GHz using a wideband filter, amplifying it to optimize gain and SFDR. However, the high ADC sampling speed and dynamic range requirements lead to substantial power consumption [2]. In Fig. 1(b), a downconversion approach is taken [3], using mixers and image-reject filters for mm-wave frequency downconversion and image reduction. This approach reduces the demand on the ADC speed. Nevertheless, achieving a higher dynamic range remains a challenge due to the limited quality factor of integrated passives. The proposed reconfigurable SDR architecture, as depicted in Fig. 1(c), includes a bandpass filter (BPF), a notch filter, a blocker detection unit, a local oscillator (LO)-image-reject filter, a baseband (BB) mixer, a BB low-pass filter (LPF), and an amplifier. It demonstrates tunable channel selection and OOB blocker rejection and performs heterodyning within a 5-GHz IF bandwidth. Yet, achieving programmability and high performance with traditional electronic filters is challenging due to limited component quality on silicon substrates [4].

Radio frequency (RF) silicon photonics (SiPh) technology has the potential to enhance mm-wave SDR receivers by providing integrated, high-quality, wideband, and reconfigurable

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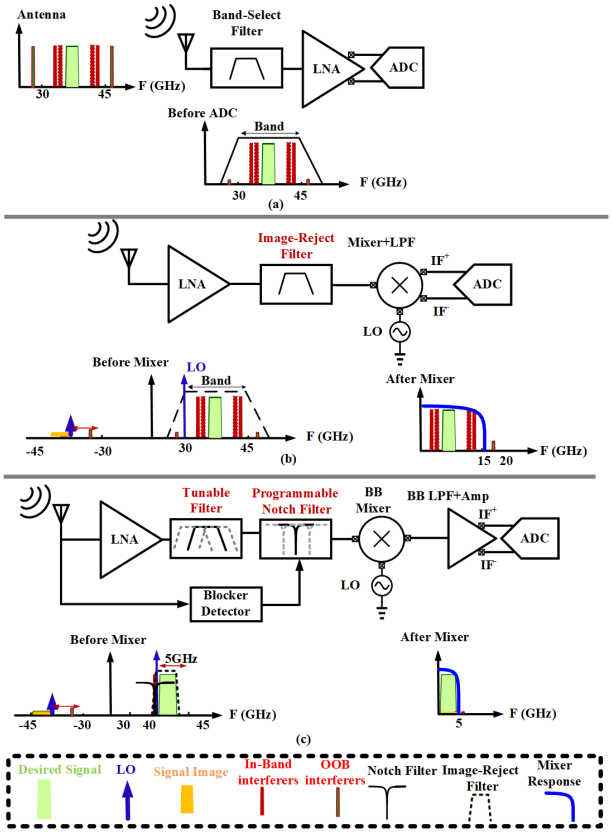


Fig. 1. Comparison of different conceptual system architectures for mm-Wave SDR receivers. (a) Direct SDR. (b) SDR with downconversion mixer and image-reject filter. (c) Proposed reconfigurable SDR.

filters across a broad spectral range, surpassing the capabilities of conventional electronic filters [5], [6], [7]. Rapid filter reconfiguration, blocker cancellation, and OOB rejection are essential for effective spectrum utilization [8]. Photonic infinite impulse response (IIR) filters with sharper filtering and better roll-off can enable mm-wave SiPh reconfigurable bandpass and notch filters to meet these requirements [9]. Addressing challenges, such as photonic process variations, and RF parameter optimization, remains critical for effective RF integration. While works [10], [11], [12] address RF-compatible calibration for a single photonic integrated filter and work [13] discusses photonic integrated circuit (PIC) optimization for direct detection, it is worth noting that this work covers these aspects for a heterodyning SDR system.

This photonically assisted SDR receiver utilizes a programmable PIC with high-Q filters, operating in the 30–45-GHz range, and featuring a complementary metal–oxide–semiconductor (CMOS) post-amplifying stage. It autonomously detects and rejects up to four strong OOB blockers while achieving more than a measured 80-dB rejection for two blockers and over 65 dB for four. The receiver maintains high in-band signal quality, with a 50-dB SFDR and −30-dB error vector magnitude (EVM) when encountering two −10-dBm OOB blockers for a 100-MSymbol/s 64-QAM desired signal at 5- and 10-GHz offset frequencies. This proof-of-concept extends our previous work [11], by adding a comprehensive system architecture analysis, design, and simulations. Furthermore, the system is optimized for SFDR to achieve the maximum SFDR across the entire bandwidth. In addition, it includes PIC and system simulation results for the SDR receiver, a detailed discussion of calibration, an in-depth examination of filtering, and additional functional measurements of the PIC and the SDR. The work also delves into a discussion and comparison of this work with various other works.

II. System Architecture and Frequency Planning

A. Overview and System Operation

Drawing upon the proposed reconfigurable SDR in Fig. 1(c), the photonically assisted hybrid SDR system in Fig. 2 combines a SiPh PIC with CMOS amplifiers. It implements the programmable filters, blocker detector, and coherent detection with PIC while using CMOS for the BB LPF and amplifier. The PIC features two input grating couplers, one for the optically modulated mm-wave signal (with power of P_S) and another for the mm-wave LO (with a power of P_{LO}). In the signal path, there is a tunable wideband fourth-order BPF comprising five tunable ring resonators (output at Point A) for channel selection, image, and jammer rejection. In addition, a tunable notch filter (output at Point B) is equipped with spectrum monitoring and jammer rejection capabilities, consisting of a directional coupler and four ring resonators for jammer rejection and two ring resonators for jammer detection. The LO path includes an LO image-reject filter composed of a ring resonator and monitoring coupler to filter the image of the LO signal (output at Point C). The jammer detection path consists of two rings that can locate interferers. Both signals on these paths (Points B and C) are combined and downconverted to IF using a directional coupler and balanced photodiode (PD), consisting of a pair of back-to-back PDs (output at Point D). Each ring resonator in the signal/LO paths is paired with a local directional coupler and a low-bandwidth (BW) transimpedance amplifier (TIA) for monitoring purposes. In addition, in the LO path, a 5% coupler connected in series with the ring resonator BPF is used to monitor a segment of the signal for calibration and tuning of the LO-BPF. An analog control signal is employed to reprogram the PIC filter responses based on the feedback from a local monitor PD and the input frequency requirements. The output current signal from the PD is centered at the frequency difference between the two paths: ($f_{\mathrm{IF}} = f_S - f_{\mathrm{LO}}$). This signal enters the CMOS unit, which provides signal conditioning through three amplifying stages and includes an offset correction circuit. The TIA converts the current into an amplified differential voltage signal, the variable gain amplifier (VGA) offers additional tunable gain, and the buffer supplies an output to drive a 50-Ω load (Point E). The offset correction circuit can correct for dc current offset at the PD output. The TIA gain is programmed by resistors and the VGA is programmed by the current source.

Fig. 3(a) illustrates the complete SDR receiver system, featuring photonically assisted hybrid CMOS/PIC chips, external modulators, and a balanced detector for frequency downconversion. This system is designed to receive the signal transmitted by the desired transmitter (transmitted power of P_{tr}

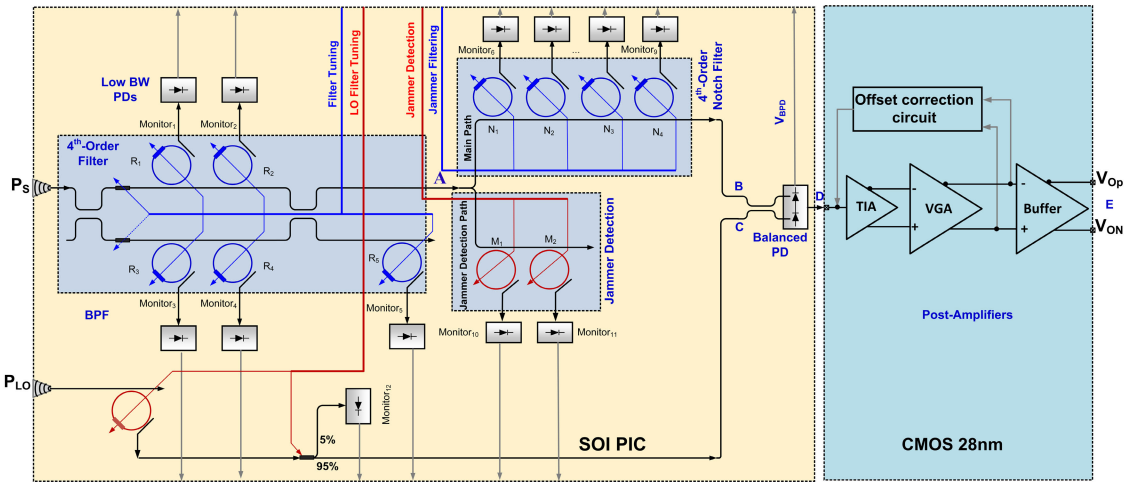
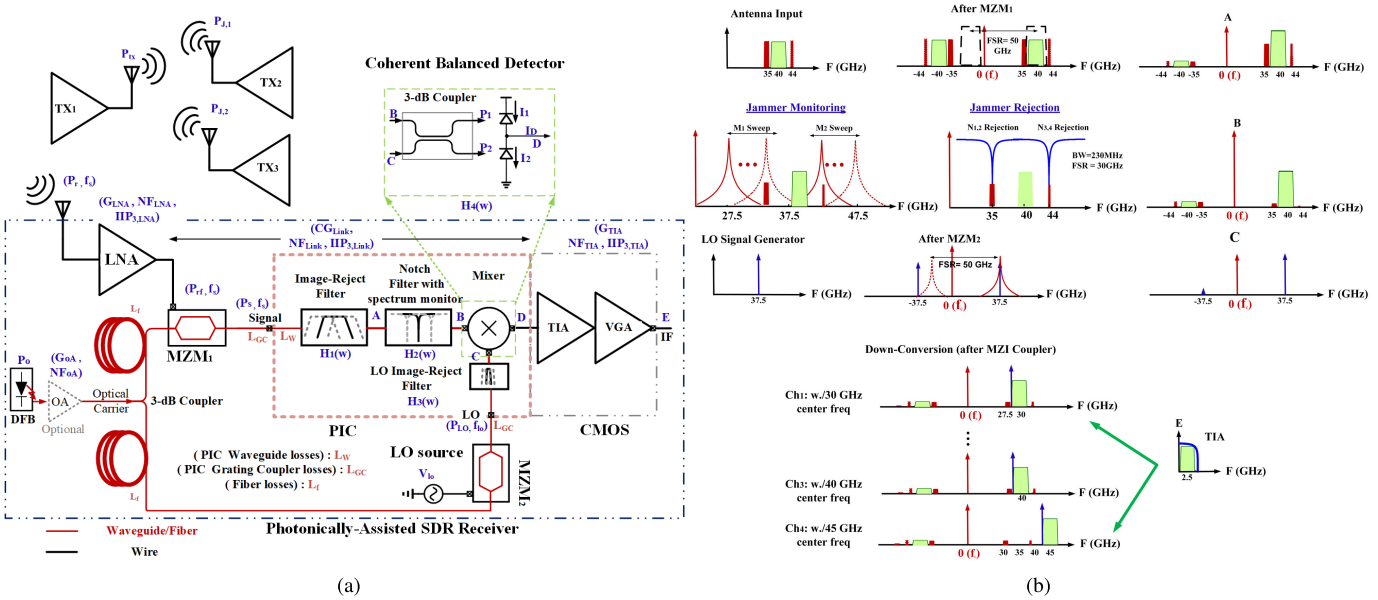


Fig. 2. Proposed photonically assisted hybrid-integrated SDR architecture.



(a) (b)

Fig. 3. (a) Full receiver system of the proposed photonically assisted SDR architecture. (b) Frequency planning of the SDR.

and received power of P_r) while managing interference from adjacent transmitters located in different channels ($P_{J_{1,2}}$) due to its reconfigurability and filtering, as explained in the following frequency plan. The mm-wave downconverter, as depicted in Fig. 3(a), utilizes a single laser source (with power of P_0 and wavelength λ or frequency w_c). The optical power of the laser can be boosted using an optical amplifier (OA), with its output connected to a 3-dB coupler, which divides the power into two paths (signal and LO paths). The divided lights are coupled with two Mach–Zehnder modulators (MZMs; $\text{MZM}_{1,2}$). MZM_1 is responsible for converting the amplified received signal by the LNA into the optical domain (P_S), effectively directing it to the signal input, while MZM_2 assumes the role of converting the LO tone (at f_{LO} and power P_{LOS}) into the optical domain (P_{LO}), seamlessly coupling it to the LO port of the PIC. Within the PIC, two mm-wave SiPh BPFs ($H_1(w)$ is the signal BPF response and $H_3(w)$ is the LO-BPF) are integrated for image rejection and the selection of upper sidebands (USBs). While the signal path delivers a BW of up to 5 GHz, the LO path offers a 1-GHz BW. Notably, both filters are fully tunable and programmable (in center frequency, rejection, and BW to accommodate various requirements. Moreover, the signal path features a photonic notch filter [$H_2(w)$] for filtering the optically modulated mm-wave wideband signals to provide more rejection capability of up to 20 dB to four different OOB blockers. Subsequently, the mm-wave and LO modulated USB signals are combined using an integrated hybrid coupler on the same chip, generating two optically mixed signals. Finally, a balanced PD with a bandwidth of up to 5 GHz generates an electrical current at the first beating difference frequency, effectively converting the mm-wave into an IF.

B. Frequency Planning

Fig. 3(b) outlines the frequency plan for the proposed photonically assisted SDR receiver system, encompassing

the desired mm-wave signal channel operating within the frequency range of 37.5–42.5 GHz, along with two OOB blockers at 35 and 44 GHz received through the antenna. MZM_1 operates at Q-bias point for maximum SFDR while modulating the input light from a distributed feedback (DFB) laser at 1550 nm. A low signal level is assumed to avoid multiharmonic distortion, due to MZM nonlinearity, limiting the blocker power to −10 dBm. The signal BPF is configured for the desired channel with f_S of 40-GHz center frequency and a 5-GHz bandwidth, facilitating image rejection and achieving over 35-dB interference rejection at Point A. The image is positioned at a 40-GHz frequency offset to the left of the carrier, allowing the BPF to provide >40-dB rejection while also rejecting the two interferers and their images at 35 and 44 GHz by >35 dB. Jammer detection is performed through two ring monitors, each searching half of the 30–45-GHz desired band, to detect the presence of interferers and configure the notch filters accordingly. The notch filter provides interference rejection, delivering >64-dB rejection of interference frequencies at Point B (two notches/each interfere) for each jammer, placed automatically with jammer detection information. $Monitor_1$ detects the interfere at 30 GHz, and $Notch_{1,2}$ are placed on top of the first jammer, while $Monitor_2$ detects the 45-GHz interfere, and $Notch_{3,4}$ are placed on top of the second jammer, each providing >64-dB rejection. The LO signal at $f_{LO} = 37.5$ GHz drives MZM_2, and the LO image-reject filter selects the upper sideband of the modulated signal, effectively rejecting the LO image (−27.5 GHz with respect to the carrier) at Point C. The mixer combines both signals at each of the four channels, along with their respective LO signals, into two outputs, resulting in a 2.5-GHz IF output from the PIC at Point D as a current difference. Finally, the CMOS amplifies these signals to drive the loading instrument at Point E. For reconfigurable operation, a few possible center frequencies for the desired signal are f_S : 30, 35, 40, and 45 GHz, with corresponding LO center frequencies of f_{LO} : 27.5, 32.5, 37.5, and 42.5 GHz, which also correspond to the LO-BPF, thus always producing an IF center frequency of 2.5 GHz at the final output.

III. Reconfigurable SDR System Design

This section formulates key performance metrics for a hybrid SDR receiver system [Fig. 3(a)]. A single-tone approach is employed, assuming small-signal input voltages from the antenna as $V_r \sin(w_s t)$ and from the LO as $V_{LO} \sin(w_{LO} t)$. The photonic link metrics include power conversion gain (CG_{Link}), noise figure (NF; NF_{Link}), third-order intercept point ($IIP_{3,Link}$), and spurious-free dynamic range ($SFDR_{Link}$). Also, the influence of the LNA is considered, with a power gain (G_{LNA}), NF (NF_{LNA}), and third-order intercept point ($IIP_{3,LNA}$). Furthermore, the impact of post-amplifiers (G_{TIA}, NF_{TIA}, and $IIP_{3,TIA}$), where G_{TIA} is the combined power gain, defined as $((V_E/I_D))^2$, is used to derive CG, NF, IIP_3, and SFDR for the entire system.

A. System Analysis

In the work [14], an expression is provided for the gain of a coherent detection link comprising two laser sources, a single differential MZM, an OA, and an electrical amplifier. However, the focus of this work is on the analysis of overall receiver gain in scenarios where two single-drive MZMs, as well as multiple post-amplifiers and a pre-amplifier, are employed to enhance link performance. Equation (1) represents the electric field at Point C (E_C), which includes three terms due to carrier and signal interactions, with coefficients (E_{C0}, E_{C1}, and E_{C-1}) corresponding to the carrier, USB, and LSB, respectively. Here, P_0 represents the laser power, G_{OA} is the gain of the OA after the laser, L_{MZM} represents the MZM losses, $\phi_{DC1,2}$ represents the dc bias angle of $MZM_{1,2}$, and V_π is the half-wave voltage of the MZM. Furthermore, L_{PIC} represents the overall PIC losses from grating coupler to PD input, including the directional coupler, that is, $L_{PIC} = IL_{WG} + IL_{GC} + IL_{DC}$. Here, IL_{WG} represents the waveguide insertion loss (IL), given by $IL_{WG} = 10 * \log_{10}(L_{WG})$, where L_{WG} is the waveguide losses expressed as a ratio, L_{GC} is the grating coupler losses, and L_{DC} is the directional coupler losses. Moreover, $V_{LO} = (2\eta Z_{in} P_{LOS})^{1/2}$, where Z_{in} is the MZM input impedance, P_{LOS} is the LO source power, and η is the MZM extinction ratio. In a similar manner, the electric field at Point B (E_B) can be determined by replacing (ϕ_{DC2}, V_{LO}, w_{LO}, and H_3) with (ϕ_{DC1}, V_{rf}, w_s, and $H_1 H_2$), where V_{rf} represents MZM_1 input voltage ($V_{rf} = (2\eta Z_{in} P_r G_{LNA})^{1/2}$), in which P_r is the received antenna power

$$
\begin{aligned}
E_C &= E_{C0} e^{j w_c t} + E_{C1} e^{j(w_c + w_{LO})t} + E_{C-1} e^{j(w_c - w_{LO})t} \\
E_{C0} &= j \sqrt{\frac{P_0 G_{OA}}{2 L_{MZM} L_{PIC}}} \cos\phi_{DC2} H_3(w_c) \\
E_{C1} &= \frac{\pi V_{LO}}{4 V_\pi} \sqrt{\frac{P_0 G_{OA}}{2 L_{MZM} L_{PIC}}} \sin\phi_{DC2} H_3(w_c + w_{LO}) \\
E_{C-1} &= \frac{-\pi V_{LO}}{4 V_\pi} \sqrt{\frac{P_0 G_{OA}}{2 L_{MZM} L_{PIC}}} \sin\phi_{DC2} H_3(w_c - w_{LO}). \quad (1)
\end{aligned}
$$

The currents through each PD are I_1 and I_2, and they are determined by (2), where ρ represents the PD responsivity

$$
\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{\rho}{2} \begin{bmatrix} |E_B|^2 + |E_C|^2 - j E_C E_B^* + j E_B E_C^* \\ |E_B|^2 + |E_C|^2 - j E_B E_C^* + j E_B^* E_C \end{bmatrix} \quad (2)
$$

$$
I_D = I_1 - I_2 = 2\rho |E_{B1}||E_{C1}| \sin((w_s - w_{LO})t). \quad (3)
$$

Considering E_B, after the signal BPF and jammer rejection, if $H_1(w_c) = H_1(w_c - w_s) = 0$, $H_1(w_c + w_s) = (L_1)^{1/2}$, and $H_2(w_c + w_s) = (L_2)^{1/2}$, meaning that both the image and carrier are rejected, while the main signal power experiences the in-band loss of $L_1 * L_2$, then E_B reduces to the USB only. Similarly, in the LO path, if $H_3(w_c) = H_3(w_c - w_{LO}) = 0$ and $H_3(w_c + w_{LO}) = (L_3)^{1/2}$, then E_C reduces to the USB only, experiencing an in-band power loss of L_3 as it passes through H_3. Thus, the first two terms in (2) ($|E_B|^2 + |E_C|^2$) reduce to dc currents only, resulting in a net ac current at Point D, denoted as I_D and given by (3). The coherent detection link conversion gain, defined as $CG_{Link} = (P_{D,IF}/P_{rf})$, and the overall receiver conversion gain, defined as $CG = (P_{E,IF}/P_r)$, are given by (4), as shown at the bottom of page 6, where $Z_{o,PD}$ is the impedance seen looking at PD output, Z_{TIA} is the transimpedance of the TIA, and Z_L is the load impedance.

TABLE I
KEY PARAMETER VALUES FOR THE SDR RECEIVER SYSTEM

Variable	BW	f_r	P_r	P_J	G_{LNA}	NF_{LNA}	$IIP_{3,LNA}$	P_0	RIN
Value	$5GHz$	$30GHz$	$-52dBm$	$-10dBm$	$22dB$	$8dB$	$10dBm$	$13dBm$	$-154dBc/Hz$
Variable	G_{OA}	NF_{OA}	$Z_{in} = Z_L$	η	IL_{MZM}	V_π	V_{LO}	$\phi_{DC1,2}$	IL_{WG}
Value	$16dB$	$8dB$	50Ω	0.5	$5dB$	$7V$	$0.7V$	$\frac{\pi}{2}$	$1dB$
Variable	IL_{GC}	IL_{PIC}	ρ	IL_1	IL_2	IL_3	Z_{TIA}	$IIP_{3,TIA}$	NF_{TIA}
Value	$7.5dB$	$8.5dB$	$0.6A/W$	$-4.5dB$	$-1dB$	$-3.5dB$	$75dB\Omega$	$-3dBm$	$3dB$

Equivalently, the contribution of the TIA/VGA to the overall SDR power conversion gain CG is a power gain of $G_{\text{TIA}} = (Z_{\text{TIA}}^2/Z_L Z_{o,\text{PD}})$.

An expression for the NF of the link is provided in [14]. However, in this study, the effect of two single-drive MZMs, pre- and post-amplifiers, is added to the NF analysis. The main sources of noise at the output include thermal noise, shot noise, relative intensity noise (RIN), and amplified spontaneous emission (ASE), all of which are present in the system [14]. The ASE noise from the OA can be quantified using the formula $[S_{\text{ase}} = (\text{hf}(G_{\text{oa}} - 1)/2) \cdot 10^{(\text{NF}_{\text{OA}}/10)}]$, where NF_{OA} is the NF of the OA, h represents Planck's constant, and f is the optical frequency. NF_{Link} is provided in (5), as shown at the bottom of the next page, where the source of each noise is annotated [14]. Moreover, balanced detection within a coherent detection system accomplishes partial cancellation of specific noise components. The extent of effectiveness in this cancellation process is quantified by the parameter γ, which is found to be 0.51 experimentally [14]. The total NF for the entire receiver system is crucial because it directly influences the output signal-to-noise ratio at the detection stage. The impact of the LNA and the post-amplifiers on the overall NF is characterized by the cascaded RF system equation. The third-order intercept point ($\text{IIP}_{3,\text{Link}}$) for the link, as provided in [14], is given by $\text{IIP}_{3,\text{Link}} = (32 * V_\pi^2/2\pi^2 * Z_{\text{in}})$. Furthermore, the overall linearity is calculated by IIP_3 for the entire receiver system, by the cascaded system equation, which relates to the link, the LNA, and the TIA. The noise floor is defined as noise floor $= K * T * \text{BW} * \text{NF}$, and the overall SFDR is calculated using $\text{SFDR} = (2/3) * (\text{IIP}_3 + 174 - \text{NF})$.

B. System Design and Simulations

In order to quantify the key receiver system performance parameters, the typical values of the parameters for each component are summarized in Table I. The proposed system is designed with 5-GHz channel BW and a minimum desired signal of -52 dBm ($P_r = -52$ dBm) for a 64-QAM modulated signal, that is, 5 GHz apart from each interferer. The signal has a center frequency (f_s) in the range of 30–45 GHz (with 30 GHz chosen for analysis), allowing interference up to -10 dBm (P_J) both driving MZM_1. The LNA specifications are chosen to be: G_{LNA} of 20 dB, NF_{LNA} 8 dB, and linearity $\text{IIP}_{3,\text{LNA}}$ of 0 dBm. The laser has a power P_0 of 13 dBm, with an RIN noise of -154 dBc/Hz. The OA has G_{OA} of 16 dB and NF_{OA} of 8 dB. The fiber length is 10 m with 0.4-dB/km losses at λ of 1550 nm, resulting in 0.004-dB loss, which can be neglected. The input impedance for MZM, Z_{in}, and the load impedance Z_L are 50 Ω; however, the load is single-ended in this case at Point E. For the MZM, the IL IL_{MZM} is 5 dB, η is estimated to be 0.5, and V_π is 7 V. The LO MZM_2 is driven by a source with voltage $V_{\text{LO}} = 0.7$ V. Both MZM_1 and MZM_2 are biased at the Q-point $V_B = (V_\pi/2)$, i.e., $\phi_{\text{DC1,2}} = (\pi/2)$ radians. For the PIC, a waveguide with a simulated IL_{WG} of 1.2 dB/cm is used with different lengths for the signal and LO paths, resulting in an average calculated IL_{WG} of 1 dB, including coupler IL. In addition, IL_{GC} and ρ are simulated to be 7.5 dB and 0.6 A/W at 1550 nm, respectively. As for the filters on the PIC, their in-band ILs IL_1–IL_3 are simulated to be -4.5, -1, and -3.5 dB, respectively. For the CMOS chip, Z_{TIA} is 75 dBΩ, resulting in G_{TIA} being 35 dB with NF_{TIA} of 3 dB and $\text{IIP}_{3,TIA}$ of -3 dBm.

The estimated link parameters are calculated as follows: $\text{CG}_{\text{Link}} = -30.1$ dB, obtained using (4), $\text{NF}_{\text{Link}} = 33.1$ dB, obtained using (5), $\text{IIP}_{3,Link} = 33.0$ dBm, and the $\text{Noise Floor}_{\text{Link}}$ is -73.8 dBm. With the association of the LNA and the TIA, the overall system parameters change, resulting in a CG of 25.17 dB, an NF of 9.8 dB, an estimated IIP_3 of 3.9 dBm, and a Noise Floor of -97 dBm. The overall SFDR is 113 dB·$\text{Hz}^{2/3}$ (67 dB for 5-GHz BW).

The power flow of the signal, noise, and jammers in the receiver system after various blocks is shown in Fig. 4(a). Both the signal and the jammers are initially amplified by the LNA gain. They then experience the PIC effect: the signal suffers from the PIC and filter losses, while the jammers selectively experience an extra OOB rejection of 80 dB, effectively reducing the jammers to below the noise floor of -97 dBm. This is followed by a gain from the TIA-VGA stage. The jammer level before the LNA is -10 dBm, which is less than the $\text{IIP}_{3,\text{LNA}}$, and then, the jammer is amplified to $+10$ dBm, which is less than the $\text{IIP}_{3,\text{PIC}}$, ensuring linear operation. The noise power at the output of each block is shown as well, to indicate the signal-to-noise ratio (SNR) level. The noise power initially starts at the antenna as KTB noise input, of -76.9 dBm. Due to the LNA, it rises to -46.9 dBm, reflecting the noise added by the LNA. With the combined effects of the PIC and LNA, it reduces to -72.1 dBm (following the main signal), and finally, due to the TIA, it goes to -35.9 dBm. Thus, the output SNR is 10.8 dB. In addition, to optimize the overall receiver SFDR, the effects of V_{LO}, NF_{TIA}, ϕ_{DC2}, and NF_{LNA} are studied. The optimized SFDR under the effects of the LNA and Φ_{DC1} were previously studied in [13]. Given the

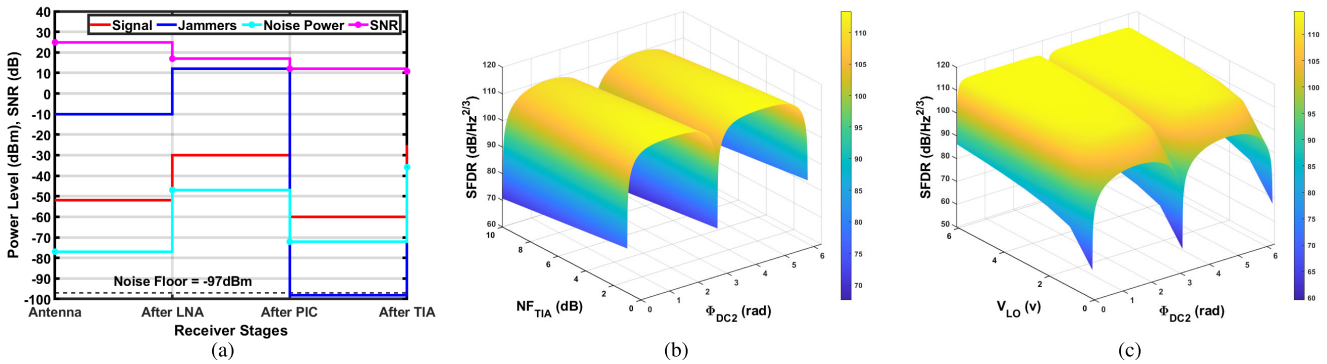


Fig. 4. (a) Signal, jammer, and noise power levels flow in the receiver system. (b) Optimization of the SFDR by ϕ_{DC2} and $\mathrm{NF_{TIA}}$. (c) Optimization of the SFDR by ϕ_{DC2} and V_{LO}.

significant losses in the photonic link CG $= -30.1$ dB, it is crucial to examine the $\mathrm{NF_{TIA}}$, as it significantly impacts the overall NF. Fig. 4(b) shows the SFDR optimization under the effect of LO path controlled by $\mathrm{MZM_2}$ bias angle ϕ_{DC2} and $\mathrm{NF_{TIA}}$. Minimum SFDR happens at $\phi_{\mathrm{DC2}} = 0$ and π since P_{LO} coupled into PIC is decreased in this condition. Notably, the maximum SFDR exceeding 110 dB·Hz$^{(2/3)}$ is achieved at different values of $\mathrm{NF_{TIA}}$ while changing ϕ_{DC2}. However, while the SDR receiver NF degrades with an increase in $\mathrm{NF_{TIA}}$, changing ϕ_{DC2} can reduce this effect in the SFDR, thus relaxing TIA design. Also, in Fig. 4(c), the SFDR is optimized while varying $\mathrm{MZM_2}$ drive voltage V_{LO} and ϕ_{DC2} from the LO path. The trend suggests that as V_{LO} voltage increases, so does the SFDR, but it peaks when ϕ_{DC2} at the Q-point. Moreover, V_{LO} higher than 2.5 V appears to have a limited effect on SFDR; however, it would introduce other nonlinearities than not captured by this small-signal analysis. Finally, Fig. 5 shows a plot of SFDR contours against $\mathrm{NF_{TIA}}$ and $\mathrm{NF_{LNA}}$. The peak SFDR value of 113 dB·Hz$^{(2/3)}$ is achieved while limiting the $\mathrm{NF_{TIA}}$ to 2.1 dB and the $\mathrm{NF_{LNA}}$ to 6.7 dB.

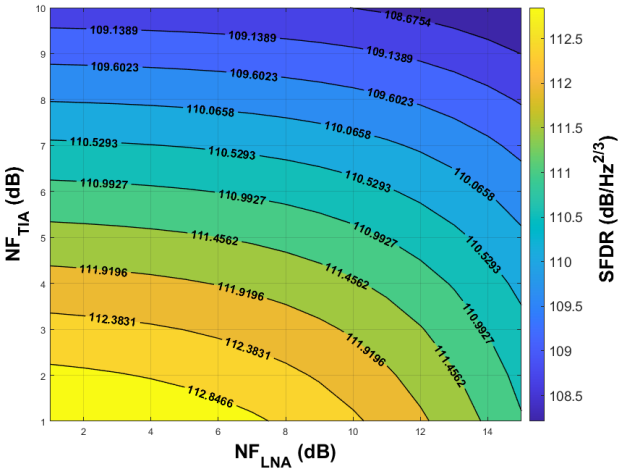


Fig. 5. SFDR contour versus $\mathrm{NF_{LNA}}$ and $\mathrm{NF_{TIA}}$.

IV. SDR Circuit Implementation

Fig. 6 illustrates the circuit schematic of the photonically assisted SDR hybrid-integrated PIC and CMOS IC. Each IC is optimized for the system specifications required at either mm-wave or IF frequencies. PICs utilize silicon (Si) substrates with buried oxide (BOX), constituting the silicon-on-insulator (SOI) substrate as indicated in [13]. In this section, we discuss the filter design for PICs and their usage in filtering both signal

$$\mathrm{CG} = G_{\mathrm{LNA}} \cdot \overbrace{\frac{4\eta * L_1 * L_2 * L_3 * \left(\rho\pi^2 * P_0 * G_{\mathrm{OA}} \sin(\phi_{\mathrm{DC1}}) \sin(\phi_{\mathrm{DC2}}) V_{\mathrm{LO}}\right)^2 \cdot Z_{\mathrm{in}} Z_{o,\mathrm{PD}}}{(4V_\pi)^4 (L_{\mathrm{PIC}} \cdot L_{\mathrm{MZM}})^2}}^{\mathrm{CG_{Link}}} \cdot \frac{Z_{\mathrm{TIA}}^2}{Z_L Z_{o,\mathrm{PD}}} \tag{4}$$

$$\begin{aligned}\mathrm{NF_{Link}} = \frac{Z_{o,\mathrm{PD}}}{4KT_0 C G_{\mathrm{Link}}} \Bigg(& \overbrace{\frac{4KT_0}{Z_{o,\mathrm{PD}}}\left(\frac{\mathrm{CG_{Link}}}{2}+1\right)}^{\text{MZM/PD thermal noise}} + \overbrace{2q\rho\left(|E_{B1}|^2+|E_{C1}|^2\right)}^{\text{LO/signal shot noise}} + \overbrace{2\rho^2|E_{B1}|^2|E_{C1}|^{2\mathrm{RIN}}}^{\text{beating LO/signal RINs}} + \overbrace{4q\rho S_{\mathrm{ase}} BW}^{\text{shot noise due to ASE}} \\ & + \underbrace{4\rho^2|E_{C1}|^2 S_{\mathrm{ase}}}_{\text{beating LO/ASE noises}} + \gamma\Bigg(\underbrace{\mathrm{RIN}\left(\rho|E_{B1}|^2\right)^2}_{\text{RIN noise from signal path}} + \underbrace{\mathrm{RIN}\left(\rho|E_{C1}|^2\right)^2}_{\text{RIN noise from LO path}} + \underbrace{4\rho|E_{B1}|^2 S_{\mathrm{ase}}}_{\text{beat between ASE and signal}} + \underbrace{4\rho^2 S_{\mathrm{ase}}^{2\mathrm{BW}}}_{\text{ASE-ASE beat noise}} \Bigg) \Bigg)\end{aligned} \tag{5}$$

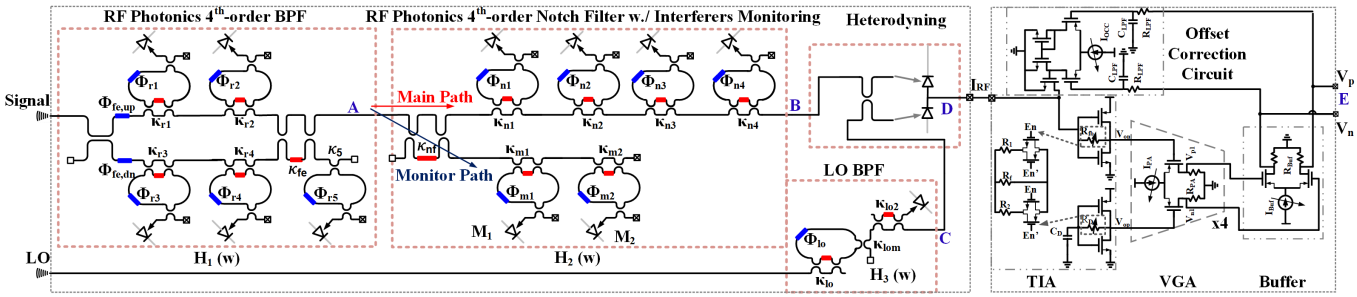


Fig. 6. Circuit implementation of the photonically assisted SDR.

TABLE II
KEY SELECTED PARAMETER VALUES FOR SDR RECEIVER CIRCUITS

Variable	$\kappa_{r1}=\kappa_{r3}$	$\kappa_{r2}=\kappa_{r4}$	$\phi_{r1}=-\phi_{r3}$	$\phi_{r2}=-\phi_{r4}$	$\phi_{fe,up}=-\phi_{fe,dn}$	κ_{fe}	ϕ_{r5}	κ_{nf}	ϕ_{n1}
Value	0.3461	0.1223	-0.1732	0.3503	-1.3768	0.5	0	0.1	0.1732
Variable	κ_{n1}	ϕ_{n2}	κ_{n2}	ϕ_{n3}	κ_{n3}	ϕ_{n4}	κ_{n4}	ϕ_{m1}	κ_{m1}
Value	0.3200	0.1732	$0.3200dB$	0.125	0.2152	0.125	0.2152	0.217	0.314
Variable	ϕ_{m2}	κ_{m2}	ϕ_{lo}	κ_{lo}	κ_{lom}	κ_{lo2}	$R_f=R_1$	R_{LPF}	C_{LPF}
Value	0.112	0.75	0.6	0.145	0.112	0.135	510Ω	$762l\Omega$	$985fF$

and LO paths. Then, we will discuss the CMOS chip design of the TIA to amplify the IF signal and drive the real-time scope 50-Ω impedance.

A. PIC Design and Simulations

The Mach–Zehnder interferometer (MZI), when paired with a ring resonator, acts as a tunable directional coupler that enables precise manipulation and observation of the resonator's coupling ratio. Incorporating a feedback phase shifter within the resonator's feedback loop further provides control over its resonance frequency. Introducing a 5% tapping coupler and a PD to the ring resonator enables monitoring of its drop port response. Such an arrangement ensures automatic calibration, which intelligently addresses process discrepancies. The MZI-ring is typically characterized with a periodic frequency response, termed the free spectral range (FSR).

In the PIC receiver illustrated in Fig. 6, the incoming signal is first channeled to the RF-photonics 4th-order BPF marked as $[H_1(w)]$ (encompassing $\text{Ring}_{1\text{–}5}$) that has an FSR of 50 GHz. This processed signal then reaches the notch filter $[H_2(w)]$ and is bifurcated into two paths: the primary route and the detection route, enabled by the initial coupler of the notch filter, denoted κ_{nf}. The primary route comprises four rings, each with an FSR of 30 GHz, operating in series as a notch filter ($N_{1\text{–}4}$). In contrast, the detection route includes $M_{1,2}$, also with an FSR of 30 GHz. The frequency response of the notch filter is characterized by $H_2(w)$. Concurrently, an optically modulated LO tone is directed to a 1st-order BPF $H_3(w)$ with an FSR of 50 GHz, selecting the USB.

B. RF-Photonics BPF

Channel-select filters, in their ideal form, demonstrate a stark transition from selection to rejection bands. This ensures minimal IL for the target bands while effectively eliminating unwanted ones. The filter's order determines the OOB rejection value, IL, and the filter's total footprint. In the context of the receiver system, the BPF is designed to have a -3-dB BW of 5 GHz and a reconfigurable center frequency spanning 30–45 GHz. This dictates that the FSR should be greater than the difference including the bandwidth, and thus, an FSR of 20 GHz is chosen to perform multiband selections. Given the relation FSR $= (C/ngL)$, where n_g is the group index and L is the filter length, a larger FSR implies a compact filter and diminished in-band loss. This is because waveguide losses scale linearly with their length. However, aiming for a higher FSR is restricted by the minimum allowed length, notably a heater length of 320 μm. An FSR of 50 GHz is, therefore, chosen. While an increased filter order (N) results in better rejection (R), it also leads to considerable in-band IL. Hence, an order of $N = 4$ is opted for. This 4th-order BPF integrates four rings, two phase shifters, and an MZI coupler, as depicted in Fig. 6. Inspired by [11], the filter is designed for an elliptical response. Standard parameters are demonstrated in Table II. MATLAB simulations, as seen in Fig. 7(a), show an in-band IL of IL 4.5 dB and an OOB rejection of 35 dB (close to 40 dB with 13-GHz offset from center frequency). The tuning feature recalibrates the 4th-order BPF's center frequency, to cover operating channels while having a 5-GHz BW, as elaborated in [6] and [13]. Resembling the design in [7], the filter represents a bandpass response with a 50-GHz FSR, a flexible 3–5-GHz BW, and a center frequency that is tunable between 30 and 45 GHz at Point A.

C. RF-Photonics Notch Filter

The filter, denoted as $H_2(w)$ and illustrated in Fig. 6, is capable of detecting and rejecting up to four interferences

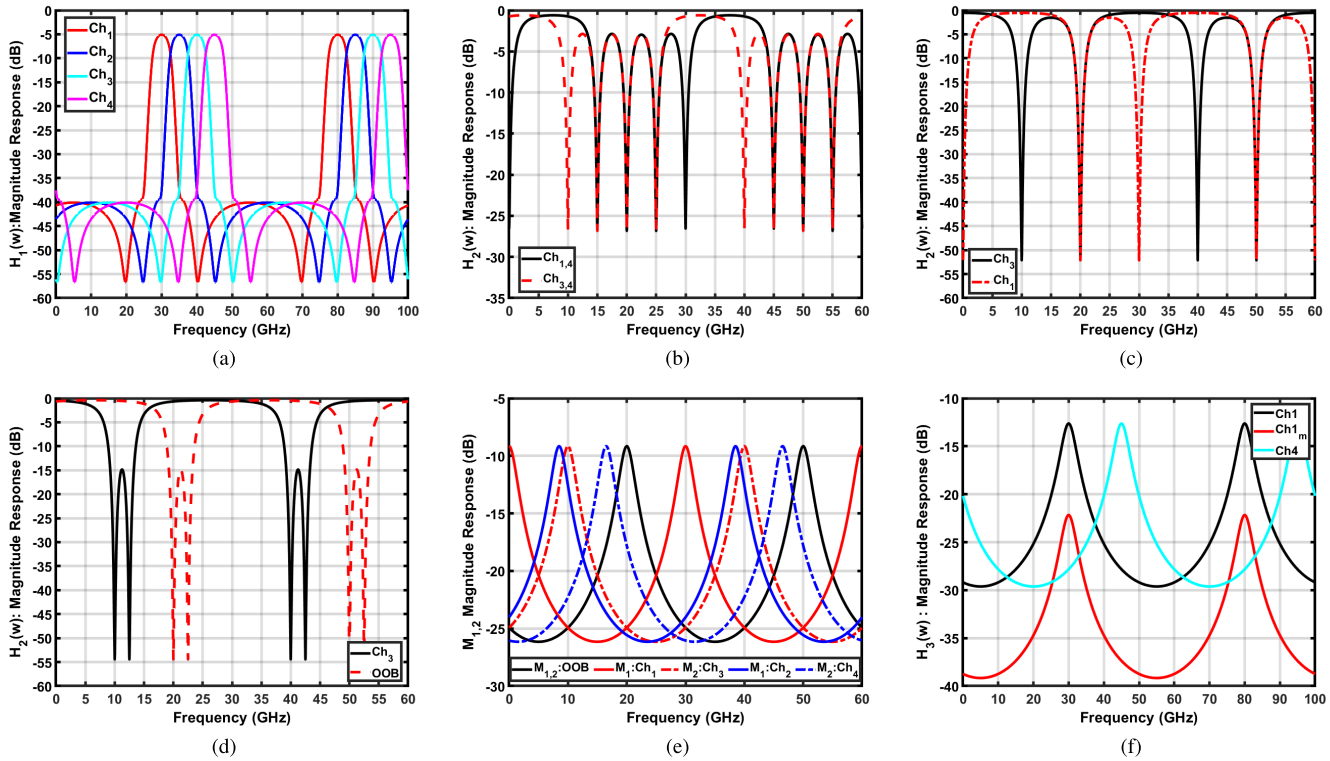


Fig. 7. Simulation results for the PIC, (a) 4th-order BPF $H_1(w)$ transmission response; (b) 1st-order notch filter, $H_2(w)$, showing four notches; (c) 2nd-order notch filter, $H_2(w)$, at 10-GHz center frequency offsets between notches; (d) 2nd-order notch filter, at 2.5-GHz center frequency offsets; (e) monitoring path transmission response; and (f) LO-BPF $H_3(w)$ transmission response.

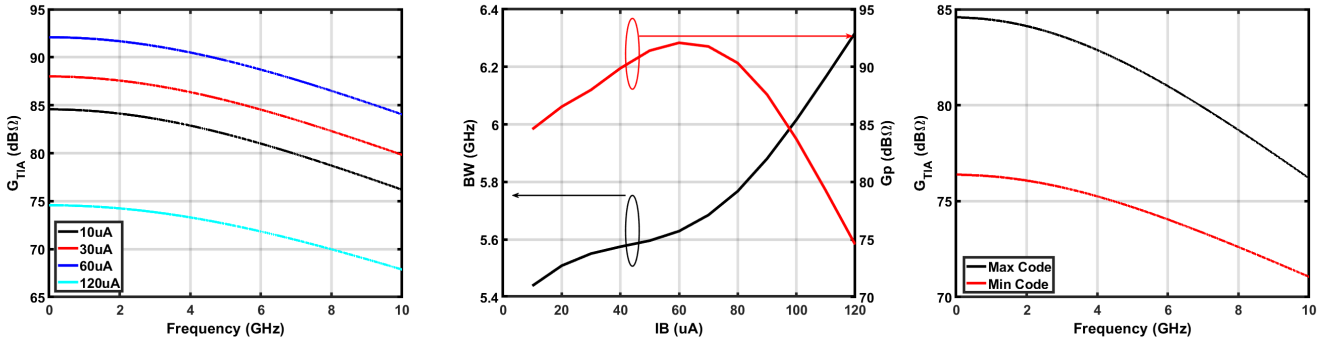
through its dual-path design. The front-end MZI coupler κ_{nf} partitions the incoming signal, allocating 90% of the power to the rejection path and the rest to the monitoring path. The rejection path is composed of four MZI-based rings N_1–N_4, each delivering rejection for narrowband interference, with individual frequency control from f_1 to f_4. The MZI-ring is designed with an FSR of 30 GHz to cover the operating band, as shown in Fig. 7(b). This resonator performs both attenuation and monitoring, peaking at the center frequency f_1, at its monitor while providing maximum amount of rejection at its through port. Intriguingly, a single MZI-ring can serve both as a BPF and a notch filter, emphasizing its adaptability in both interference detection and rejection. When cascading these four different MZI-ring resonators from their through ports, the cumulative effect yields an overall configuration with four first-order notches. Each of these notches corresponds to a different resonance frequency, ranging from f_1 to f_4. The specific relationship between these resonance frequencies and the parameters of the individual resonators can be expressed as (6), where H_{N1-4} denote the frequency responses of individual notches 1–4 [i.e., $H_{N1-4}(w)$]

$$H_2(w) = \sqrt{1-\kappa_{\text{nf}}} \cdot (H_{N1} \cdot H_{N2} \cdot H_{N3} \cdot H_{N4}). \tag{6}$$

The filter's major parameters include FSR, set by the ring's dimensions and influential in enhancing the quality factor (Q), BW, and rejection level. Both BW and rejection level are functions of the coupling ratio κ_r, and thus, a critical coupling value is chosen for maximum rejection. Moreover, the achievable rejection is affected by the spacing between the four notches. Each of the four MZI-based rings introduces a distinct frequency notch, guaranteeing a rejection of $>$25 dB, and can be tuned in center frequency to eliminate undesired signals. With a center frequency offset of 5 GHz, it yields a 1st-order notch filter with four notches, as shown in Fig. 7(b).

The simulations presented in Fig. 7(c) clarify the transmission response of this 4th-order notch filter, $H_2(w)$, illustrating it as a combination of two second-order filters, with their center frequencies spaced 10 GHz apart. Such a configuration can achieve a rejection of up to 52 dB for interferences at specific frequencies, such as 40 GHz (Ch_3) and 50 GHz, leading to rejections at intervals of 10 and 20 GHz, due to the FSR. The progression in notch frequency spacing, evolving from an initial 2.5 GHz [Fig. 7(d)] to a broader 10 GHz [Fig. 7(c)], highlights the filter's capability in rejecting multiple neighboring channels or OOB interference. To realize optimal performance, it is essential to design FSR, rejection level, and BW, all of which are dependent on κ_r. The chosen FSR of 30 GHz ensures a minimal in-band loss of 1 dB for the desired frequency sweep range. The simulated maximum combined rejection at OOB results from the overlap between the notch and the BPF. For instance, at 10 GHz, the BPF provides 50 dB of rejection [shown in red in Fig. 7(a)], and the notch offers 55 dB [indicated in red in Fig. 7(d)], leading to a combined rejection of 105 dB.

The monitoring path of the notch filter, as depicted in Fig. 6, corresponds to the bottom path after the front-end



(a) (b) (c)

Fig. 8. Simulation results for the TIA-VGA gain control at (a) 1.2 V_{DD} versus frequency at different IBs, (b) IB effect on BW and G_p, and (c) resistor control effect on gain.

coupler. This monitoring path combines two MZI-ring resonators, M_1 and M_2, which act as BPFs, each designed to detect interferences within half of the operational band. Each resonator has an FSR of 30 GHz, augmented by two heaters, similar to notch filter. These heaters fine-tune both the resonance frequency and the coupling ratio, thereby setting the filter's order and its BW. The first monitoring M_1 response is detailed by (7), where $H_{d,m1}(w)$ is the drop port response of M_1. Given that M_2 utilizes the through port of M_1 as its input, its response can be articulated by (8). To prevent an overlap of notch and BPF functionalities in M_2, the sweep range of ϕ_{M1} is restricted to bypass the same range covered by M_2. This configuration divides the search domain, into two half bands, and reduces the sweeping time. Consequently, each monitor scans a distinct half of the 30–45-GHz frequency span (M_1: 30–38.75 GHz and M_2: 38.75–45 GHz). The simulation complete monitoring response is presented in Fig. 7(e). Initially, both $M_{1,2}$ are positioned OOB. Subsequently, M_1 addresses the 30–37.5-GHz frequency spectrum, encompassing both Ch_1 (red solid) and Ch_2 (blue solid). In contrast, M_2 searches the subsequent frequency range, capturing Ch_3 (red dashed) and Ch_4 (blue dashed)

$$H_{m1}(w) = \sqrt{\kappa_{\mathrm{nf}}} \cdot H_{d,m1}(w) \tag{7}$$

$$H_{m2}(w) = \sqrt{\kappa_{\mathrm{nf}}} \cdot \left(H_{t,m1}(w) \cdot H_{d,m2}(w)\right). \tag{8}$$

D. LO-BPF and Image Rejection

The automatically tunable LO-BPF is comprised of an MZI-ring paired with a directional coupler. This MZI-ring BPF is designed with an FSR of 50 GHz. The bandpass response is achieved by connecting the drop port of the MZI-ring to a monitoring coupler with a coefficient of κ_{lom}, which has been designed and calibrated to provide 50% coupling ratio to the next MZI coupler. This response is then routed to an MZI coupler (κ_{lo2}) that has been calibrated to provide a 90% coupling ratio to the main path at Point C and 5% to a local monitor. The LO-BPF transfer function is represented by $[H_3(w)]$. The simulation is shown in Fig. 7(f), where the filter is placed at Ch_1 as shown in red and the filter monitoring response is shown in red. Then, the filter is tuned to Ch_4. Both the LO-BPF and its monitoring display bandpass response, and thus, adjusting the monitoring can automatically adjust the LO-BPF. The resonance frequency and rejection levels of the ring resonators are adjusted by $N+$ resistive heaters utilizing the thermo-optic effect [11]. The drop port of the coupler is complemented with a local PD monitor, which identifies the pole/zero location of the ring and the associated couplers, facilitating automatic control of ring and monitor coupling ratio (κ_{LO} and κ_{lom}), resonance frequency (ϕ_{LO}), and path coupler (κ_{lo2}) [6].

E. RF-Photonics Downconverter

In the realm of RF-photonic systems, two fundamental techniques for signal detection and processing exist: direct detection and coherent detection. Direct detection involves the transformation of a broadband RF signal into an optically modulated format, followed by optical filtering and subsequent direct reversion to an RF signal using an optical receiver, as shown in [13]. Despite its apparent simplicity, direct detection poses certain limitations, notably requiring the use of broadband detectors and amplifiers to accommodate the filtered narrowband signals. This translates into system complexity, higher cost, and increased power consumption, often leading to excessive heat generation. In contrast, coherent detection offers a more efficient and cost-effective approach. By downconverting high-frequency mm-wave input to a lower IF output through the mixing of an optically filtered signal with a photonic LO signal, coherent detection simplifies detector requirements, eliminates the need for RF mixers, and results in a more streamlined and power-efficient system. While certain challenges and complexities persist, recent research endeavors, such as [14] and [15], have strived to overcome these obstacles and further enhance the feasibility of coherent detection within RF-photonic systems. The proposed receiver takes advantage of coherent detection feature as will be discussed in the following.

Heterodyning is done through a 50% coupler and a balanced PD where the coupler combines the top and bottom paths into two different outputs. The balanced PD, consisting of two PDs back-to-back ($\mathrm{PD}_{1,2}$), boosts the electrical IF output current I_{rf} by 3 dB over single PD at the expense of doubling the parasitic capacitance.

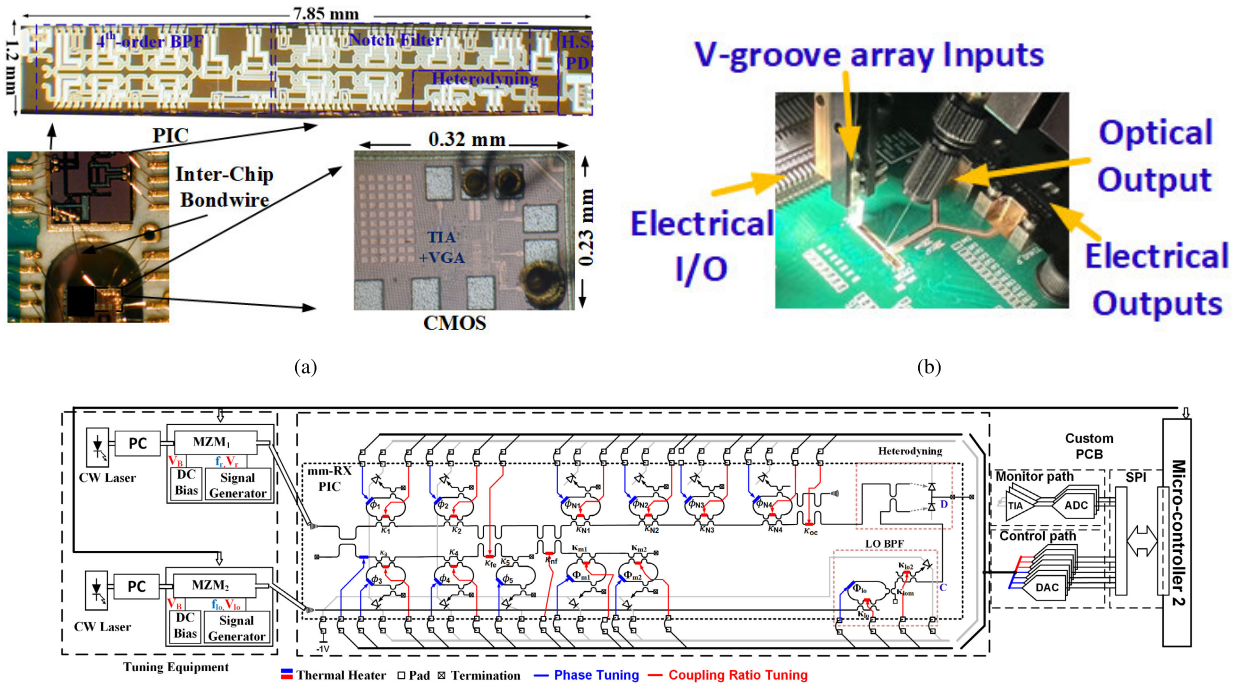


Fig. 9. (a) Two chips micrographs and their interchip bond wire, (b) photograph of the measurement setup, and (c) block diagram showing the Si-PIC mm-RX with tuning equipment.

F. CMOS Circuits

The post-amplifier CMOS stage, as depicted in Fig. 6, includes a TIA followed by a sequence of four cascaded VGA stages, culminating in a buffer. The TIA operates based on an inverter amplifier configuration. This amplifier offers switchable feedback resistances (R_{fb}), which can be selected as R_f, R_1, or R_2, to provide gain control. An auxiliary dummy amplifier stage, characterized by a dummy capacitor C_D, is also incorporated to generate a differential output voltage signal from the first stage. Directly connected to the TIA input is the balanced output from the PD. This output is maintained at a dc bias of ($V_{\text{DD}}/2$). PD configurations ensure that the anode of PD_2 remains grounded, while PD_1's cathode connects to a 2 V_{dc}.

Constructed with a current steering resistive loaded, the VGAs, driving a similar buffer, guarantee adjustable gain and a robust fan-out to the 50-Ω load. Gain control is realized by modulating tail currents, labeled as I_{PA} and I_{BUF}. This is shown in Fig. 8(a), which presents the TIA gain frequency response and is affected by bias current source (I_B) control ranging from 10 to 120 μA, and bias current (IB) is reflected to both I_{PA} and I_{BUF}. Under 1.2 V_{DD}, the gain varies between 75 and 92 dB·Ω.

Mitigating input node offsets, an offset correction circuit has been integrated, as shown in Fig. 6. An LPF (R_{LPF} and C_{LPF}) is placed in series with a differential-to-single-ended current steering operational transconductance amplifier. Fig. 8(b) shows the BW and the gain peak (G_p) versus IB adjustments. A peak gain of 92 dB·Ω achieved at 60 μA, while a peak BW of 6.3 GHz is observed at 120 μA.

Furthermore, Fig. 8(c) shows the G_{TIA} frequency response variation at different feedback resistor values (resistor code) within the TIA. At the nominal IB (10 μA), the TIA power consumption is 76.5 mW under 1.2 V_{DD}.

In summary, the CMOS stage shows a transimpedance gain of 60 dB·Ω, a versatile gain control span of 20 dB, a BW of 5 GHz, and a power consumption of 75.8 mW under 1.2 V_{DD}.

V. Fabrication and Measurement Results

The hybrid mm-wave Si-PIC/CMOS receiver (RX) was fabricated using the AMF CMC SOI Si-PIC and CMOS 28-nm processes, as illustrated in Fig. 9(a). To reduce thermal crosstalk, the chip, originally 780 μm thick, was thinned to 78 μm [16]. Given the different heights of the two chips, the CMOS chip is placed inside a cavity, and they are connected via a bond wire. The length of the bond wire was optimized to introduce minimal parasitic inductances, ensuring that they do not affect the TIA bandwidth. The PIC, developed using an SOI Si-photonics process, occupies an area of 9.42 mm^2, whereas the CMOS, designed in 28 nm, spans 0.0736 mm^2.

A. PIC Measurement

Fig. 9(b) shows the picture of optical measurement setup, showing the optical fiber vertical coupling stage and the PIC printed circuit board (PCB). Designed with two vertical grating couplers per chip, positioned orthogonally and spaced at 250 μm, the PIC is excited with optically modulated RF and LO signals via a V-groove array. After fabrication, the PIC's initial responses were found to be distorted due to process and temperature variations, necessitating an initial calibration

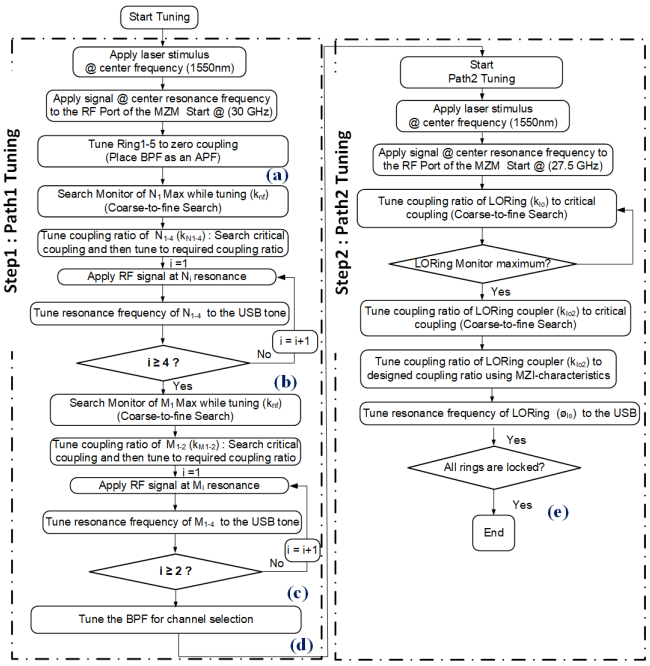


Fig. 10. Full PIC calibration algorithm.

before any measurements. The automated calibration and tuning setup for the PIC mm-RX is detailed in Fig. 9(c) and includes two mm-wave signal generators, two polarization controllers (PCs), and two external MZMs. The tuning PCB is equipped with dedicated digital-to-analog converters (DACs), TIA-VGA units (OPA2381), and ADCs (ADS8332). Thus, 13 TIA-VGA units are needed to support 13 PDs, and three eight-channel 16-bit ADCs are used. Each DAC (LTC 2668) can support up to 16 channels. In total, two DACs are utilized: for the signal path (supporting 25 microheaters) and for the LO path (supporting three heaters). The external modulation-based calibration algorithm is utilized here as in [6], through an Arduino microcontroller.

The process of calibrating the PIC's response entails an initial correction of its distorted response, utilizing the calibration algorithm depicted in Fig. 10. The PIC is tested using an optical vector network analyzer (OVA) connected between the input array with two inputs and Point C as optical output, as shown in Fig. 9. The filter is then fine-tuned to achieve the desired responses and the response is stored at different instances during the running algorithm. This is illustrated in Fig. 10, with points (a)–(e) in the flowchart. Below is a detailed walk-through of the calibration procedure.

1) Reference Baseline: The initial step prior to utilizing the calibration algorithm involves measuring the PIC's baseline response from the main path, as depicted in Fig. 11(d). For calibration, the PIC response is configured to emulate an all-pass filter (APF) (point (a) in the flowchart), providing a reference baseline. This helps in identifying the combined losses ($\mathrm{IL_{PIC}} + \mathrm{IL_{WG}} + \mathrm{IL}_F$) that can be assessed using the OVA or an optical spectrum analyzer. The same procedure can be applied to the LO path to determine discrepancies in losses due to fabrication variations and differing waveguide lengths. In addition, the initial phase of calibration extracts the relationship between the ADC output and applied power, which is described as the electrooptic effect [17].

2) Notch Filters: After the BPF is set in the APF mode, the notch filter calibration targets calibrating the resonance and coupling ratios of the four notches (point (b) in the flowchart). The tunable front-end coupler (κ_{nf}) is tuned to 0% initially. This step maximizes the signal directed toward the notch filter rejection path for the calibration to start. Calibration starts by applying a single tone at the required center frequency for N_i and utilizes the external modulator-based automatic calibration algorithm [6]. In the rejection path, notch rejection value is controlled by tuning the coupler (κ_i) for each ring and subsequently adjusting the resonance frequency for individual rings by tuning (ϕ_i). Notably, this tuning is dependent on the previous rings being set to APF. The calibrated responses of these filters are portrayed in Fig. 11(a) and (b). These filters, depending on the application requirements, can be modified for enhanced interference rejection. They can operate as first-order or second-order notch filters, efficiently rejecting numerous interfering signals with considerable attenuation.

3) Spectrum Monitoring: After the notch filter calibration ends, the monitor calibration begins, as shown in the algorithm in Fig. 10. The target is to calibrate the monitor rings coupling and resonance (point (c) in the flowchart). Conversely, the tunable front-end coupler (κ_{nf}) is recalibrated to 100%. It entails the utilization of monitoring elements ($M_{1,2}$) for spectral characteristics detection and analysis. This process commences at an OOB location, refined subsequently to inspect the operational band. Fig. 11(c) demonstrates the methodology for monitoring and dissecting these frequencies, initiating from a specific point and progressively scanning the spectrum. Furthermore, the responses from M_1 and M_2, both shown in OOB and finely tuned conditions, can be observed in Fig. 11(c). Finally, (κ_{nf}) is placed at the designed 10%.

4) Bandpass Filter: After the monitor detector calibration, the response is fine-tuned to yield two distinct BPF behaviors (point (d) in the flowchart), named as BPF and BPF_2 [Fig. 11(d)]. Fig. 11(d) illustrates the various bandwidths and shapes of the filters, highlighting the Butterworth characteristics. In contrast, Fig. 11(e) shows the elliptic response of the filter initially placed OOB and then tuned to Ch_1 and Ch_3. When compared with the simulation results in Fig. 7(a), both figures show agreement, particularly in terms of OOB, IL, and BW. Moreover, the combined signal path can be deduced through multiplication of H_1 [Fig. 11(d) and (e)] and H_2 [Fig. 11(a) and (b)]. If the notch filter is configured as a first-order filter [Fig. 11(a)], a maximum of 27.5 dB (an average of 20-dB rejection) was measured at four different interference frequencies. Furthermore, if the notch is configured as a second-order filter [Fig. 11(b)], a maximum of 45-dB rejection (an average of 35-dB rejection) is provided in channels. Thus, the overall OOB rejection can reach up to 80 dB for two blockers (45 dB from the BPF and >35 dB from a second-order notch) and 65 dB (first-order notch provides >20 dB), located at least 10 GHz from the desired signal.

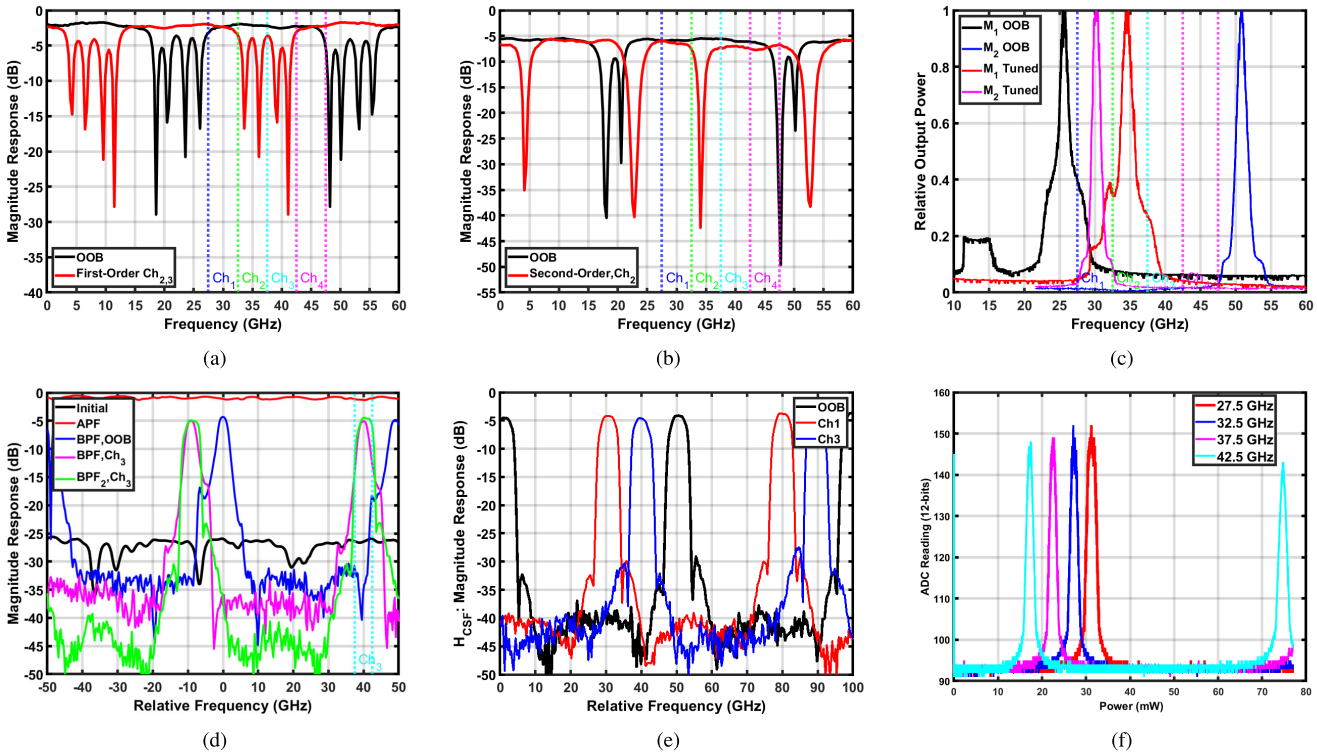


Fig. 11. Measured PIC responses. (a) First-order notch filter. (b) Second-order notch filter. (c) Response of monitoring rings. (d) Initial, APF, and BPF of the BPF filter. (e) BPF tuned to different center frequencies. (f) LO-BPF response versus ADC reading showing the peak at different RF frequencies.

5) LO-BPF: The final stage of the calibration process is to calibrate the LO-BPF and couplers (point (e) in the flowchart). The calibration starts by applying a frequency offset to the MZM_2 at the resonance frequency and tuning the ring coupler (κ_{LO}) and monitoring coupler (κ_{lo2}). Then, tune the LO-BPF resonance frequency to ϕ_{LO} to the resonance frequency. Fig. 11(f) presents the calibrated ring results across a spectrum of center frequencies. The ADC readings (12 bits) represent the response from the drop port, while the through port registers only a fraction of the total power. The power peak in the figure corresponds to the RF input signal levels during the calibration process. For calibration, multiple LO tone frequencies have been utilized, specifically 27.5, 32.5, 37.5, and 42.5 GHz, to interact with the signals at $Ch_{1,2}$, as shown in the legend of Fig. 11(f). Notably, the FSR of the LO-BPF is apparent for the 42.5-GHz tone, by applying power higher than 75 mW, which limits the maximum tuning power.

B. SDR Measurement

The PIC undergoes testing with a variety of stimuli generated either from a vector network analyzer (VNA) or a combination of an arbitrary waveform generator (AWG), upconverter, and VNA. For assessing the RF responses of the filter, the VNA provides inputs at points (a) and (b) and reads at Point D, as depicted in Fig. 12. A single DFB laser source (D2500) is connected to the erbium-doped fiber amplifier (EDFA) (KPS-BTC-13-Sd-FA keopsys), which acts as the OA. This is then linked to a power splitter (TW1550R5F1), where the laser power is divided between the two MZMs. The resulting output either interfaces directly with the VNA or undergoes downconversion for measurement on a real-time scope. Within the context of RF testing, Fig. 13(a) shows the channel-selection capability of the BPF when subjected to an input of two narrowband tones at Ch_1 (30 GHz), representing the target channel, and Ch_2 (34 GHz), representing the nontarget channel. When the channel-select filter aligns with the Ch_1 band, it selects Ch_1 with an in-band attenuation of 5 dB while concurrently rejecting Ch_2 by 35 dB. The SDR uses MZM_1, a single-drive MZM (ln05s-fc), in the mm-wave signal path. Upon receiving a 30-GHz RF input, it generates two sidebands and the carrier in the optical domain. These sidebands reside 30 GHz away from the carrier as shown by the input to PIC spectrum in Fig. 13(b) in blue. The optical signal is fed into the BPF that rejects the image at 30-GHz offset to the left of the carrier. The optical input and filtered output signal as a result of the image rejection are depicted in Fig. 13(b), illustrating the selection of the USB and attenuation of other components. The filter effectively rejects the lower sideband to the noise floor level of the optical spectrum analyzer (−38 dBm), while the rejection performance can be further improved with a higher resolution spectrum analyzer. In addition, Fig. 13(c) demonstrates a first-order jammer rejection filter performance, where two tones at Ch_2 (32.7 GHz) and Ch_3 (37.1 GHz) are simultaneously rejected by the notch filter with a minimum of 27-dB attenuation. These signals are applied to the MZM RF input, selected by the jammer reject filter (with a limited loss of L_2) and then subjected to jammer rejection filtering at the designated frequencies. Ultimately, the PIC produces an interference-free signal to the heterodyning coupler and the PDs.

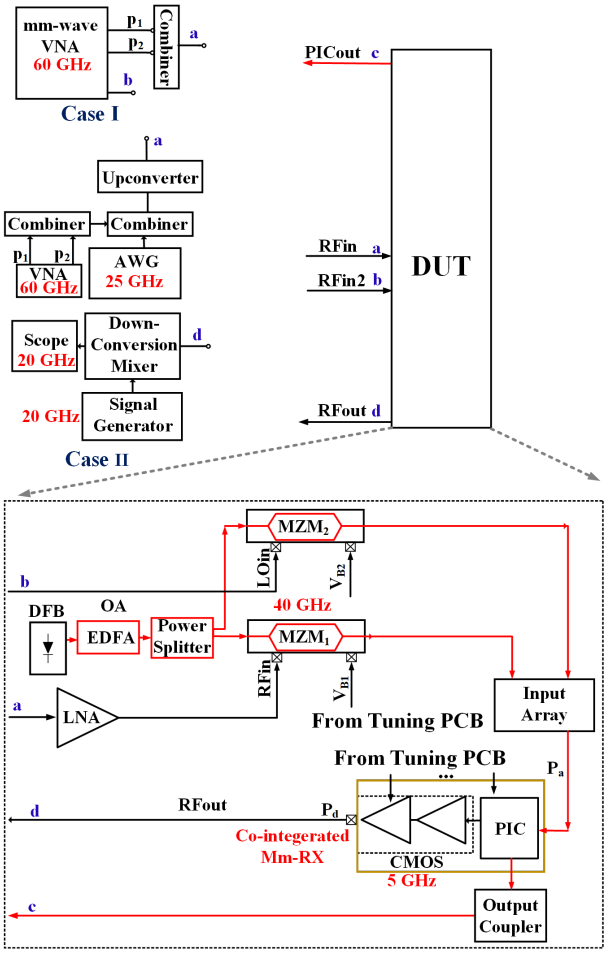


Fig. 12. Automatically controlled mm-wave measurement setups for the SDR.

For the RF performance evaluation, the PIC is configured in an APF mode. Inputs are directed to $MZM_{1,2}$ mm-wave ports, while the buffer output is bond-wired to a transmission line terminating in an SMA. Incorporating both a pre-amplifier (83051A) and a post-amplifier (ZX60-6013E) as LNAs and baseband amplifiers, this setup enhances the NF and overall gain. Fig. 13(d) displays the measured link CG and NF, highlighting a peak CG (CG_{max}) of 25 dB and a minimum NF (NF_{min}) of 9.9 dB. The overall NF and CG deteriorate with frequency because of the BW limitations of the PD/TIA. The observed peaking lies in 2.5 GHz in the CG can be attributed to the bond wire inductance. The measured channel BW of the overall SDR is 5.2 GHz. The TIA operates at a supply voltage of 1.2 V_{DD}, and its gain is set to the maximum available level. Fig. 13(e) provides an insight into the measured linearity metrics against input power, depicting fundamental output power, IM_3, output noise level (NLO), and noise density. The link attains an IIP_3 of 0 dBm, $P_{1\,dB}$ of −9.5 dBm, and an SFDR of 50 dB at an IF frequency of 2.5 GHz. The measured noise density using the VNA is at −165 dBm/Hz. The effect of the blocker on the linearity of the system is shown in Fig. 13(f), where the B1dB reaches a minimum number −7 dBm at small offset and reaches up to 16 dB at higher offsets. Moreover, the blocker NF is also shown in Fig. 13(f), where the NF increases by 6 dB with −50-dBm blocker at 100-MHz offset and increases by 3 dB at 1-GHz offset.

To assess the performance of the modulated signal, an AWG producing a 64-QAM signal, which is then combined with two interferers, is linked to point a through an upconverter, as shown in Fig. 12. Point b, on the other hand, receives a continuous-wave (CW) signal from the VNA. At Point D, a downconverter is connected, receiving its input from the signal generator, with the final output being channeled to a real-time scope. The measured constellations from a blocker test with and without notch filtering are presented in Fig. 14. Si-PIC is supplied with a 100-MSymbol/s 64-QAM signal at −25 dBm and two mm-wave blockers at −10 dBm. The modulated signal carrier frequency is 30 GHz, while blocker frequencies are 35 and 40 GHz and the IM3 term of the two blockers due to the third-order nonlinearity of the SDR directly falls into the desired band and distorts the constellation. Fig. 14 confirms that the received signal without filtering cannot be reconstructed due to the large in-band IM_3 term. Then, automatic detection of these two blockers starts and the location information is provided to notch filters N_{1-4} through spectrum sensing ring resonators M_1 and M_2. The notch filter is then reconfigured into a second-order notch filter, resulting in two notches for each interferer frequency. Then, N_1 and N_2 are centered at 35 GHz to reject the first interferer, and (N_3/N_4) combination is centered at 40 GHz for the second interferer. Therefore, the demodulated signal has improved constellation as shown in Fig. 14 and EVM has improved from −23.5 to −30.0 dB.

VI. Discussion

Table III provides a detailed performance summary of the presented integrated SiPh SDR and contrasts it with other state-of-the-art designs. These include the time-approximation filter [18], the N-path filters from RFIC 2021 [19] and RFIC 2020 [20], as well as the six-port discriminator microwave IC presented in [21]. In our approach, we harness the potential of the PIC to facilitate blocker rejection using a fourth-order BPF and notch filters. Our design operates in the 30–45-GHz mm-wave band, surpassing the frequency range of all referenced works. In addition, it supports a versatile bandwidth range of 3–5 GHz, which is broader than the best-reported bandwidth of 4 GHz from [21]. For narrowband interferers, the blocker rejection value reaches up to 80 and 60 dB for quad interferers. These metrics are superior to alternatives, such as the 45-dB value reported in [18]. With an RF gain of 25 dB, our design exceeds the performance of the best previous work in [19]. In comparison, our work provides a minimum NF that stands at 9.9 dB, which is lower than most of the prior SDR receivers [19]. The IIP_3 is set at 3.1 dBm, primarily limited by the LNA, which is sufficient for SDR receivers and is competitive compared to counterparts. Meanwhile, $P_{1\,dB}$ measures at −6.4 dBm, and the SFDR is at 50 dB, emphasizing the design's suitability for SDR applications. Finally, the total chip area for this work is 9.42 mm^2. Moreover, in this research, a high linearity LNA is considered, which can be designed for integration in the CMOS process along the lines of the approach proposed in [22]. Although the MZM and

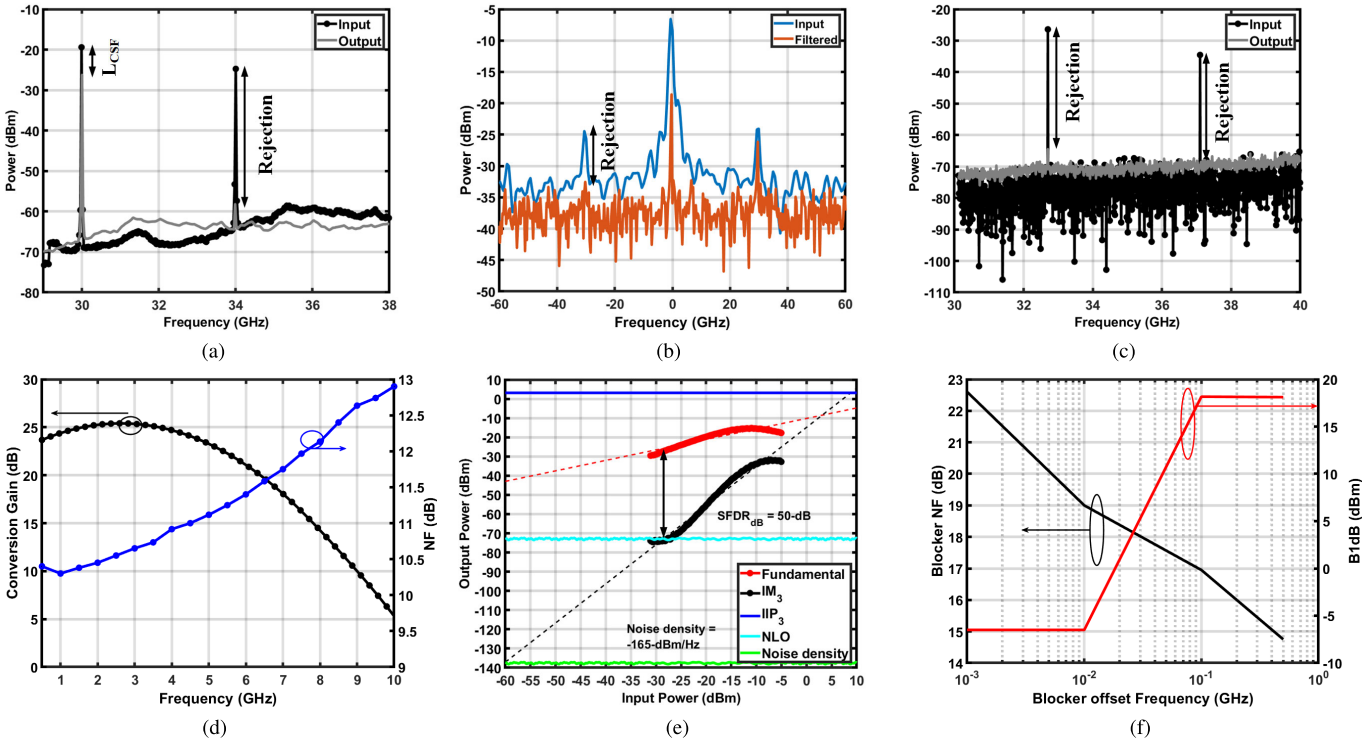


Fig. 13. Measured RF responses of the SDR receiver. (a) BPF response to two input tones at desired and undesired bands. (b) Image-rejection performance to select the USB at the desired band. (c) Jammer rejection performance rejecting two interferers. (d) CG and NF versus frequency. (e) Linearity metrics versus input power at 2.5 GHz. (f) Blocker1dB (B1dB) and NF at different blocker offset frequencies.

TABLE III

PERFORMANCE SUMMARY OF THE PRESENTED HYBRID-INTEGRATED SDR AND COMPARISON WITH THE STATE-OF-THE-ART

	This Work	**RFIC 2022 [18]**	**RFIC 2021 [19]**	**RFIC 2020 [20]**	**TMTT 2005 [21]**
Blocker Rejection Technique	PIC BPF and Notch Filter	Time-Approximation Filter	N-Path Filter	N-Path Filter	NA
Frequency Range (GHz)	30 $\sim$ 45	31 $\sim$ 37	6 $\sim$ 31	10 $\sim$ 35	24-30
Signal Bandwidth (MHz)	3000 $\sim$ 5000	550 $\sim$ 660	320 $\sim$ 470	400	< 4 GHz
OOB Blocker Rejection (dB)	First-Order: 65 Second-Order: 80	45	25	9	NA
RF Gain (dB)	25	4 $\sim$ 6	-6.6 $\sim$ -4.5	11 $\sim$ 15	8
NF (dB)	9.9 $\sim$ 12.9	12 $\sim$ 17	5 $\sim$ 20	12.5 $\sim$ 15.7	NA
IIP$_3$ (dBm)	3.1	NA	1.4 $\sim$ 6.3	+10 $\sim$ +14.1	NA
P$_{1dB}$ (dBm)	-6.4	-6	-7.4 $\sim$ -2	-2.5 $\sim$ 0	NA
SFDR (dB)	50	NA	NA	NA	NA
Total Chip Areas (mm^2)	9.42	0.46	0.69	NA	NA
Technologies	SOI PIC and 28nm CMOS	28nm CMOS	45nm SOI	28nm CMOS	microwave IC[1]
External Components	MZM$_{1,2}$, LNA and Post-Amplifier	—	—	—	NA
Power Dissipation (mW)	900	67	320	22.8	NA
B1dB (dBm)	16 @ 0.1 GHz	-5.8 3.8	-2	1.5	NA
BlockerNF (dB)	14 @ 1GHz	NA	NA	NA	NA

[1] The specific technology to implement this microwave IC wasn't specified

the LNA are not integrated in the current work, the estimated area overhead would be approximately 3.2 mm^2 in case they will be integrated in the future according to [22] and [23]. The total system could be integrated yielding an overall size of 22.5 mm^2. In this research, thermoelectric cooler (TEC) under thinned SiPh chip is utilized to significantly reduce the excessive calibration time due to thermal crosstalk [10] while consuming a high power, yielding an overall system power of 900 mW. The expansive chip area underscores the inherent tradeoffs in SDR designs, particularly when leveraging hybrid integration to boost photonic performance. While this approach can significantly elevate performance metrics, it simultaneously inflates the chip footprint, leading to increased fabrication costs and potential surges in power

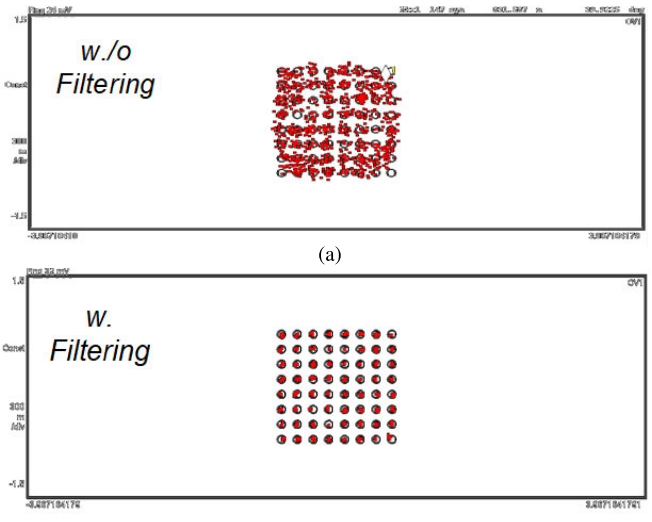


Fig. 14. Modulation measurement (a) w./o and (b) w./ interference filtering.

consumption. Striking the right balance among these factors is vital, as different applications may prioritize one over the other. Moreover, this work introduces a comprehensive PIC filter structure that efficiently addresses the challenges often associated with implementing higher order analog IIR filters on CMOS chips. The design uniquely supports automatic calibration of center frequency, bandwidth, and off-band rejection, surpassing capabilities in prior works [18], [19], [20], [21]. In addition, RF downconversion is demonstrated, with the balanced PD current being amplified and detected.

VII. Conclusion

In summary, this article presents a 30–45-GHz CMOS/Si-PIC hybrid-integrated SDR. Channel selection is demonstrated across four different bands and OOB interferences are effectively rejected. Moreover, this work demonstrates an automatically calibrated, programmable receiver with OOB blocker rejection capability. The analysis of the hybrid-integrated SDR receiver link and optimization is provided to study the effects of different parameters. Future works should consider the integration of the two MZMs within the PIC and the LNA within the CMOS chip. In conclusion, our work provides high-performance SDR utilizing photonic filters. However, balancing hybrid integration benefits against the tradeoffs in chip size and power consumption to optimize SDR receivers.

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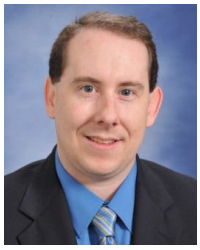

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