A 16-32GHz RF Silicon Photonic Receiver with 22nm FD-SOI CMOS Driver

Yu-Lun Luo, Dharma Paladugu, Ramy Rady, Kamran Entesari, Samuel Palermo

Department of Electrical and Computer Engineering, Texas A&M University, USA
royulun@tamu.edu

***Abstract*—This paper presents an integrated radio-over-fiber (RoF) link including a CMOS driver and a silicon photonic Mach-Zehnder Modulator (MZM). The RoF link covers an operating bandwidth of 16-32 GHz by co-designing the output matching networks with the bond wire and MZM.**

Keywords—CMOS, *Low Noise Amplifier, Microwave photonics, Mach-Zehnder modulator, Driver, Radio over fiber, Silicon photonics*

I. Introduction

Radio-over-fiber (RoF) is a technology that combines the benefits of radio frequency (RF) transmission with the advantages of optical fiber communication. In a RoF system, the received wireless signal is modulated onto an optical carrier wave and distributed through optical fiber networks. The low-loss characteristics of the fiber enable the deployment of the baseband processing far away from the remote antenna units (RAUs) [1]. This reduces system complexity and has the potential to improve wireless signal coverage. Therefore, this technique holds promise for future handsets and indoor communications.

CMOS chip and silicon photonic chip offer advantages for building the RoF link, such as low cost and the possibility of integration into a single chip. However, advanced CMOS processes may face challenges in low supply voltage operation, while silicon MZMs may exhibit higher loss or $V\pi$ compared to those in other processes. An example of the RoF system is shown in Fig. 1. To improve the minimum detectable signal and meet signal-to-ratio (SNR) requirement, electrical driver is necessary. It amplifies the weak signal from antenna and delivers linear voltage swing to modulate the MZM.

In this work, we report the first integrated RoF link that includes both a CMOS MZM and a silicon MZM. The RoF link operates over a frequency range of 16-32GHz. The overall system demonstrates a peak gain of 5 dB and an IIP3 performance of -1.6 dBm. The power consumption of the electrical driver is 209mW.

II. SILICON PHOTONIC MZM DESIGN

Silicon MZM is promising for implementing CMOS monolithic integration [4]. In this paper, we present a differential traveling-wave MZM. Driving MZM differentially offers advantages such as higher efficiency and elimination of second-order nonlinearity.

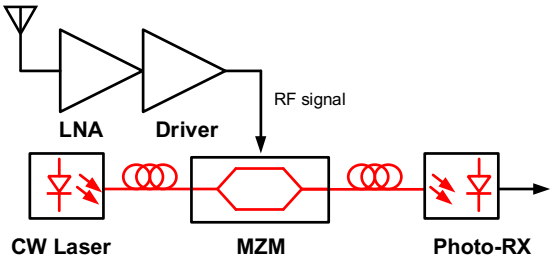

Fig. 1. RoF system.

Designing the doping of the PN junction on the MZM involves a trade-off between loading parasitic capacitance and amount of phase shifting. It is essential to match the RF index of the transmission line with the optical velocity in the waveguide. In our work, the transmission line electrode is designed to be 50Ω. An on-chip resistance is used as the termination. The width and clearance to the ground of the transmission is designed to be 36um and 33um, respectively. The spacing between two differential lines is 200um. The length of MZM is 2mm, enabling operation up to 25GHz. The default reversed-bias voltage is 2V sourced from CMOS chip. The micrograph of the photonic chip is shown in Fig. 2.

III. Electrical Driver Design

Fig. 2 illustrates the block diagram and the schematic of proposed differential MZM driver. The MZM driver is fabricated using CMOS 22nm FD-SOI technology. To suppress the overall noise of the system, we adopt a low-noise amplifier (LNA) as the first stage. For input matching, we apply the conventional inductive source-degeneration technique. Next, a balun is utilized to convert the single-ended signal to a differential signal and provide interstage matching between the pre-driver and LNA. The pre-driver is a two-stack-FET structure designed to provide gain for the overall system. The driver stage is a three-stack-FET structure that further increases the headroom of the supply voltage and is designed to deliver a large voltage swing to modulate the MZM. The output matching network performs optimal impedance matching for the driver. The magnetically coupled resonator (MCR) technique is applied to all interstage and output matching networks. In this frequency range, minimizing the inductance of the bond wire is crucial. To achieve this, we position the two chips as close as possible. The inductance of the bond wire is simulated to be 150 pH using electromagnetic (EM) simulation. Additionally, the interface is

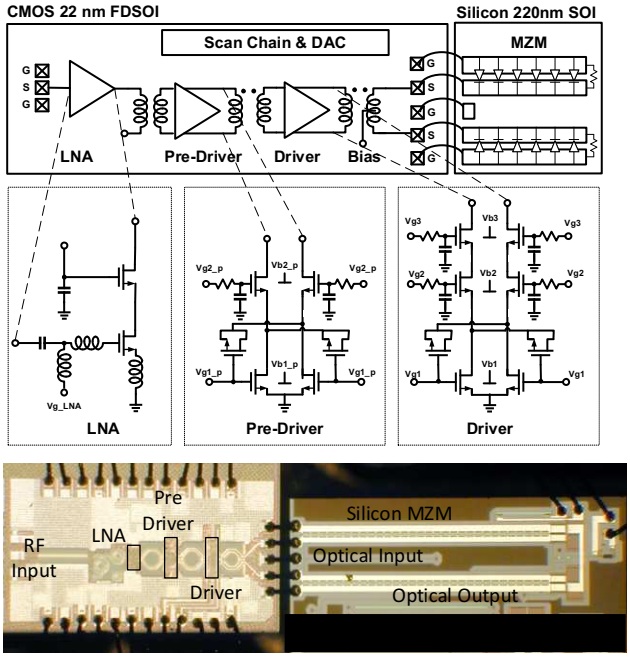

Fig. 2 Schematic of the proposed RoF link and micrograph.

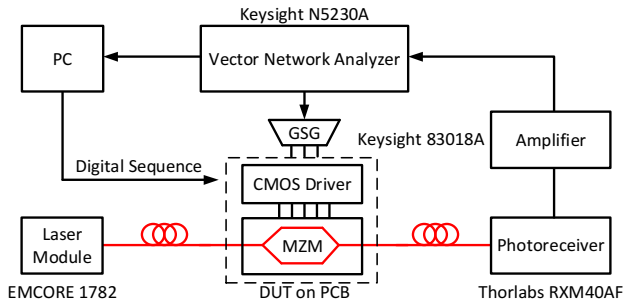

Fig.3 Measurement setup.

designed in a GSGSG configuration to aid the RF signal transition.

IV. Measurement Results

Fig. 3 illustrate the measurement setup. Two chips are mounted on the FR-4 PCB. The tuning voltages for the CMOS chip and the heater for the photonic chip are supplied externally through the PCB. The bias voltages are generated from an internal digital-to-analog controlled by the scan chain. The input signal is applied via GSG probe, and then the output of the driver connects to the input of the MZM through bond wires in GSGSG configuration. The continuous-wave laser source (EMCORE 1782) is coupled to MZM via grating coupler. To compensate for the optical power loss of the grating coupler at both the input and output, higher power is required. The modulated optical signal is then connected to a photoreceiver module (Thorlabs RXM40AF) and an amplifier (Keysight 83018A). Overall performance is characterized by the S-parameters and IIP3 using vector network analyzer (Keysight N5230A).

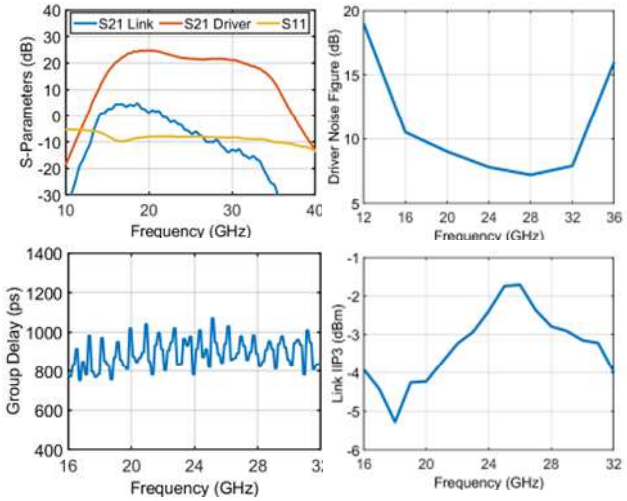

Fig.4 Measured S-parameters of link and driver, NF of the driver, group delay and IIP3 of the link.

Fig. 4 displays the S-parameters, IIP3, group delay, and noise figure of the driver alone (on-wafer probing) and the RoF link. The S21 bandwidth of the driver covers 16-32 GHz, and the noise figure ranges from 7-10dB. The S11 is lower than -8 dB within the bandwidth. The overall link is measured to have 5 dB peak gain, -1.6 dBm IIP3, and less than 400ps group delay variation. The power consumption of the electrical driver is 209mW. The roll-off in the frequency response may be caused by the uncertainty of the process variation [5]. Additionally, the gain of the link is limited by the optical loss of the grating coupler.

V. Conclusion

This paper demonstrates the integration of a CMOS driver and a silicon MZM. The stack-FET structure helps overcome the drawback of low supply voltage operation in CMOS processes. Additionally, the MCR technique is utilized to co-design the input impedance of the MZM and the connection with the bond wire.

Acknowledgment

This work was supported by the National Science Foundation under Grants ECCS-1807281 and ECCS-1824341.

References

[1] L. Pereira, et al., “Implementation of a multiband 5G NR fiber-wireless system using analog radio over fiber technology,” Optics Communications, vol. 474, p. 126112, 2020.

[2] Z. Zong et al., "A 28GHz Two-Way Current Combining Stacked-FET Power Amplifier in 22nm FD-SOI," 2020 IEEE Custom Integrated Circuits Conference, pp. 1-4, 2020,

[3] Y. Luo, et al., "A Power-Efficient 20–35-GHz MZM Driver With Programmable Linearizer for Analog Photonic Links in 28-nm CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 71, no. 3, pp. 1262-1273, 2023

[4] R. Ding, et al., “Design and characterization of a 30-GHz bandwidth low-power silicon traveling-wave modulator”, Optics Communications, Vol 321, p. 124-133, 2014.

[5] N. Hosseinzadeh, et al., "A 0.5-20 GHz RF Silicon Photonic Receiver with 120 dB•Hz2/3 SFDR using Broadband Distributed IM3 Injection Linearization," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2019, pp. 99-102