# A mm-wave CMOS/Si-Photonics Hybrid-Integrated Software-Defined Radio Receiver Achieving > 80-dB Blocker Rejection of < -10 dBm In-Band Blockers

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***Abstract* — This paper presents a hybrid-integrated mm-wave software-defined radio (SDR) receiver front-end implemented with silicon photonics and CMOS chips. The proposed SDR leverages a programmable silicon photonics IC (PIC) with high-Q filters to perform re-configurable channel-selection/image-rejection and jammer-rejection with tunable center frequency of 30-45 GHz, and 3-5 GHz bandwidth. Up to four out-of-band blockers are automatically detected and rejected simultaneously. Also, the desired mm-wave signal is mixed with a tunable local oscillator (LO) carrier and down-converted to a 2.5-GHz IF center frequency. Subsequently, the CMOS IC converts the current signal into an amplified voltage signal, thus compensating for PIC losses. The PIC is fabricated using a silicon-over-insulator (SOI) process, and the CMOS is fabricated using 28nm process. The receiver achieves > 80-dB rejection for two blockers and > 65-dB rejection for four blockers. The EVM measures -30-dB using a 100-MSymbol/s 64-QAM signal at the presence of a 10-dBc out-of-band blocker.**

***Keywords* — Millimeter-Wave radio receivers, programmable silicon photonics filters, software-defined-radio, RFICs.**

## I. Introduction

Next-Generation wireless communication systems demand mm-wave wideband receivers to meet the growing wireless access and the required data throughput. A major challenge for these receivers is to maintain a high tolerance for both in-band and out-of-band (OOB) blockers. This motivates employing a re-configurable software-defined radio (SDR) receiver that aggregates multiple contiguous frequency bands while sufficiently tolerating in-band and filtering OOB blockers, thus providing multi-channel wideband operation. Traditional electronic SDRs face significant challenges at mm-wave frequencies due to lack of programmable electronic filters and the limited quality factor of passives on silicon substrate which makes it hard to implement high-order filtering. There has been increasing interest in mixer-first receiver architectures for addressing in-band blockers such as ([1], [2], [3]) but achieving high OOB blocker rejection and high spurious free dynamic range (SFDR) simultaneously, is still a challenge. This limits their maximum instantaneous BW, especially for mm-wave operation. Recently, there has been a growing interest in other technologies to realize SDR such as photonic-based multi-band transceiver [4], but it is a complex and bulky implementation. RF Silicon photonics technology can realize integrated band-pass and notch filters to perform channel-selection and interference cancellation at mm-wave frequencies [5], and has the potential to assist CMOS amplifying stages in the receiver by providing the necessary filtering solutions for OOB blockers.

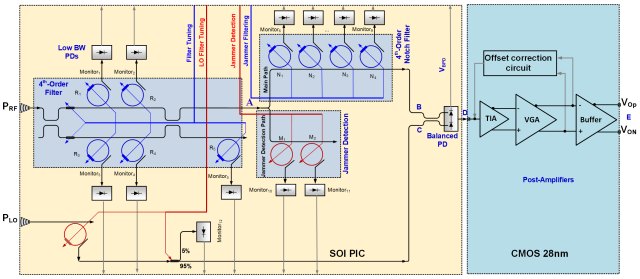



Fig. 1. The proposed photonically-assisted hybrid SDR architecture.

This work presents a photonically-assisted SDR receiver featuring high-Q factor silicon photonics filters that are highly programmable and capable of rejecting strong OOB blockers and a CMOS post-amplifying stage. A proof-of-concept receiver prototype in SOI Photonics and 28nm CMOS process demonstrates the reconfigurability to cover multiple operating bands within 30-45 GHz frequency range and > 35-dB interference rejection using the channel-select band-pass filter (BPF) at adjacent and alternate channels, and an overall rejection > 80-dB using both bandpass and notch filters.

## II. Proposed Photonically-Assisted SDR

Fig. 1 illustrates the proposed photonically-assisted hybrid SDR consisting of a PIC and CMOS amplifiers. Two input grating couplers are available to the PIC for optically-modulated mm-wave signal, $P_{RF}$, and mm-wave LO, $P_{LO}$, respectively. The top path consists of a tunable wideband BPF for channel-selection/image-rejection and jammer-rejection and a tunable notch filter with spectrum monitoring and jammer rejection capabilities. The bottom path comprises of LO image-reject filter. Both of these paths are combined through a directional coupler and fed into a balanced PD. The output current signal by the PD is centered at the frequency difference between the two paths $f_{IF} = f_{RF} - f_{LO}$ which enters the CMOS unit. The CMOS unit provides signal conditioning by three amplifying stages and an offset correction circuit. The trans-impedance amplifier (TIA) converts the current signal into a differential amplified voltage signal, then the variable gain amplifier (VGA) provides more tunable gain and the buffer provides an output to drive

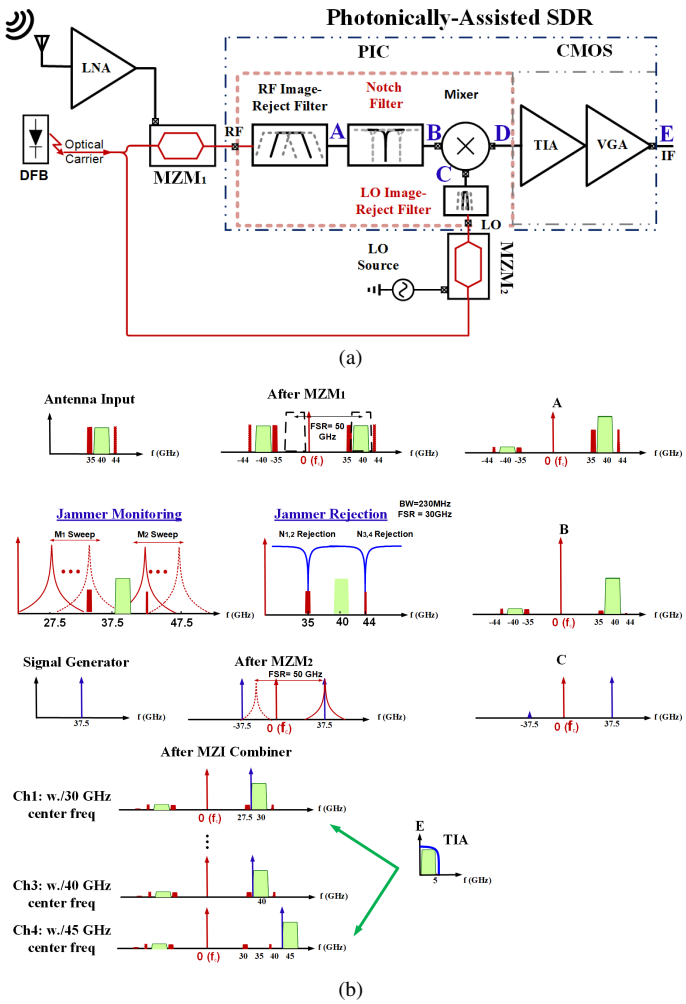



Fig. 3. (a) The full receiver system of the proposed photonically-assisted SDR architecture, and (b) frequency planning of the SDR.

50-Ω load. An analog control signal re-programs PIC filter responses, while a local monitor PD for each ring returns a signal to indicate pole/zero locations. Moreover, the monitor path signal is able to locate the interferes.

Fig. 3a shows the full SDR receiver system including photonically-assisted SDR, two external Mach-Zehnder Modulators ($MZM_{1,2}$) and low noise amplifier (LNA). Tunable RF image-rejection filter, notch filter, LO image-rejection filter, and mixer are all encompassed in the PIC part and gain stages are built into the CMOS unit of the proposed photonically-assisted SDR. The system is driven by two inputs; a mm-wave received signal by the antenna is amplified by the LNA to optimally drive $MZM_1$ and improve the overall system gain, SFDR and reduce the overall NF. Then, $MZM_1$ converts it to optical domain going to $P_{RF}$ input, also $MZM_2$ converts the LO tone into optical domain coupled to $P_{LO}$ port. A frequency plan for the proposed photonically-assisted SDR receiver system is shown in Fig. 3b. The desired mm-wave signal (27.5-32.5,...,42.5-47.5 GHz) and OOB blockers both are received through the antenna. $MZM_1$ is biased at Q-point for maximum linearity while modulating the light input from a distributed feedback laser (DFB) at 1550-nm. The BPF is configured for one of the channels and its corresponding BW, and thus image-rejection and partial inference rejection of > 35-dB is performed at point A. Two ring monitors detect the location of two interferers and automatically configure the notch filters to their proper locations. The notch filter provides an extra 30-dB rejection to interference frequencies at Point B. The LO signal (27.5,...,42.5 GHz) drives $MZM_2$ and the LO image-reject filter selects the upper side-band of the modulated signal, thus rejecting LO image at point C. The mixer combines both signals at each of the four channels and its corresponding LO to provide a 2.5-GHz output from the PIC at point D. Finally, the CMOS amplifies these signal to drive the loading instrument at point E.

## III. Circuit Implementation

### A. Silicon Photonics Circuits

Fig. 2 illustrates the circuit schematic of the photonically-assisted SDR. The RF photonics $4^{th}$-order BPF ($Ring_{1-5}$) is designed similar to [5] to provide a band-pass response with a free spectral range (FSR) of 50-GHz, a re-configurable 3∼5-GHz BW, and center frequency to cover 30∼45 GHz range at point A. The simulated filter response in MATLAB shows an insertion loss of -4.8-dB and an OOB rejection > 35-dB (≈ 40-dB at 12.7 GHz offset from center), which agrees with the measurement results of Fig. 5a. The notch filter starts with a tunable coupler which divides the signal between main and monitor paths by 90% coupling ratio to the main path. The main path consists of four rings

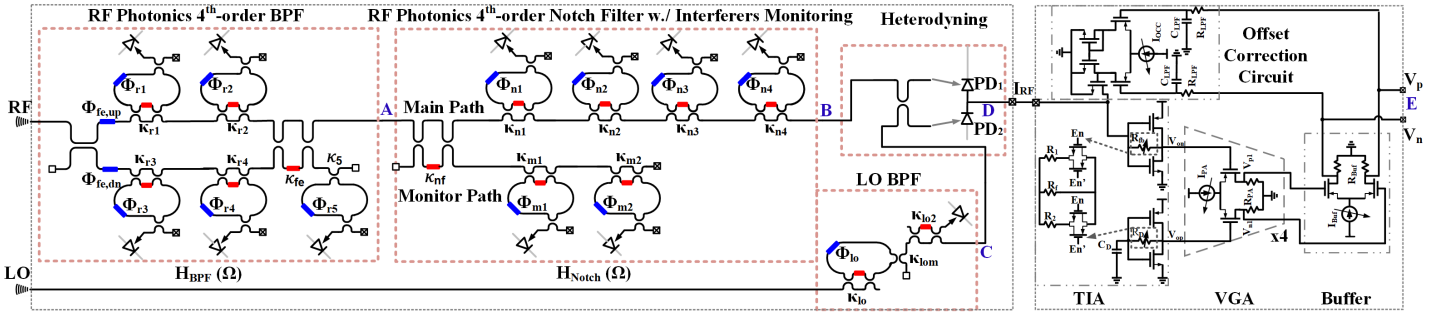



Fig. 2. The circuit implementation of the photonically-assisted SDR.

acting as four notch filters ($N_{1-4}$), while the monitor path consists of two rings ($M_{1-2}$) acting as BPF from input to each local monitor. The unit element of the notch filter is a ring resonator with FSR of 30-GHz, two heaters to control resonance frequency and coupling ratio which determine the order of the filter and the level of rejection, respectively. For the interferer monitoring rings, two rings are chosen to divide the search range evenly and thus reduce the sweeping time required by half. Each monitor ring provides a peak at the location of any interferers in its search range, which is used to tune the notch filter resonance frequency. The LO BPF comprises of a ring resonator with FSR of 50-GHz with output from the band-pass response going to an MZI coupler tuned to provide 90% coupling ratio to the main path at point C and 10% to a local monitor. The resonance frequency and rejection level of all the ring resonators are controlled by $N$+ resistive heaters using the thermo-optic effect, where applying a DC voltage/current shifts the pole/zero magnitude level and frequency location. A local PD monitor is used with each ring to indicate the location of the pole/zero of each ring, which can be automatically-controlled by an external controller [6]. Heterodyning is done through a 50% coupler and a balanced PD where the coupler combines the top and bottom paths into two different outputs. The balanced PD, consisting of two PDs back-to-back ($PD_{1,2}$), boosts the electrical IF output current $I_{RF}$ by 3 dB over single PD at the expense of doubling the parasitic capacitance.

The CMOS TIA is an inverter amplifier with three switchable feedback resistances $R_{fb}$ (as either $R_f$,$R_1$, or $R_2$) for gain control and a dummy amplifier stage with dummy capacitor $C_D$. The balanced PD output is directly connected to the TIA input so it is dc-biased at $V_{DD}/2$. The anode of $PD_2$ is connected to ground, and the cathode of $PD_1$ is connected to 2-$V_{DC}$. Four cascaded VGA amplifiers as current steering resistive-loaded stages and a current steering resistive-loaded buffer are used to provide a tunable gain and sufficient fan-out to the load impedance of 50-Ω. Also, VGA and buffer gain control is provided through the tail current ($I_{PA}$ and $I_{BUF}$, respectively) control. The offset correction circuit of $C_{LPF}$ $R_{LPF}$ low pass filter and differential to single ended current steering operational trans-impedance amplifier is used to compensate for offset at the input node. The full CMOS stage provides a gain of 60-dBΩ with 20-dB gain control and 3-dB BW of 5-GHz, while consuming 18∼75.6 mW from 0.7∼1.2 $V_{DD}$.

## IV. Measurement Results

The micro-graph of the hybrid-integrated SDR receiver prototype is shown in Fig. 4. Since the PIC is thinned to 75-$\mu$m to reduce thermal coupling [6], the PIC and CMOS chips do not have similar heights, hence; the CMOS chip is placed inside a cavity and the two chips are directly connected through a bond-wire. The PIC is fabricated in SOI Si-photonics process occupying an area of 9.42 mm$^2$, while the CMOS is fabricated in 28nm occupying an area of 0.0736 mm$^2$. The PIC response is measured by optical vector analyzer (OVA)

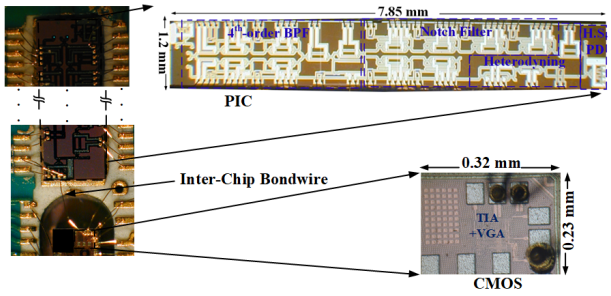



Fig. 4. The two chips micro-graphs and their inter-chip bondwire.

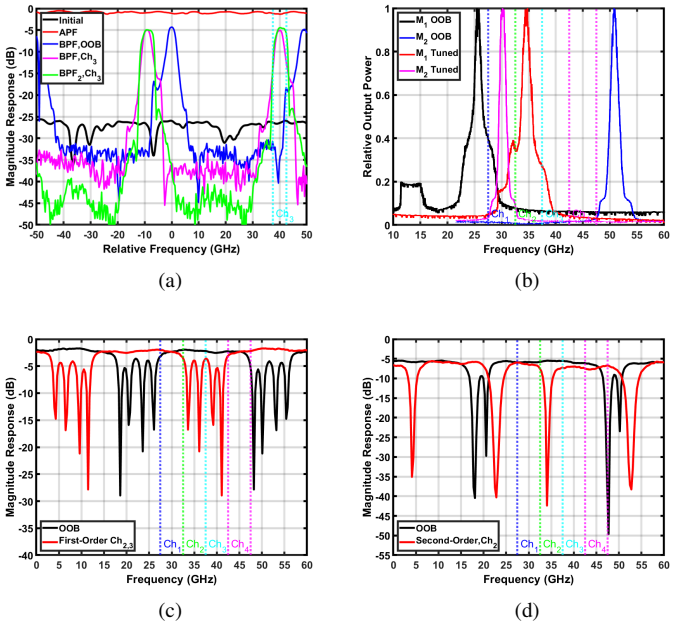


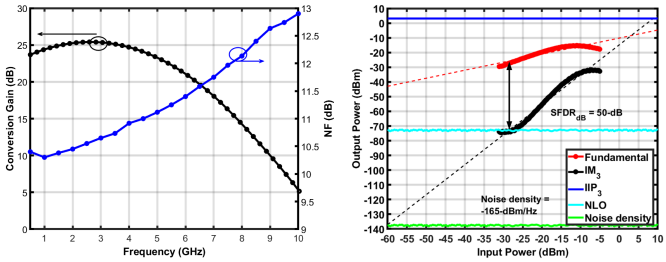

Fig. 5. Measured PIC optical response at different programming options; (a) initial, APF and BPF at different center frequencies and BWs, (b) spectrum monitoring, (c) first-order notch filter, and (d) second-order notch filter.

and the initial response is shown in Fig. 5a, which is then automatically calibrated to display an all-pass filter (APF) and two different BPF responses with either $BPF_1$ (placed at OOB or at $Ch_3$) and -3dB-BW of 3-GHz or $BPF_2$ at $Ch_3$ and -3dB-BW of 5-GHz. The spectrum monitoring is done through $M_{1-2}$ and the spectrum for detecting two interferers is shown in Fig. 5b, where the monitor is first placed at the location of OOB and then tuned to search for the band of operation. The first-order notch filter demonstrates quadruple interferer rejection capability with maximum of 30-dB as shown in Fig. 5c, which is shown for OOB and then tuned in a way that two notches are located in $Ch_2$ and the other two are located in $Ch_3$ (i.e. dual-band). Furthermore, the notch filter is tuned as a second-order filter to show up to two interferers rejection with > 45-dB initially at OOB and then at $Ch_2$ as shown in Fig. 5d. The full top path response is then a combination of Fig. 5a and Fig. 5d that shows a maximum rejection of > 80-dB (> 35-dB from BPF and 45-dB from notch filter).

For measuring the RF performance, the PIC is placed

Table 1. Performance summary of the presented hybrid-integrated SDR and comparison with the state-of-the-art.

| Specification | This Work | RFIC 2022 [1] | RFIC 2021 [2] | RFIC 2020 [3] |
|---|---|---|---|---|
| **Blocker Rejection Technique** | PIC BPF and Notch Filter | Time-Approximation Filter | N-Path Filter | N-Path Filter |
| **Frequency Range (GHz)** | 30 $\sim$ 45 | 31 $\sim$ 37 | 6 $\sim$ 31 | 10 $\sim$ 35 |
| **Signal Bandwidth (MHz)** | 3000 $\sim$ 5000 | 550 $\sim$ 660 | 320 $\sim$ 470 | 400 |
| **OOB Blocker Rejection (dB)** | First-Order: 60<br>Second-Order: 80 | 45 | 25 | 9 |
| **RF Gain (dB)** | 25 | 4 $\sim$ 6 | -6.6 $\sim$ -4.5 | 11 $\sim$ 15 |
| **NF (dB)** | 9.9 $\sim$ 12.9 | 12 $\sim$ 17 | 5 $\sim$ 20 | 12.5 $\sim$ 15.7 |
| **$IIP_3$ (dBm)** | 3.1 | NA | 1.4 $\sim$ 6.3 | +10 $\sim$ +14.1 |
| **$P_{1dB}$ (dBm)** | -6.4 | -6 | -7.4 $\sim$ -2 | -2.5 $\sim$ 0 |
| **SFDR (dB)** | 50 | NA | NA | NA |
| **Total Chip Areas ($mm^2$)** | 9.42 | 0.46 | 0.69 | NA |
| **Technologies** | SOI PIC and 28nm CMOS | 28nm CMOS | 45nm SOI | 28nm CMOS |
| **External Components** | $MZM_{1,2}$, LNA and Post-Amplifier | — | — | — |




(a) (b)

Fig. 6. Measured RF responses of the SDR receiver; (a) CG and NF. vs frequency, and (b) linearity metrics vs input power at 2.5-GHz.

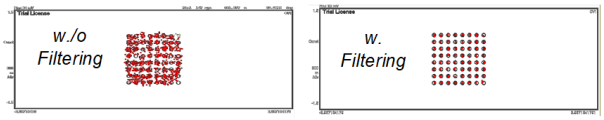



Fig. 7. Modulation measurement w./o (left) and w./ (right) interferer filtering.

in an APF mode with two inputs provided to $MZM_{1,2}$ mm-wave input ports and output from the buffer bond-wired to a transmission line terminated by SMA. Both pre-amplifier (83051A) and post-amplifier (ZX60-6013E) serve as LNAs and base-band amplifiers, improving the NF and overall gain. The measured link conversion gain (CG) and noise figure (NF) are shown in Fig. 6a, with a max. CG ($CG_{max}$) of 25-dB and a min. NF ($NF_{min}$) of 9.9-dB. Fig. 6b illustrates the measured linearity metrics vs input power, where the fundamental output power, $IM_3$, noise level at the output (NLO) and noise density are shown. The link achieves $IIP_3$ of 0-dBm, $P_{1dB}$ of -9.5-dBm and SFDR of 50-dB at IF frequency of 2.5 GHz.

The measured constellations from a blocker test with and without notch filtering is presented in Fig. 7. Si-PIC is supplied with a 100-MSymbol/s 64-QAM signal at -25 dBm and two mm-wave blockers at -10 dBm. The modulated signal carrier frequency is 30-GHz, while blocker frequencies are (35 and 40)-GHz. Fig. 7 confirms that the received signal without filtering cannot be reconstructed due to the large in-band folded blocker. Then, automatic-detection of this blocker starts and the location information is provided to the notch filter. The notch filter is then reconfigured as a second-order notch filter centered at 35-GHz. Therefore, the demodulated signal has improved constellation as shown in Fig. 7 and EVM has improved from -23.5 to -30.0-dB.

## V. Conclusion

A CMOS/Si-PIC hybrid-integrated SDR is investigated in this paper. Channel selection is demonstrated for four different bands and OOB interference is properly rejected. This work demonstrates an automatically calibrated, programmable receiver with OOB blocker rejection capability. A comparison between the presented integrated SDR receiver performance and other recent mm-wave integrated CMOS SDRs is shown in table 1. Future works should consider the integration of the two MZMs within the PIC and the LNA/post-amplifier within the CMOS chip.

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