Applied Physics Letters

RESEARCH ARTICLE | DECEMBER 11 2023

Thermal analysis of thermoelectric active cooling including external thermal resistances

Nicolas Marquez Peraca ; Qing Zhu ; Junichiro Kono ; Geoff Wehmeyer

Appl. Phys. Lett. 123, 243901 (2023)
https://doi.org/10.1063/5.0176286

CrossMark

11 December 2023 17:51:26

QBLOX
Integrates all Instrumentation + Software for Control and Readout of
Superconducting Qubits
NV-Centers
Spin Qubits
Spin Qubits Setup
find out more >

Applied Physics Letters ARTICLE pubs.aip.org/aip/apl

Thermal analysis of thermoelectric active cooling including external thermal resistances

Cite as: Appl. Phys. Lett. **123**, 243901 (2023); doi: 10.1063/5.0176286
Submitted: 12 September 2023 · Accepted: 20 November 2023 ·
Published Online: 11 December 2023

Nicolas Marquez Peraca,[1] Qing Zhu,[2] Junichiro Kono,[1,3,4,5] and Geoff Wehmeyer[2,a)]

AFFILIATIONS

[1]Department of Physics and Astronomy, Rice University, Houston, Texas 77005, USA
[2]Department of Mechanical Engineering, Rice University, Houston, Texas 77005, USA
[3]Department of Electrical and Computer Engineering, Rice University, Houston, Texas 77005, USA
[4]Smalley-Curl Institute, Rice University, Houston, Texas 77005, USA
[5]Department of Materials Science and NanoEngineering, Rice University, Houston, Texas 77005, USA

[a)]Author to whom correspondence should be addressed: geoff.wehmeyer@rice.edu

ABSTRACT

Thermoelectric active cooling uses nontraditional thermoelectric materials with high thermal conductivity, high thermoelectric power factor, and relatively low figure of merit (ZT) to transfer large heat flows from a hot object to a cold heat sink. However, prior studies have not considered the influence of external thermal resistances associated with the heat sinks or contacts, making it difficult to design active cooling thermal systems or compare the use of low-ZT and high-ZT materials. Here, we perform a non-dimensionalized analysis of thermoelectric active cooling under forced heat flow boundary conditions, including arbitrary external thermal resistances. We identify the optimal electrical currents to minimize the heat source temperature and find the crossover heat flows at which low-ZT active cooling leads to lower source temperatures than high-ZT and even $ZT \to +\infty$ thermoelectric refrigeration. These optimal parameters are insensitive to the thermal resistance between the heat source and thermoelectric materials, but depend strongly on the heat sink thermal resistance. Finally, we map the boundaries where active cooling yields lower source temperatures than thermoelectric refrigeration. For currently considered active cooling materials, active cooling with $ZT < 0.1$ is advantageous compared to $ZT \to +\infty$ refrigeration for dimensionless heat sink thermal conductances larger than 15 and dimensionless source powers between 1 and 100. Thus, our results motivate further investigation of system-level thermoelectric active cooling for applications in electronics thermal management.

Published under an exclusive license by AIP Publishing. https://doi.org/10.1063/5.0176286

11 December 2023 17:51:26

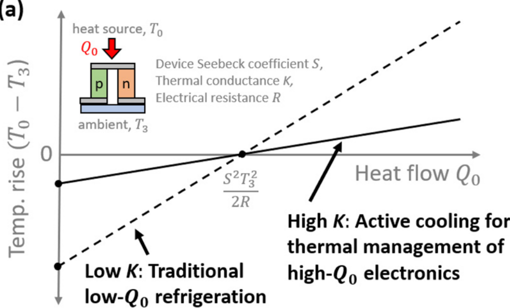
The increasing demand for high-performance computing clusters and artificial intelligence supercomputers has led to modern computer chips reaching peak powers on the order of 1000 W.[1,2] These emerging technologies are imposing stringent requirements on efficient cooling solutions capable of dissipating large powers.[3–5] In recent decades, thermoelectric (TE) devices have been explored for integrated circuit cooling.[6–8] In traditional TE cooling, the goal is to achieve source temperatures lower than that of the heat sink, i.e., refrigeration. Materials with low thermal conductivity (κ) and high power factors ($\mathrm{PF} = \sigma\alpha^2$, where α is the Seebeck coefficient and σ is the electrical conductivity), that is, high $ZT = \sigma\alpha^2 T/\kappa$, are preferred for refrigeration since the coefficient of performance (COP) of a TE module increases with increasing ZT.[9–11] Prior TE modeling works[12–25] focused on thermal models spanning across multiple layers of complexity, aspiring to understand under what circumstances TEs could outperform traditional air-cooling heat sinks or vapor-compression refrigerators.[12,15,26] The overarching conclusion has been that TE materials such as Bi_2Te_3, SiGe, and PbTe with a $ZT \sim 1$ cannot compete with traditional refrigeration systems in terms of COP.[12,15,27,28] Nevertheless, TEs have found niche applications in the market due to their small size, robustness, and simplicity.[29–31] For instance, TEs can be found in portable coolers, climate-control seat systems, and in laser diodes for temperature control and wavelength stabilization.[30–33]

In 2015, Zebarjadi[34] proposed a TE cooling mechanism—hereto referred to as TE active cooling—that considers a heat source warmer than the heat sink and uses TE materials with high κ and high PF, but relatively low-ZT. Active cooling uses both the Fourier and Peltier-induced heat flows to transfer energy in the natural gradient direction of heat transfer, consequently acting as an active heat sink.[35] This mechanism was recently experimentally implemented by Adams *et al.*[36] using correlated ($CePd_3$) and magnon-drag metals (Co) as the p- and n-type materials of an active cooling device, respectively.

Published under an exclusive license by AIP Publishing

The recent discoveries in this field of research has led to new works looking for novel and low-cost materials suitable for active cooling applications—both experimentally and computationally.[35,37–40] However, previous active cooling studies have imposed constant-temperature boundary conditions in their thermal models and have ignored external thermal resistances. Here, external thermal resistances refers to every thermal resistance in series with the TE material, including interfacial, contact, constriction/spreading resistances and the thermal resistance of the physical heat sink itself. For TE refrigeration, it has been shown that not accounting for these parameters significantly impacts the performance of the TEs and leads to higher source temperatures than those of an optimally designed TE system.[14,16,17] In addition, for most applications, the hot- and cold-side temperatures of a TE material are a response to the input conditions and not know *a priori*.[14,20]

In this paper, we perform an analysis of TE active cooling under forced heat flow boundary conditions, including arbitrary external thermal resistances. We consider a TE active cooler with device-level Seebeck coefficient (S), thermal conductance (K), and electrical resistance (R) [see Fig. 1(a)]. In what follows, the nondimensionalized variables are indicated with a superscript asterisk. We find an analytical solution for the optimal electrical current $J^*_{\min}$ that minimizes the heat source (chip) temperature, T_0 [see Fig. 1(b)]. We identify the lower crossover heat flow $(Q_0^*)_{\text{crossover}}$ at which $ZT = 0.1$ active cooling yields lower chip temperatures than $ZT = 1$ TE refrigeration. The parameters $J^*_{\min}$ and $(Q_0^*)_{\text{crossover}}$ are independent of the dimensionless heat source-side thermal conductance (G_0^*) but depend on the dimensionless heat sink-side thermal conductance (G_1^*). Moreover, we quantify the temperature difference ΔT^* between a baseline $ZT \to +\infty$ TE refrigerator system and an active cooling device. For currently considered active cooling materials, we find that active cooling with $ZT < 0.1$ is advantageous compared to $ZT \to +\infty$ refrigeration for $G_1^* > 15$ and $1 < Q_0^* < 100$. Our results pave the way toward further studies of active cooling in high-heat flux applications.



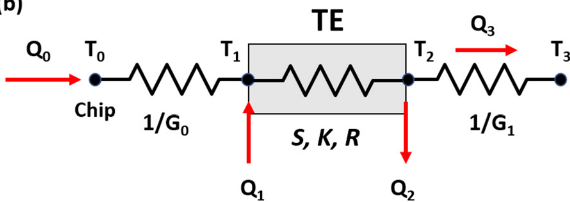


FIG. 1. Active cooling concept. (a) Traditional TE materials with high-ZT (low-K, dashed black line) are suitable for low-Q_0 refrigeration applications, aiming to keep a device at temperature T_0 below ambient temperature (T_3). Nontraditional TE materials with low-ZT (high-K, solid black line) are suitable for active cooling[34–40] applications in high-Q_0 flow cases, where the heat source is warmer than the heat sink. The crossover power, equal to $S^2T_3^2/2R$ when no external thermal resistances are included, marks the transition point between regimes. (b) Thermal resistance network used in the thermal modeling of this work. Here, arbitrary heat source-side and heat sink-side thermal resistances, $1/G_0$ and $1/G_1$, respectively, account for any finite external thermal resistances present in the system.

We solve the following three 1D, steady-state energy balance equations for a TE material, assuming a constant rate of heat transfer (Q_0) on the heat source side, a constant heat sink (T_3) temperature, and including arbitrary external thermal resistances between the heat source and the heat sink sides [$1/G_0$ and $1/G_1$, respectively, see Fig. 1(b)]:[41]

$$Q_0 = G_0(T_0 - T_1), \tag{1}$$

$$Q_0 = SIT_1 + K(T_1 - T_2) - \frac{1}{2}RI^2, \tag{2}$$

$$SIT_2 + K(T_1 - T_2) + \frac{1}{2}RI^2 = G_1(T_2 - T_3). \tag{3}$$

Here, S, K, and R are the device Seebeck coefficient, device thermal conductance, and device thermal resistance, respectively. For a TE module consisting of N p- and n-type thermocouples of length $L_{p,n}$ and cross-sectional area $A_{p,n}$, $S = N(\alpha_p - \alpha_n)$, $K = N\left(\kappa_p \frac{A_p}{L_p} + \kappa_n \frac{A_n}{L_n}\right)$, and $R = N\left(\frac{\rho_p}{A_p/L_p} + \frac{\rho_n}{A_n/L_n}\right)$, where $\alpha_{p,n}$, $\kappa_{p,n}$, and $\rho_{p,n}$ are the Seebeck coefficient, thermal conductivity, and electrical resistivity of the individual p–n legs, respectively. Q_0 is the rate of heat transfer into the system, T_0 and T_3 are the heat source (chip) and heat sink temperatures, T_1 and T_2 are the unknown TE heat source-side and heat sink-side temperatures, I is the driving current, and G_0 and G_1 are the thermal conductances between the chip and the TE and between the TE and the heat sink, respectively [see Fig. 1(b)]. We assume that S, K, and R are temperature-independent material properties; therefore no Thomson effect is present. The driving current I is taken to be positive when positive charge flows from the n- to the p-type TE leg, in which case heat is absorbed from the chip and liberated at the heat sink (cooling).[42]

To non-dimensionalize these equations, we start by dividing them by the crossover power under no external thermal resistances [i.e., $\frac{S^2T_3^2}{2R}$, see Fig. 1(a)], which gives

$$Q_0^* = G_0^*(T_0^* - T_1^*), \tag{4}$$

$$Q_0^* = 2J^*T_1^* + \frac{2}{ZT_3}(T_1^* - T_2^*) - J^{*^2}, \tag{5}$$

$$2J^*T_2^* + \frac{2}{ZT_3}(T_1^* - T_2^*) + J^{*^2} = G_1^*(T_2^* - 1). \tag{6}$$

Here, we have defined the following dimensionless parameters:

$$T^* = \frac{T}{T_3}, \tag{7}$$

$$Q_0^* = \frac{Q_0}{(S^2T_3^2/2R)}, \tag{8}$$

$$G_0^* = \frac{G_0}{(S^2T_3/2R)}, \tag{9}$$

$$G_1^* = \frac{G_1}{(S^2T_3/2R)}, \tag{10}$$

11 December 2023 17:51:26

Published under an exclusive license by AIP Publishing

$$J^* = \frac{I}{(ST_3/R)}, \quad (11)$$

$$ZT_3 = \frac{S^2}{KR} T_3. \quad (12)$$

The device thermal conductance K only appears in the denominator of Eq. (12). Therefore, changing ZT_3 while holding the other dimensionless variables fixed can be easily interpreted as directly changing K without modifying S or R. The explicit solution to Eqs. (4)–(6) is

$$T_0^* = \frac{Q_0^*}{G_0^*} + \frac{4J^{*^2} + 2Q_0^* - 2J^{*^3} ZT_3 - 2J^* Q_0^* ZT_3 + G_1^*(2 + J^{*^2} ZT_3 + Q_0^* ZT_3)}{2(G_1^* + G_1^* J^* ZT_3 - 2J^{*^2} ZT_3)}. \quad (13)$$

The G_0^* dependence only appears in the denominator of the first term in Eq. (13). Therefore, any temperature differences or derivatives of this equation are independent of G_0^*, which is an important observation for the discussion in the next sections. In the supplementary material, we show how the general solutions for T_0^* and the dimensionless current (J^*) reduce to previously reported active cooling solutions when there are no external thermal resistances. The baseline values of $G_0^* = 4$ and $G_1^* = 46$ used in some calculations in the following were estimated from previously reported TE measurements,[13,17] with dimensional values shown in Table S1.

Figure 2(a) plots the dimensionless chip temperature T_0^* as a function of J^* for different values of Q_0^*. Since it is desirable to operate the TE device at optimal electrical current, we begin by minimizing T_0^* with respect to J^* by calculating $\frac{\partial T_0^*}{\partial J^*} = 0$. When arbitrary external thermal resistances are included, the solution is a fourth-order polynomial in J^*, and only one of the four roots is real and positive, which we define as $J^*_{\min}$ (see the supplementary material). Gray vertical lines in Fig. 2(a) correspond to $J^*_{\min}$ for each Q_0^*. In general, $J^*_{\min}$ is a function of G_1^*, ZT_3, and Q_0^* and needs to be optimized in each case. From here on, we use this value of J^* in Eq. (13), which reduces the number of system parameters to be optimized from 4 to 3, assuming Q_0^* is given.

Figure 2(b) shows $T^*_{0,\min}$ plotted as a function of ZT_3 for four different values of Q_0^*. In this plot, changing ZT_3 at fixed Q_0^* is equivalent to varying K while holding the dimensional variables S, R, and Q_0 fixed for each value of Q_0^*. For low values of Q_0^*, increasing the figure of merit ZT_3 provides refrigeration below ambient temperature, as shown for $Q_0^* = 0.1$ (blue curve). However, as Q_0^* increases, lower values of ZT_3 yield lower chip temperatures than high values of ZT_3 (red, black, and purple curves, respectively), which is the basis for TE active cooling. Notice that for the red, black, and purple curves $T^*_{0,\min} > 1$ for any ZT_3, indicating that the chip temperature is always greater than the ambient temperature, as expected for active cooling. For $Q_0^* = 1$ and $G_{0,1} \to +\infty$, the $T^*_{0,\min} \to 1$ limit is recovered (see the supplementary material), in agreement with the Fig. 1(a) sketch showing $T_0 = T_3$ for $Q_0 = S^2 T_3^2 / 2R$. The qualitative trends shown here also hold in the case where $G_0^* > G_1^*$, as shown in Fig. S2.

Figure 3 plots $T^*_{0,\min}$ as a function of Q_0^* for $ZT_3 = 1$ (dashed lines) and $ZT_3 = 0.1$ (solid lines) and three different values of G_1^*. This plot is a quantitative version of the sketch shown in Fig. 1(a), now considering the effects of heat sink thermal resistances. Here, Q_0^* increases while ZT_3 is held constant at either 0.1 or 1; from Eqs. (8)–(12), this scenario could correspond to an increase in the dimensional heat flow Q_0 at fixed S and R while considering a large K (low ZT_3) or small K (high ZT_3). We define the dimensionless lower and upper crossover powers $(Q_0^*)_{\text{crossover}}$ and $(Q_0^*)_{\max}$ as the intersection points between these two curves. Only the $(Q_0^*)_{\text{crossover}}$ intersection is shown in Fig. 3, while the behavior of $(Q_0^*)_{\max}$ is explored below. Figure 3 shows that active cooling with $ZT_3 = 0.1$ yields a lower chip temperature than $ZT_3 = 1$ refrigeration for $Q_0^* > (Q_0^*)_{\text{crossover}}$ [while $Q_0^* < (Q_0^*)_{\max}$, as in Fig. 3]. $(Q_0^*)_{\text{crossover}}$ increases from $(Q_0^*)_{\text{crossover}} \sim 0.5$ for $G_1^* = 2$ to $(Q_0^*)_{\text{crossover}} > 1$ for

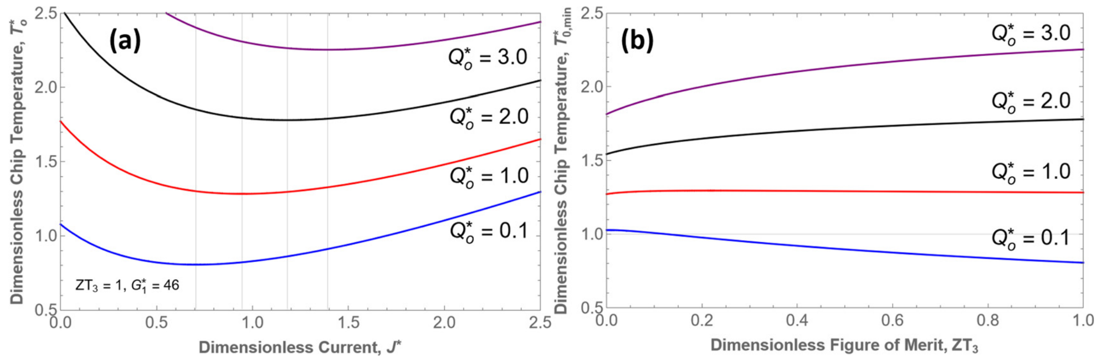


FIG. 2. Chip temperature optimization. (a) The optimal electrical current $J^*_{\min}$ (vertical gray lines) increases with increasing Q_0^*. $J^*_{\min}$ is independent of the dimensionless heat source thermal conductance, G_0^*. Numerical values used for these calculations are: $G_0^* = 4$, $G_1^* = 46$, $ZT_3 = 1$ (see the supplementary material), and Q_0^* from 0.1 to 3. (b) For low values of Q_0^*, increasing the figure of merit ZT_3 provides refrigeration below ambient temperature (blue curve). However, as Q_0^* increases, lower—rather than higher—values of ZT_3 yields a lower chip temperature. Horizontal gray line represents $T_0^* = 1$, in which the chip temperature and ambient temperature are equal. Numerical values used for these calculations are $G_0^* = 4$, $G_1^* = 46$, $J^* = J^*_{\min}$.

11 December 2023 17:51:26

Published under an exclusive license by AIP Publishing

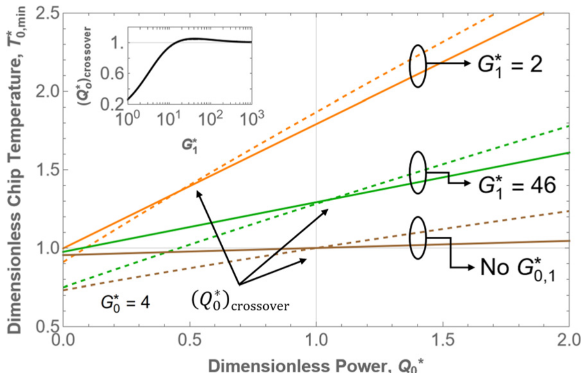


FIG. 3. Crossover between low-ZT_3 active cooling and high-ZT_3 refrigeration. The $ZT_3 = 1$ (dashed lines) and $ZT_3 = 0.1$ (solid lines) curves intersect at the dimensionless lower $(Q_0^*)_{crossover}$ (black arrows) and upper $(Q_0^*)_{max}$ (not shown) crossover powers, marking the transition between the active cooling and refrigeration regimes. For $(Q_0^*)_{max} > Q_0^* > (Q_0^*)_{crossover}$, active cooling with low-ZT_3 yields a lower chip temperature than high-ZT_3 refrigeration. Vertical and horizontal gray lines corresponds to $Q_0^* = 1$ and $T^*_{0,min} = 1$, respectively. Inset: $(Q_0^*)_{crossover}$ is independent of G_0^* and shifts to lower values as G_1^* decreases.

$G_1^* = 46$ and approaches 1 for the case of infinite $G^*_{0,1}$, representing no thermal resistances. $(Q_0^*)_{crossover}$ is only a function of G_1^*, as shown in the inset of Fig. 3.

The physical meaning of the crossover points shown in Fig. 3 can be understood by referring to the simpler case with no external thermal resistances. Figure 1(a) shows that crossover power in the no-external resistance case represents the scenario where there is no temperature difference across the TE material, meaning that the Fourier heat flow contribution $K(T_1 - T_2)$ in Eqs. (2) and (3) vanishes for all K. The physical interpretation of the crossover in Fig. 3 including external resistances is more complicated because the crossover conditions do not typically correspond to the case when $T_1^* = T_2^*$, but rather simply differentiate the regions where high K is preferable to low K for mitigating the temperature rise.

Figure 3 shows that at smaller G_1^* and $ZT_3 = 1$, the chip temperature is larger than the ambient even for small Q_0^* near 0.1, meaning that the high-K (low-ZT_3) active cooling device is more advantageous for heat removal at smaller values of Q_0^*, compared to the no-resistance scenario. Beyond $G_1^* = 15$, $(Q_0^*)_{crossover}$ stays within 5% of unity, and we recover the crossover of Fig. 1(a) $(S^2T_3^2/2R)$ for negligible thermal resistances. In dimensional units, using representative values from prior TE measurements reported in Table S1, for $G_1 \sim 0.5$ W/K and $ZT_3 = 0.1$, active cooling is more advantageous than $ZT_3 = 1$ refrigeration for powers above $(Q_0)_{crossover} \sim 30$ W.

Figure 4 quantifies the temperature difference between a baseline $ZT_3 \to +\infty$ TE refrigeration system and an active cooling device. We define a dimensionless temperature difference $\Delta T^* = T^*_{0,baseline} - T^*_{0,min}$. Here, we are comparing two systems with identical external thermal conductances G_0^* and G_1^* and have chosen $T^*_{0,baseline}$ to be the temperature of a $ZT_3 \to +\infty$ TE refrigerator and $T^*_{0,min}$ the temperature of an active cooling device with dimensionless figure of merit ZT_3. Taking ZT_3 to infinity for finite G_1^* corresponds to taking a device with thermal conductance $K = 0$. ΔT^* does not depend on G_0^* since we are calculating a temperature difference [see Eq. (13)]. In the $\Delta T^* > 0$ (outperformance) regions, low-ZT_3 active cooling leads to lower source temperatures than $ZT_3 \to +\infty$ refrigeration. This improvement compared to even the $ZT_3 \to +\infty$ limit is possible, since in active cooling, the heat source temperature is larger than ambient [see Fig. 1(a)], and the system operates in forced heat transfer mode.[43] The thermal energy from the hot heat source and work applied to the system are dissipated at the cold heat sink, consistent with the second law of thermodynamics, consequently making active cooling more advantageous for heat removal than refrigeration.[43,44] Gray areas in Fig. 4 correspond to $\Delta T^* < 0$ and represent regions where there is no benefit in using active cooling over TE refrigeration (underperformance). White solid lines are the $\Delta T^* = 0$ boundaries in each case.

Figure 4 shows that the outperformance regions compared to the $ZT_3 \to +\infty$ limit shrink as G_1^* decreases: in active cooling, the excess power that is transferred to the TE material for Peltier cooling must be dissipated by the heat sink, and a lower G_1^* makes this task more

11 December 2023 17:51:26

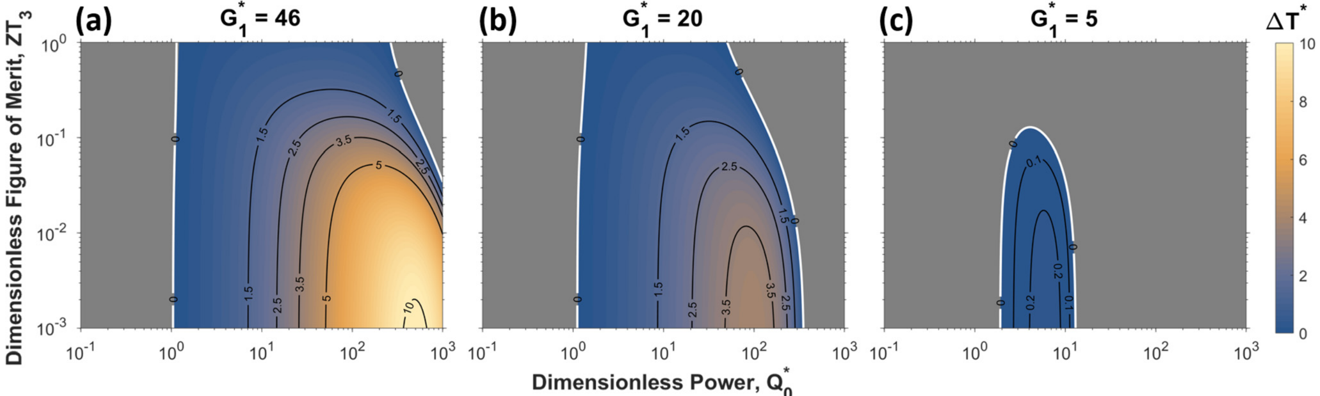


FIG. 4. Outperformance of low-ZT_3 active cooling over $ZT_3 \to +\infty$ refrigeration. $\Delta T^* = T^*_{0,baseline} - T^*_{0,min}$ is the temperature difference between a $ZT_3 \to +\infty$ baseline refrigeration system and an active cooling device with dimensionless figure of merit ZT_3 for dimensionless heat sink conductances of (a) 46, (b) 20, and (c) 5. Taking ZT_3 to infinity while holding G_1^* and Q_0^* fixed is equivalent to taking the thermal conductance K to 0 at fixed power factor. In the regions where $\Delta T^* > 0$, active cooling yields lower chip temperatures than $ZT_3 \to +\infty$ TE refrigeration; this improvement is possible because the chip temperature is warmer than the ambient temperature. Gray areas correspond to $\Delta T^* < 0$ and represent regions where there is no benefit in using active cooling over refrigeration. White solid lines are the $\Delta T^* = 0$ boundaries in each case. ΔT^* is independent of G_0^*.

Published under an exclusive license by AIP Publishing

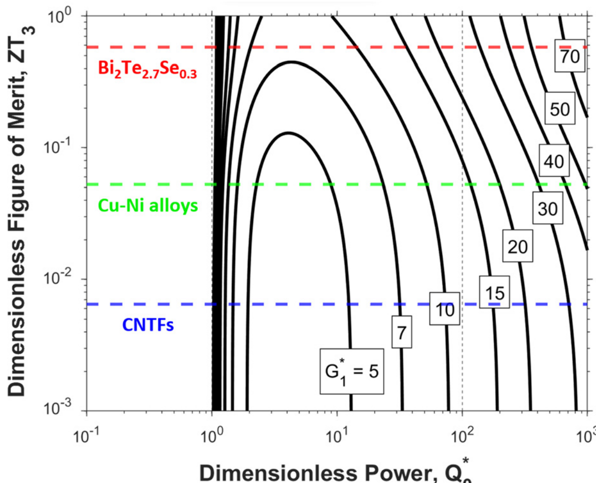


FIG. 5. Boundaries of the outperformance regions. For a given value of G_1^*, the $\Delta T^* = 0$ boundaries (white solid lines in Fig. 4) delimit the region where low-ZT_3 active cooling outperforms $ZT_3 \to +\infty$ refrigeration. These boundaries are independent of G_0^* and uniquely determined by G_1^* for a given Q_0^* and ZT_3. Horizontal dashed lines are the ZT_3 values of a common TE material (BiTeSe,[45] red) and two candidates for active cooling applications, Cu–Ni alloys[35] (green) and carbon nanotube fibers[37] (CNTFs, blue), respectively. Vertical dashed lines correspond to $Q_0^* = 1$ and $Q_0^* = 10^2$, respectively.

challenging. For example, Fig. 4(a) shows that a dimensionless temperature difference $\Delta T^* > 2.5$ compared to $ZT_3 \to +\infty$ can be achieved for $ZT_3 < 0.1$ and Q_0^* between 20 and 300. In addition, we can obtain the relative temperature reduction by calculating $|T^*_{0,\text{baseline}} - T^*_{0,\text{min}}|/T^*_{0,\text{baseline}} = \Delta T^*/T^*_{0,\text{baseline}}$. For $\Delta T^* \sim 2$ and $Q_0^* = 10$, we obtain a $\Delta T^*/T^*_{0,\text{baseline}} \sim 63\%$ relative temperature reduction if active cooling is selected over $ZT_3 \to +\infty$ TE refrigeration.

Figure 5 investigates the $\Delta T^* = 0$ boundaries of the outperformance regions (white solid lines in Fig. 4) as a function of G_1^*. For an application with specific Q_0^*, ZT_3, or G_1^* requirements, this plot provides the range of values needed to design an active cooling device capable of remaining competitive against best-case scenario TE refrigeration. We find that for currently considered active cooling materials, such as Cu-Ni alloys[35] (green horizontal dashed line) and carbon nanotube fibers[37] (CNTFs, blue horizontal dashed line), active cooling with $ZT < 0.1$ is advantageous compared to $ZT_3 \to +\infty$ refrigeration for $G_1^* > 15$ and $1 < Q_0^* < 100$ (vertical dashed lines), respectively. Common TE materials, such as BiTeSe (red horizontal dashed line),[45] on the other hand, require $G_1^* > 25$ to outperform $ZT_3 \to +\infty$ TE refrigeration for the same Q_0^* range.

This manuscript primarily focuses on changing ZT_3 by tuning the thermal conductance K at fixed power factor. If instead we increase the power factor while holding the dimensional values of K, G_1, and Q_0 constant, this will have the effect of increasing ZT_3, while reducing Q_0^* and G_1^*. These changes tend to reduce the temperature rise in the system, while also making active cooling less advantageous than traditional TE refrigeration, as the limitation of refrigeration is based on the finite power factor [see crossover point of $S^2T_3^2/2R$ in Fig. 1(a)]. Therefore, as expected, it is optimal to select the TE material to maximize the power factor for both TE refrigeration and active cooling applications. Prior work has also shown that thin-film[46,47] and/or micro-thermoelectric devices[24,48] can be advantageous for near-junction thermal management of high heat fluxes. Based on the modeling in this work, further experimental studies integrating high power factor and high thermal conductance active cooling materials[37,40] in thin-film or micro-thermoelectric format could offer opportunities to mitigate chip temperature rises if contact resistances can be made sufficiently small and fabrication can be performed in a scalable manner.

In summary, this work uses analytical solutions to the one-dimensional TE equations to explore the temperature profiles and heat flows associated with TE active cooling when arbitrary external thermal resistances are included. We use this solution to obtain the range of figures of merit and dimensionless heat flows at which active cooling leads to lower source temperatures than $ZT_3 \to +\infty$ TE refrigeration and to establish the lower and upper bounds of this region. These results show that for state-of-the-art materials, active cooling is advantageous compared to $ZT_3 \to +\infty$ refrigeration for dimensionless heat sink thermal conductances larger than 15 and dimensionless source powers between 1 and 100 using dimensional values from previously reported TE measurements.[13,17] We estimate a relative temperature reduction of at least 60% can be achieved for source powers on the order of 1000 W if active cooling is selected over TE refrigeration and the active cooling device has the same S and R as the traditional TE device. The solutions presented here can be used in the design and analysis of active cooling devices for thermal management and temperature control of high-power electronics.

See the supplementary material for a description of the electrical current optimization procedure, theoretical limiting cases of the active cooling equations, temperature calculations for the case where $G_0^* > G_1^*$, and dimensional values used to obtain the base-case dimensionless G_0^* and G_1^* parameters.

This study was supported by the National Science Foundation under Grant No. 2230727. N.M.P would like to gratefully acknowledge Liu Idea Lab for Innovation and Entrepreneurship for their support. J.K. acknowledges support from the Robert A. Welch Foundation through Grant No. C-1509.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Nicolas Marquez Peraca: Conceptualization (equal); Investigation (equal); Methodology (equal); Writing – original draft (lead). **Qing Zhu:** Methodology (supporting). **Junichiro Kono:** Supervision (equal); Writing – review & editing (equal). **Geoff Wehmeyer:** Conceptualization (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

11 December 2023 17:51:26

Published under an exclusive license by AIP Publishing

REFERENCES

[1]A. Reuther, P. Michaleas, M. Jones, V. Gadepally, S. Samsi, and J. Kepner, "AI and ML accelerator survey and trends," in *IEEE High Performance Extreme Computing Conference (HPEC)* (IEEE, 2022).

[2]S. Shankar and A. Reuther, "Trends in energy estimates for computing in AI/machine learning accelerators, supercomputers, and compute-intensive applications," in *IEEE High Performance Extreme Computing Conference (HPEC)* (IEEE, 2022).

[3]K. Ebrahimi, G. F. Jones, and A. S. Fleischer, "A review of data center cooling technology, operating conditions and the corresponding low-grade waste heat recovery opportunities," Renewable Sustainable Energy Rev. **31**, 622–638 (2014).

[4]Z. Li and S. G. Kandlikar, "Current status and future trends in data-center cooling technologies," Heat Transfer Eng. **36**, 523–538 (2015).

[5]C. Nadjahi, H. Louahlia, and S. Lemasson, "A review of thermal management and innovative cooling strategies for data center," Sustainable Comput. **19**, 14–28 (2018).

[6]F. J. DiSalvo, "Thermoelectric cooling and power generation," Science **285**, 703–706 (1999).

[7]S. B. Riffat and X. Ma, "Thermoelectrics: A review of present and potential applications," Appl. Therm. Eng. **23**, 913–935 (2003).

[8]L. E. Bell, "Cooling, heating, generating power, and recovering waste heat with thermoelectric systems," Science **321**, 1457–1461 (2008).

[9]J. R. Sootsman, D. Y. Chung, and M. G. Kanatzidis, "New and old concepts in thermoelectric materials," Angew. Chem., Int. Ed. **48**, 8616–8639 (2009).

[10]A. M. Dehkordi, M. Zebarjadi, J. He, and T. M. Tritt, "Thermoelectric power factor: Enhancement mechanisms and strategies for higher performance thermoelectric materials," Mater. Sci. Eng., R **97**, 1–22 (2015).

[11]L. A. Nimmagadda, R. Mahmud, and S. Sinha, "Materials and devices for on-chip and off-chip Peltier cooling: A review," IEEE Trans. Compon., Packag. Manuf. Technol. **11**, 1267–1281 (2021).

[12]R. Simons and R. Chu, "Application of thermoelectric cooling to electronic equipment: A review and analysis," in *Sixteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No. 00CH37068)* (IEEE, 2000).

[13]P. E. Phelan, V. A. Chiriac, and T.-Y. Lee, "Current and future miniature refrigeration cooling technologies for high power microelectronics," IEEE Trans. Compon. Packag.g Technol. **25**, 356–365 (2002).

[14]G. L. Solbrekken, K. Yazawa, and A. Bar-Cohen, "Chip level refrigeration of portable electronic equipment using thermoelectric devices," in *International Electronic Packaging Technical Conference and Exhibition* (ASME, 2003), Vol. 36908, pp. 647–652.

[15]R. Simons, M. Ellsworth, and R. Chu, "An assessment of module cooling enhancement with thermoelectric coolers," J. Heat Transfer **127**, 76–84 (2005).

[16]R. A. Taylor and G. L. Solbrekken, "An improved optimization approach for thermoelectric refrigeration applied to portable electronic equipment," in *International Electronic Packaging Technical Conference and Exhibition* (ASME, 2005), Vol. 42002, pp. 2139–2145.

[17]K. Fukutani and A. Shakouri, "Design of bulk thermoelectric modules for integrated circuit thermal management," IEEE Trans. Compon. Packag. Technol. **29**, 750–757 (2006).

[18]M. H. Hasan and K. C. Toh, "Optimization of a thermoelectric cooler-heat sink combination for active processor cooling," in *9th Electronics Packaging Technology Conference* (IEEE, 2007), pp. 848–857.

[19]M. Hodes, "Optimal pellet geometries for thermoelectric refrigeration," IEEE Trans. Compon. Packag. Technol. **30**, 50–58 (2007).

[20]R. A. Taylor and G. L. Solbrekken, "Comprehensive system-level optimization of thermoelectric devices for electronic cooling applications," IEEE Trans. Compon. Packag. Technol. **31**, 23–31 (2008).

[21]H. Zhang, Y. Mui, and M. Tarin, "Analysis of thermoelectric cooler performance for high power electronic packages," Appl. Therm. Eng. **30**, 561–568 (2010).

[22]K. Yazawa, A. Ziabari, Y. R. Koh, A. Shakouri, V. Sahu, A. G. Fedorov, and Y. Joshi, "Cooling power optimization for hybrid solid-state and liquid cooling in integrated circuit chips with hotspots," in *13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (IEEE, 2012), pp. 99–106.

[23]M. Hodes, "Optimal design of thermoelectric refrigerators embedded in a thermal resistance network," IEEE Trans. Compon., Packag. Manuf. Technol. **2**, 483–495 (2012).

[24]Y. R. Koh, K. Yazawa, and A. Shakouri, "Performance and mass optimization of thermoelectric microcoolers," Int. J. Therm. Sci. **97**, 143–151 (2015).

[25]M. R. Pearson and C. E. Lents, "Dimensionless optimization of thermoelectric cooler performance when integrated within a thermal resistance network," J. Heat Transfer **138**, 081301 (2016).

[26]J. S. Brown and P. A. Domanski, "Review of alternative cooling technologies," Appl. Therm. Eng. **64**, 252–262 (2014).

[27]G. J. Snyder and E. S. Toberer, "Complex thermoelectric materials," Nat. Mater. **7**, 105–114 (2008).

[28]J. Mao, G. Chen, and Z. Ren, "Thermoelectric cooling materials," Nat. Mater. **20**, 454–461 (2021).

[29]D. Enescu and E. O. Virjoghe, "A review on thermoelectric cooling parameters and performance," Renewable Sustainable Energy Rev. **38**, 903–916 (2014).

[30]D. Zhao and G. Tan, "A review of thermoelectric cooling: Materials, modeling and applications," Appl. Therm. Eng. **66**, 15–24 (2014).

[31]S. Twaha, J. Zhu, Y. Yan, and B. Li, "A comprehensive review of thermoelectric technology: Materials, applications, modelling and performance improvement," Renewable Sustainable Energy Rev. **65**, 698–726 (2016).

[32]J. Fairbanks, *Thermoelectric Applications in Vehicles Status 2008* (US Department of Energy, 2008).

[33]J. Yang and F. R. Stabler, "Automotive applications of thermoelectric materials," J. Electron. Mater. **38**, 1245 (2009).

[34]M. Zebarjadi, "Electronic cooling using thermoelectric devices," Appl. Phys. Lett. **106**, 203506 (2015).

[35]S. Li, K. Snyder, M. S. Akhanda, R. Martukanitz, M. Mitra, J. Poon, and M. Zebarjadi, "Cost-efficient copper-nickel alloy for active cooling applications," Int. J. Heat Mass Transfer **195**, 123181 (2022).

[36]M. Adams, M. Verosky, M. Zebarjadi, and J. Heremans, "Active Peltier coolers based on correlated and magnon-drag metals," Phys. Rev. Appl. **11**, 054008 (2019).

[37]N. Komatsu, Y. Ichinose, O. S. Dewey, L. W. Taylor, M. A. Trafford, Y. Yomogida, G. Wehmeyer, M. Pasquali, K. Yanagi, and J. Kono, "Macroscopic weavable fibers of carbon nanotubes with giant thermoelectric power factor," Nat. Commun. **12**, 4931 (2021).

[38]H. Luo, X. Li, Y. Wang, Y. Jin, M. Yao, and J. Yang, "High-throughput screening of room temperature active Peltier cooling materials in Heusler compounds," npj Comput. Mater. **8**, 199 (2022).

[39]F. Garmroudi, M. Parzer, A. Riss, C. Bourgès, S. Khmelevskyi, T. Mori, E. Bauer, and A. Pustogow, "High thermoelectric performance in metallic NiAu alloys," arXiv:2303.03062 (2023).

[40]T. da Câmara Santa Clara Gomes, N. Marchal, F. Abreu Araujo, and L. Piraux, "Flexible active Peltier coolers based on interconnected magnetic nanowire networks," Nanomaterials **13**, 1735 (2023).

[41]H. Lee, *Thermoelectrics: Design and Materials* (John Wiley & Sons, 2016).

[42]M. Hodes, "On one-dimensional analysis of thermoelectric modules (TEMs)," IEEE Trans. Compon. Packag. Technol. **28**, 218–229 (2005).

[43]J. Ramousse and C. Goupil, "Chart for thermoelectric systems operation based on a ternary diagram for bithermal systems," Entropy **20**, 666 (2018).

[44]D. V. Schroeder, *An Introduction to Thermal Physics* (Oxford University Press, 1999).

[45]Q. Li, Z. Wei, Q. Ma, Z. Li, and J. Luo, "Optimizing room-temperature thermoelectric performance of n-type $Bi_2Te_{2.7}Se_{0.3}$," ACS Omega **6**, 33883–33888 (2021).

[46]I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley, and R. Venkatasubramanian, "On-chip cooling by superlattice-based thin-film thermoelectrics," Nat. Nanotechnol. **4**, 235–238 (2009).

[47]E. Isotta, J. Andrade-Arvizu, U. Syafiq, A. Jiménez-Arguijo, A. Navarro-Güell, M. Guc, E. Saucedo, and P. Scardi, "Towards low cost and sustainable thin film thermoelectric devices based on quaternary chalcogenides," Adv. Funct. Mater. **32**, 2202157 (2022).

[48]Q. Zhang, K. Deng, L. Wilkens, H. Reith, and K. Nielsch, "Micro-thermoelectric devices," Nat. Electron. **5**, 333–347 (2022).

11 December 2023 17:51:26

Published under an exclusive license by AIP Publishing