

Reconfigurable Resistive Switching in VO₂/La_{0.7}Sr_{0.3}MnO₃/Al₂O₃ (0001) Memristive Devices for Neuromorphic Computing

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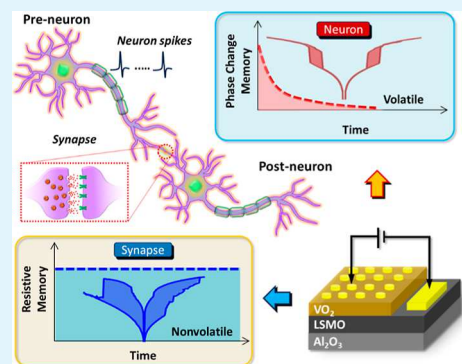
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ABSTRACT: The coexistence of nonvolatile and volatile switching modes in a single memristive device provides flexibility to emulate both neuronal and synaptic functions in the brain. Furthermore, such a device structure may eliminate the need for additional circuit elements such as transistor-based selectors, enabling low-power consumption and high-density device integration in fully memristive spiking neural networks. In this work, we report dual resistive switching (RS) modes in VO₂/La_{0.7}Sr_{0.3}MnO₃ (LSMO) bilayer memristive devices. Specifically, the nonvolatile RS is driven by the movement of oxygen vacancies (V_o) at the VO₂/LSMO interface and requires a higher biasing voltage, whereas the volatile RS is controlled by the metal–insulator transition (MIT) of VO₂ under a lower biasing voltage. The simple device structure is electrically driven between the two RS modes and thus can operate as a one selector–one resistor (1S1R) cell, which is a desirable feature in memristive crossbar arrays to avoid the sneak-path current issue. The RS modes are found to be stable and repeatable and can be reconfigured by exploiting the interfacial and phase transition properties, and thus, they hold great promise for applications in memristive neural networks and neuromorphic computing.

KEYWORDS: metal–insulator phase transition, reconfigurable memristor, VO₂/LSMO heterostructures, dual resistive switching, neuromorphic computing



1. INTRODUCTION

Traditional digital computers have faced inherent limitations when it comes to tasks that require the cognitive capabilities of the brain, such as pattern recognition, learning, adaptation, and parallel processing of massive amounts of data in real time.¹ Meanwhile, neuromorphic computing based on memristive devices has emerged as a crucial area of research and development due to its potential to revolutionize the field of artificial intelligence and computing.^{2,3} Memristive devices, which exhibit variable resistance based on their previous electrical history, replicate certain fundamental aspects of neural behavior.⁴ This capability enables the creation of networks with artificial neurons and synapses. Neuromorphic systems based on such networks not only process information but also learn from it, adapt, and make decisions with remarkable efficiency and parallelism.^{5,6}

Vanadium oxide (VO₂)-based memristive devices are one of the promising classes of materials in the field of artificial neurons.^{7–9} These artificial neurons leverage the unique property of VO₂ to emulate the nonlinear dynamics of biological neurons, which is the metal–insulator transition (MIT) and quick relaxation in response to external stimuli such as electrical pulses.⁹ In the past decade, a great deal of research effort has been devoted to understanding the electrically induced MIT in VO₂ thin films on both crystalline

and amorphous substrates (Al₂O₃, TiO₂, Si, SiO₂, Ge, Ti, Pt, and TiN).^{10–15} The MIT in VO₂ thin films have been well achieved on many different substrates, which makes this material particularly appealing for developing CMOS-compatible artificial neurons.¹⁶ For instance, Yi et al. demonstrated that the sputter-deposited Pt/VO₂/Pt devices on Si₃N₄/Si substrates achieve several biological neuronal dynamics with a superior energy efficiency of >10¹³ spikes/J.⁹

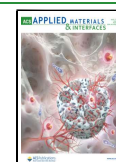
Recently, a reconfigurable resistive switching (RS) system that can perform both volatile (as a neuron) and nonvolatile (as a synapse) switching has gained more attention as it holds great potential for realizing energy and scaling compatible fully memristive neural networks.^{3,17,18} This comes in handy in situations where the random change of conductance state due to the sneak-path current can be an issue in large-scale memristor arrays. So far, one transistor–one memristor (1T1R) or one selector–one resistor (1S1R) architectures have been adapted to avoid the read/write noise due to the

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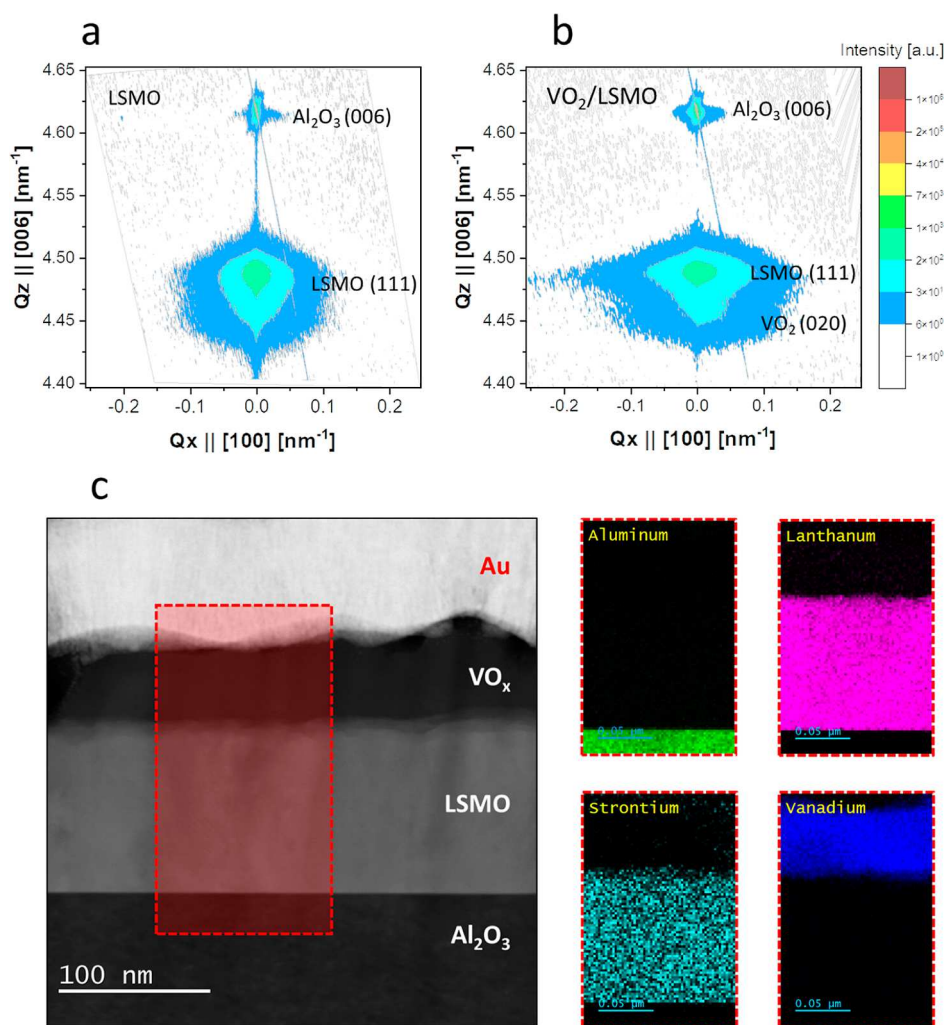


Figure 1. (a,b) X-ray RSM of LSMO and VO_2/LSMO thin films with respect to $\text{Al}_2\text{O}_3(006)$. (c) A cross-sectional STEM image of the Au/ VO_2 /LSMO/ Al_2O_3 device with elemental mapping.

sneak-path current and enhance the training/learning accuracy.^{19,20} Unfortunately, such an architecture is prone to high energy consumption, a large footprint, limited scalability, and slow switching speed as it often relies on additional transistors or filamentary-type devices. Thus, dynamically configurable phase transition materials such as VO_2 and NbO_2 integrated with other oxide materials would be a promising alternative. The switching in these binary oxides is purely electronic and possesses high endurance, ultrafast switching speed (≤ 10 ns), and ultralow switching energies (< 10 fJ). Fu et al. constructed a spiking convolutional neural network with $\text{V}/\text{VO}_x/\text{HfWO}_x/\text{Pt}$ devices that can be operated under RRAM (resistive) and threshold (selector) modes by simply tuning the electric field.¹⁷ This device architecture has already shown significant improvements in terms of energy and area constraints compared to conventional 1T1R or 1S1R architectures, entailing more exploration in this direction.

In this work, we propose a new reconfigurable Au/ VO_2 /LSMO memristive device that exhibits nonvolatile and volatile RS modes by simply varying the applied electric field across the device. To the best of our knowledge, this is the first report on the VO_2/LSMO bilayer system and thus is the subject of fundamental interest for microelectronic devices in general. The device operates in nonvolatile and volatile modes, where

the switching is controlled by the VO_2/LSMO interface barrier and the MIT of VO_2 , respectively. Specifically, the nonvolatile RS is characterized by the formation and collapse of the VO_2/LSMO interface barrier by oxygen vacancy (V_o) migration and requires a high (bipolar) threshold voltage (± 4 V) to switch between the high-resistance state (HRS) and low-resistance state (LRS), whereas the volatile RS results from the MIT of VO_2 by Joule heating and requires a low threshold voltage (~ 1.5 V). These versatile RS properties within a single device have the potential to combine two fundamental elements, artificial neurons and synapses, for neuromorphic systems. Furthermore, it has the potential of eliminating the need for additional circuit components like transistors or filamentary memristor-based selectors, enabling higher-density device integration, and ultimately reducing the operational power of the memristive artificial neural networks.

2. RESULTS AND DISCUSSION

The structure of the LSMO and VO_2/LSMO bilayer films on Al_2O_3 (0001) substrates was investigated by X-ray diffraction (XRD). Figure 1a shows the reciprocal space mapping (RSM) of the Al_2O_3 (006) and LSMO (111) peaks for an LSMO single-layer film. Figure 1b shows an RSM of the VO_2/LSMO bilayer. The $2\theta-\omega$ scan of a single-layer LSMO thin film

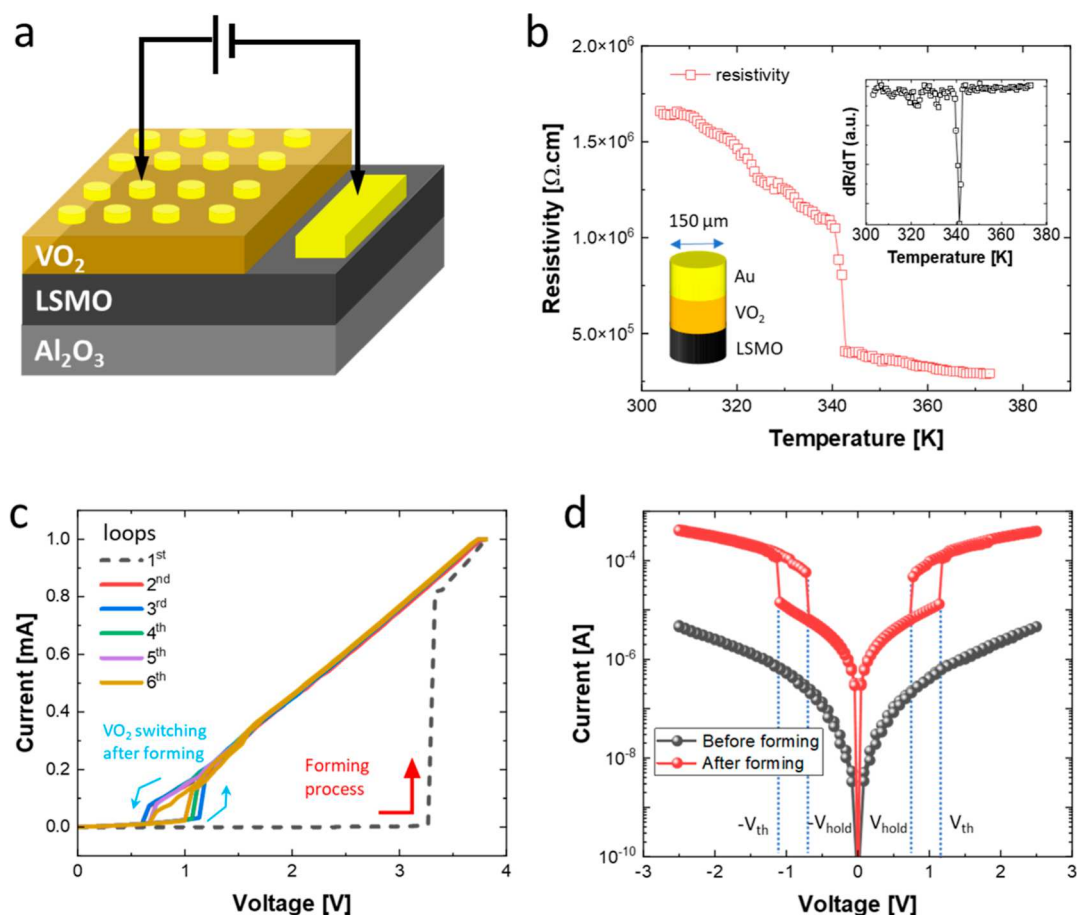


Figure 2. (a) Schematic illustration of the Au/ VO_2 /LSMO heterostructure device for current–voltage (I – V) measurements. (b) Resistance vs temperature (R – T) characteristic of the device. Insets show the individual device used for R – T measurements and the corresponding first-order derivative of the R – T . (c) I – V curves of the device where forming occurred in the first sweep and VO_2 threshold switching in the subsequent voltage sweeps. (d) I – V curves of the device before and after forming.

deposited on Al_2O_3 indicates that LSMO is preferentially oriented in the (110) and (111) directions (Figure S1). Previous studies have shown that the preferred growth direction of LSMO on Al_2O_3 (0001) is (111) with the orientation ratio as high as 83.4% with respect to other directions.²¹ As evident in the RSM, the peak around 40° in the bilayer sample is significantly enhanced compared to that of LSMO/ Al_2O_3 . This is not surprising as the VO_2 (020) peak is at 39.9° , which is extremely close to LSMO (111) at 40.5° . In a comparison of the RSMs, the pure LSMO layer shows LSMO (111) along with Al_2O_3 (006), whereas the VO_2 /LSMO bilayer shows overlapped peaks that can be attributed to LSMO (111) and VO_2 (020), as labeled in Figure 1b. It should also be pointed out that although the LSMO thin film is not epitaxial, VO_2 still shows (020) preferred orientation in our samples. Next, the electrical transport property of pure LSMO films of thickness ~ 110 nm on Al_2O_3 substrates is measured, and the sheet resistivity is found to be ~ 1.8 m $\Omega\cdot\text{cm}$, as shown in Figure S3, which is in the range of reported resistivity for LSMO films.²² As compared to the VO_2 film, the LSMO buffer layer (also serving as the bottom electrode) is much more conductive. To measure the RS characteristics, vertical devices with a structure of Au/ VO_2 /LSMO were fabricated, as shown in Figure 1c, where the VO_2 thickness was ~ 50 nm whereas the LSMO thickness was ~ 110 nm. The diameter of the Au top electrodes was $\sim 150\ \mu\text{m}$ (Figure S2). Inset images in

Figure 1c show elemental mapping of VO_2 /LSMO heterostructure, indicating distinct layer structure.

Figure 2 shows the device architecture and typical I – V characteristics of the Au/ VO_2 /LSMO device before and after the forming process. Prior to the measurement of electric field-induced switching characteristics, the MIT of VO_2 was confirmed by resistance vs temperature (R – T) measurement, as shown in Figure 2b. The resistance of an individual cell is probed at 0.1 V with increasing temperature, as shown in the inset of Figure 2b. The MIT occurs at ~ 340 K, as demonstrated by an abrupt drop in resistance, which agrees well with the VO_2 bulk phase transition temperature.^{10,23} However, the magnitude of the phase transition in our vertical device seems much smaller than that of VO_2 thin films on insulating substrates where a lateral configuration has been commonly used for R – T measurement.^{24,25} This is expected as the resistance of VO_2 in the vertical geometry is comparable to or smaller than the electrode and contact resistance, whereas the resistance of VO_2 in a lateral configuration is much larger than the electrode and contact resistance. Another possible reason for this could be the presence of defects and grain boundaries in the VO_2 film, as suggested by previous reports.^{26,27} The gradual decrease in resistance below and above the phase transition temperature of 340 K can be attributed to the increased charge carrier concentration in the VO_2 thin films by the thermal effect.²⁸ Especially, the decrease

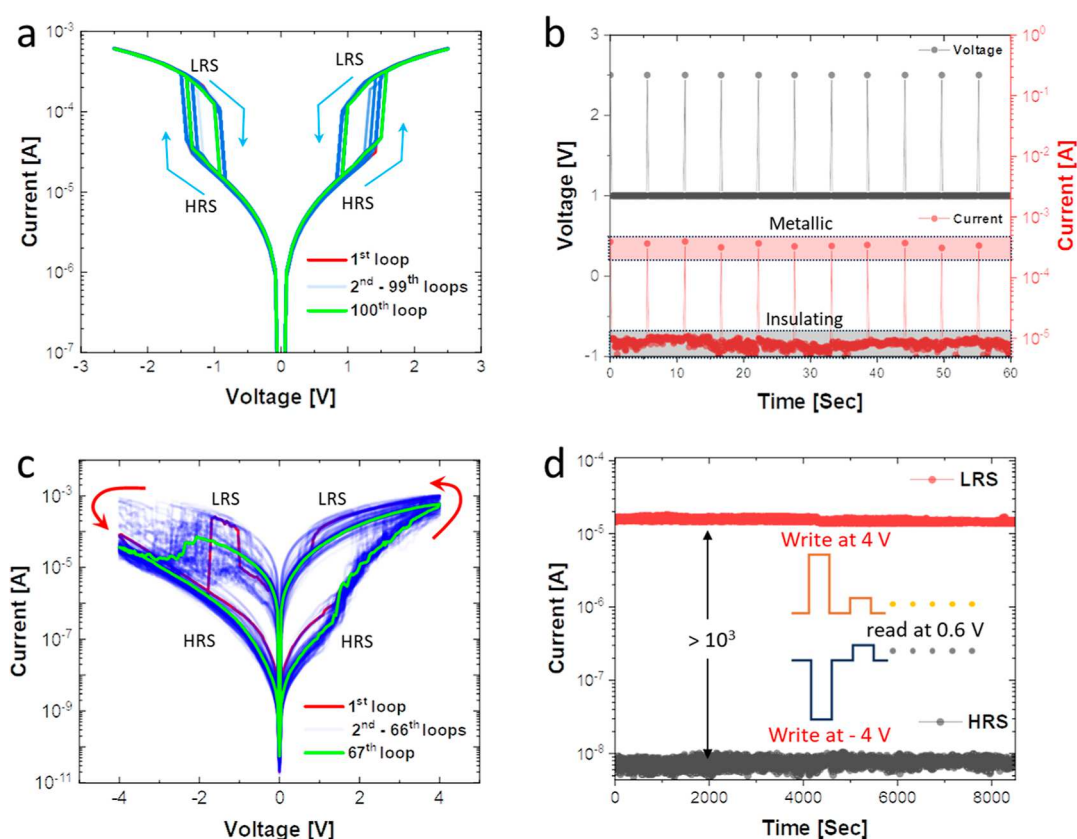


Figure 3. Volatile and nonvolatile RS of the Au/VO₂/LSMO device. (a) Volatile RS induced by the phase transition of VO₂ in a small voltage range of -2.5 to 2.5 V. (b) Retention characteristics under the volatile switching mode. (c) Nonvolatile RS induced by the forming and rupturing of the VO₂/LSMO interface barrier at a large voltage range of -4 to 4 V. (d) Retention characteristics of the nonvolatile mode. Write and read pulse amplitudes are indicated in the figures, and the pulse width is fixed at 100 ms.

in overall resistance after MIT in the VO₂ could be due to a decrease in resistivity of the LSMO bottom electrode at elevated temperatures.

Next, we systematically studied the switching characteristics of the Au/VO₂/LSMO device by applying a ramping DC bias across the Au top electrode and the LSMO bottom electrodes. Initially, the as-fabricated device exhibits the HRS and requires a high voltage sweep from 0 to 4 V to switch to the LRS, which is called the set or forming process (Figure 2c). Once the device is formed, the consecutive I - V loops show threshold switching at a much smaller voltage range (<1.5 V) due to the electrical MIT of VO₂. The I - V curve shows clear hysteretic behavior for both positive and negative polarities with the hysteresis loops being pinched at the origin, as shown in Figure 2d (red curve). The resistance decreases by ~ 10 times as the device switches from the HRS to LRS, which is higher as compared to the resistance change during the thermally triggered MIT before forming. Thus, the magnitude of the MIT as defined by the ratio of the HRS and LRS currents is significantly affected by the forming process. A clear distinction between I - V curves before and after the forming process is observed, as shown in Figure 2d, in which the hysteresis is not present before forming and the base current is nearly 17 times less than the HRS current after forming at the same bias voltage. However, the forming process in our device is achieved without applying a compliance current (CC) limit, i.e., the self-compliance effect, which could be due to the conductivity limit of the LSMO bottom electrodes. The self-

compliance effect in a memristive device is an attractive feature as it eliminates the need for external current-limiting circuits.

Figure 3 shows the volatile and nonvolatile RS of the Au/VO₂/LSMO device. After forming the device with a high positive voltage sweep (0 to 4 V), a perfectly reversible and reproducible I - V hysteresis is obtained because of the MIT of VO₂, as shown in Figures 3a and S4. Such a RS is independent of the voltage polarity and requires a low threshold voltage of <1.5 V to switch from the HRS to LRS. The device remains in the LRS until the applied bias is higher than the holding voltage (V_{hold}). However, when the voltage is reduced to less than V_{hold} , the device instantly switches to the HRS, indicating a volatile mode of RS. Upon repeating the I - V hysteresis measurements up to one hundred consecutive cycles, a minor shift in V_{th} and V_{hold} toward a lower voltage is observed, likely due to the remaining residual heat from the previous cycles (Figure S5). The volatile RS properties were further confirmed by pulsed mode measurements with a write/read pulse voltage of $2.5/1$ V, as shown in Figure 3b. Thus, this mode of RS can be implemented to construct spiking neurons such as leaky integrate and fire (LIF) and adaptive-LIF.^{29–31} Interestingly, the same device exhibits polar and nonvolatile RS with a voltage sweep of -4 V $\rightarrow$ 0 V $\rightarrow$ 4 V, as shown in Figure 3c. As mentioned earlier, the positive voltage sweep from 0 to 4 V sets the device to the LRS, whereas the device resets to the HRS when a negative voltage sweep from 0 to -4 V is applied. The RS under nonvolatile mode is also found to be stable and repeatable, as confirmed by repeated DC sweeping (Figure 3c) and pulsed mode (Figure S6) measurements from -4 to 4 V.

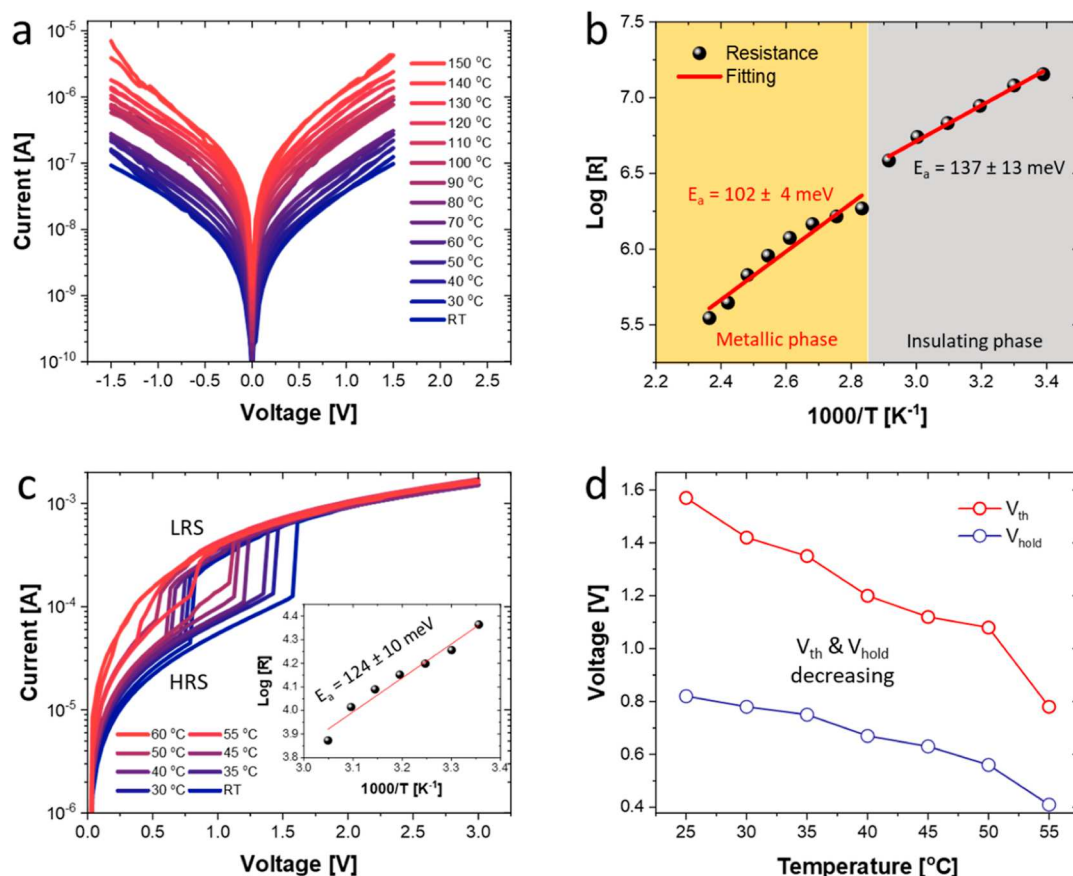


Figure 4. Temperature-dependent I – V response of the Au/VO₂/LSMO heterostructure device. (a) I – V curves at different temperatures before forming. (b) Corresponding R – T plot used for the extraction of activation energies. (c) I – V curves at different temperatures after forming. The inset shows the R – T plot under the HRS. (d) Summary of the threshold voltage (V_{th}) and holding voltage (V_{hold}) with respect to the temperature.

Under this voltage range, the overall switching is contributed by the VO₂/LSMO interface switching and the MIT of VO₂. However, the signature of the MIT tends to disappear with repeated voltage sweeping, giving rise to a gradual change in current in the MIT region. This can be correlated to heat accumulation during repeated measurement, which may prevent VO₂ from completely transitioning back to the insulating phase. Regardless, the resistance states under this RS mode are found to be stable with an On/Off ratio greater than 10^3 , as confirmed by the pulsed measurement in Figure 3d. Thus, this mode of RS can also be used to emulate synaptic properties.

Figure 4 shows the temperature-dependent study of the Au/VO₂/LSMO device at ambient conditions for which the device was attached to the heating stage. The device was measured at different temperatures before and after the electrical forming process. The temperature-dependent I – V curves of the device before forming are shown in Figure 4a. For this, a low voltage range of $-1.5 \rightarrow 0 \rightarrow 1.5$ V was used to prevent undesired forming of the device during measurement. As seen in Figure 4a, the current (resistance) gradually increases (decreases) with increasing temperature from room temperature up to 60 °C. When the temperature rises above 70 °C, an abrupt increase in current is observed due to the MIT of the VO₂.^{25,26} These measurements were used to extract the activation energy (E_a) and thermally activated conduction mechanism, as shown in Figure 4b. The temperature-dependent resistance of the device can be expressed as^{25,32}

$$\log[R] = R_0 + E_a/kT$$

where R_0 is the resistance at room temperature, k is the Boltzmann constant, and T is the temperature. The linear slope of the Arrhenius plots ($\log[R]$ vs. $1000/T$) provides the value of E_a , which is estimated to be 137 ± 13 and 102 ± 4 meV for the insulating and metallic states, respectively. The estimated E_a in our sample slightly differs from previously reported E_a for phase pure VO₂ films (230–250 meV in insulating and 80–90 meV in metallic states).³³ Specifically, we have noticed that the E_a insulating phase is slightly smaller, whereas the metallic-state E_a is slightly larger as compared to the previously reported values.^{25,33} This likely may be due to the presence of off-stoichiometric VO₂ in the thin film, as well as the presence of oxygen vacancies and the thermionic barrier at the VO₂/LSMO interface. A similar trend in E_a was observed previously in off-stoichiometric VO₂ films. Furthermore, we studied the temperature dependent I – V characteristics after forming the device with a $0 \rightarrow 4$ V sweep in Figure 4c. The corresponding values of V_{th} and V_{hold} are summarized in Figure 4d. The V_{th} and V_{hold} decrease from ~ 1.58 to 0.8 V and ~ 0.8 to 0.4 V, respectively, as the temperature increases from room temperature to 55 °C. It is also observed that the HRS current gradually increases with respect to temperature, while the LRS current remains similar. This indicates the semiconducting or highly resistive nature of VO₂ in the HRS and its metallic-like nature in the LRS. Once the temperature increases above 60 °C, VO₂ in the device becomes metallic with a linear (Ohmic) I – V relationship throughout the voltage range. The insulating

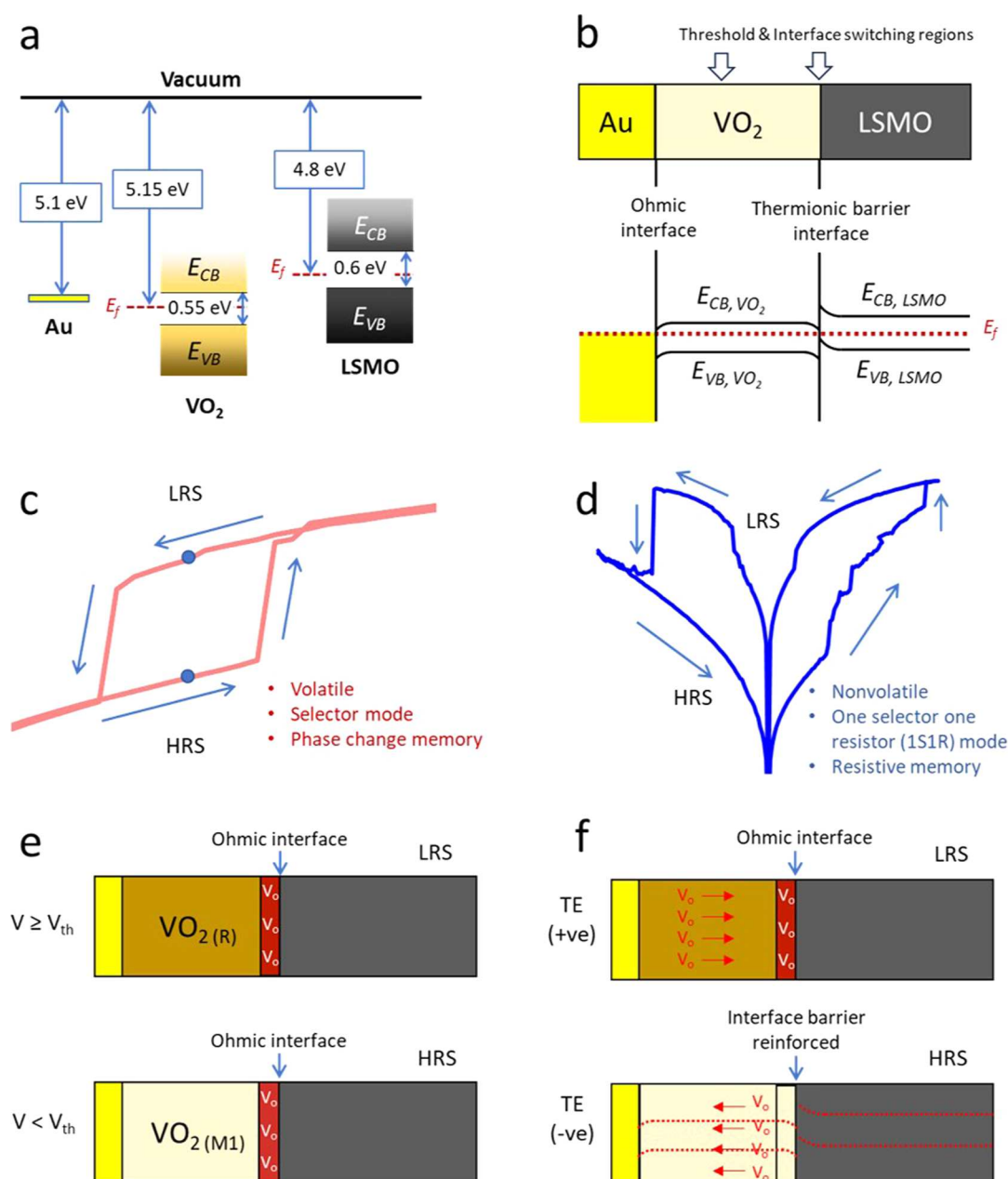


Figure 5. Energy band alignment of Au/VO₂/LSMO (a) before contact and (b) after contact. Two modes of RS: (c) volatile-type and (d) nonvolatile type. Schematic illustrations of switching mechanisms under (e) volatile and (f) nonvolatile modes.

phase E_a is extracted to be 124 ± 10 meV, which is less than that of the device before forming. This further indicates that the VO₂/LSMO interface barrier plays an important role in controlling the conduction mechanism of our device.

Figure 5 illustrates the possible mechanisms for dual RS modes in the Au/VO₂/LSMO devices. First, we analyzed the energy band alignment of different material layers before and after contact, as shown in Figure 5a,b. The Au/VO₂ interface is intrinsically ohmic as the work function of VO₂ (5.15 eV) is close to that of Au (5.10 eV).³⁴ In the case of the VO₂/LSMO bottom interface, an interfacial barrier and a depletion region may exist because of the work function difference $\Delta E_f = 0.35$ eV, as shown in Figure 5b,³⁵ which is primarily responsible for these two switching modes in our devices. When a positive voltage is applied to the top electrode, oxygen vacancies (V_o) in the VO₂ thin films are pushed to the bottom interface. When

the bias voltage reaches above the critical limit (~ 4 V), the thermionic barrier between the VO₂ and LSMO interface collapses. In a recent report on the role of V_o on work function, it was shown that oxygen-deficient VO₂ can exhibit a work function as low as 4.40 eV.³⁶ Thus, by pushing more V_o toward the bottom interface, the Fermi level of VO₂ can be lifted to match the Fermi level of LSMO. Furthermore, it has been reported that the oxygen stoichiometry in VO₂ films can be modulated by an electric field such that the positive bias removes oxygen ions and creates more oxygen defects, making VO₂ more conducting, whereas the inverse effect can be achieved with a negative bias.³⁷ The device remains in the LRS until a negative bias (-4 V) is applied, which attracts V_o toward the top electrode and reinforces the interface barrier between VO₂ and LSMO. This process resets the device back to its original HRS. To realize threshold switching, i.e., volatile

Table 1. Summary of the Recently Reported Volatile and Nonvolatile Memristive Devices

device structure	switching type	volatile/nonvolatile control mechanism	selector (volatile) mode		memory (nonvolatile) mode		1S1R
			cycles	on/off	cycles	on/off	
Ni/SiO ₂ /Pt ³⁸	filamentary	compliance current (CC)	10	10	14	100	no
Pt/Ag/SiO _x /Pt ³⁹	filamentary	CC	20	10 ⁶	20	10 ⁶	no
Ag/TaO _x /TiN ⁴⁰	filamentary	CC	100	14.3	100	73.2	no
Pt/TaO _x /TiN ⁴¹	filamentary	CC	20	10 ³		100	no
Ag/CuInSe ₂ /Mo ⁴²	filamentary	CC	400	10 ⁴	160	10 ⁵	no
Ag/AlZS/Cs ₃ Cu ₂ Cl ₅ /W ⁴³	filamentary	CC	65	10 ⁴	400	100	no
Pt/TaO _x /Pt/Ag/TaO _x /Ag ⁴⁴	filamentary	CC	10	100	100	10 ¹⁰	yes
Pd/Ag/HfO _x /Ag/Pd/TaO _x /Ta ₂ O ₅ /Pd ⁴⁵	filamentary	filament in the RS layer	10 ⁸	10 ¹⁰			yes
V/VO _x /HfWO _x /Pt ¹⁷	phase change	filament in the RS layer	10 ¹²	100	10 ¹⁰	10 ³	yes
TiN/TiO ₂ /NbO _x /Pt ¹⁸	phase change	filament in the RS layer		50	100	100	
Au/VO ₂ /LSMO (this work)	phase change	interface (self-compliance)	300	10	1500	10 ³	yes

RS, the device needs to be biased with a smaller voltage (after the forming with a large bias of 4 V) that is just enough to induce the electrical MIT of VO₂ by Joule heating. The volatile RS is nonpolar and symmetrical, which could be attributed to the formation of ohmic contacts at both the top and bottom interfaces. Finally, we compared the Au/VO₂/LSMO device with recently reported memristive devices with volatile and nonvolatile RS properties in Table 1. The first six rows in the table show examples of filamentary-type devices in which a CC is used to regulate the volatile and nonvolatile switching modes. The memory type of these devices relies on the strength of filament formation during the set process. Specifically, a higher CC promotes robust filament formation, leading to nonvolatile memory, whereas a lower CC induces partial/weak filament formation and, thus, volatile memory. However, these memristive devices could not be concurrently switched in both volatile (as a selector) and nonvolatile (as a resistor) modes to achieve the 1S1R operation that is required in large memristive crossbar arrays. An alternative approach has been reported in which both the volatile and nonvolatile memristor components are integrated within a single cell to attain 1S1R functionality (rows seven to ten in the table). These devices often require a complicated sequence of programming pulses because individual components need to be set to attain the 1S1R operation. Furthermore, combining multiple filamentary-type devices could be challenging from the fabrication and large-array integration perspective. In this context, the device architecture we propose presents a novel approach to realize 1S1R operation by leveraging interfacial and MIT properties. By tuning the negative voltage at the LRS, the device can be set in two different HRS modes, as shown in Figure S7. This design not only simplifies device operation but also may offer practical advantages such as simple device fabrication for large-area integration and energy-efficient training of neural networks with fewer programming pulses.

3. CONCLUSIONS

In summary, a reconfigurable memristor of the Au/VO₂/LSMO configuration is demonstrated to exhibit the volatile and nonvolatile RS modes depending on the magnitude of the applied electric field. The device requires a bipolar high voltage sweep of −4 to 4 V to set and reset the nonvolatile mode, and it is dominated by the interface between VO₂ and LSMO. However, the volatile mode requires a low threshold voltage of ∼1.5 V, and the RS is dominated by the MIT of VO₂. The RS mechanism is discussed based on the formation and collapse of

the thermionic barrier between the VO₂ and LSMO interface accompanied by the MIT of the VO₂ phase. As a result of the coexistence of both RS modes in a single device, it can operate as a neuron as well as a synapse in artificial neural networks. From a broader perspective, such memristive devices can also provide advantages over the size and energy constraints of the existing fully memristive neural networks. Thus, this work provides a new strategy to realize a memristive system that can combine fundamental neural activities with a simple hardware design.

4. EXPERIMENTAL SECTION

The VO₂/LSMO bilayer thin films were grown on *c*-plane Al₂O₃ (0001) single-crystal substrates (MTI Corp.) by using pulsed laser deposition (PLD). The chamber base pressure prior to PLD growth was 3 × 10^{−7} Torr. First, an LSMO layer was deposited on Al₂O₃ (0001) at 750 °C under an oxygen partial pressure of 100 mTorr. After the LSMO deposition, the substrate temperature was ramped down to 500 °C at 10 °C/min and held for 10 min. Subsequently, the VO₂ deposition was carried out at 500 °C without breaking the vacuum. During the VO₂ deposition, the oxygen partial pressure was maintained at 10 mTorr and kept the same until the temperature was reduced to 100 °C at 10 °C/min after VO₂ deposition. Stoichiometric La_{0.7}Sr_{0.3}MnO₃ and V₂O₅ ceramic targets were ablated with a KrF excimer laser at a laser fluence of 2 J/cm² and at a laser repetition rate of 4 and 2 Hz for LSMO and VO₂ deposition, respectively. The target and substrate were rotated during deposition to improve the thickness uniformity with a target-substrate distance of 5.5 cm.

To confirm the phase and crystallinity of the as-deposited thin films, XRD was performed using a Rigaku SmartLab with a wavelength of 1.5408 Å. Scanning electron microscopy (SEM) (Apero, Thermo Scientific) was used to image the surface of the thin films and devices. Cross-sectional transmission electron microscopy (TEM) samples were prepared by a standard focused ion beam (FIB) lift-out process on a FEI Helios 600 dual beam SEM/FIB with a Ga⁺ ion source operated at 30 kV. A FEI Titan 80-300 S/TEM with an image-corrector operated at 300 keV was used. For the device characterization, Au top electrodes of ∼100 nm thickness were deposited using e-beam evaporation. The size of Au top electrodes was defined by a prepatterned shadow mask. Electrical transport measurements were performed with Keithley 2636B source measure units in an ambient environment (relative humidity <20%) with the bias applied on the top Au disks and the LSMO layer grounded, i.e., two probe mode. The Linkam HFS600E-PB4 probe station was used for in situ temperature-dependent measurements.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.3c19032>.

XRD (2θ – ω) spectra, SEM images, and supporting current–voltage (I – V) characteristics (PDF)

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Notes

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