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PAPER

Power efficient MoS_2 synaptic devices based on Maxwell–Wagner interfacial charging in binary oxides

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Abstract

Synaptic devices with tunable weight hold great promise in enabling non-von Neumann architecture for energy efficient computing. However, conventional metal-insulator-metal based two-terminal memristors share the same physical channel for both programming and reading, therefore the programming power consumption is dependent on the synaptic resistance states and can be particularly high when the memristor is in the low resistance states. Three terminal synaptic transistors, on the other hand, allow synchronous programming and reading and have been shown to possess excellent reliability. Here we present a binary oxide based three-terminal MoS_2 synaptic device, in which the channel conductance can be modulated by interfacial charges generated at the oxide interface driven by Maxwell-Wagner instability. The binary oxide stack serves both as an interfacial charge host and gate dielectrics. Both excitatory and inhibitory behaviors are experimentally realized, and the presynaptic potential polarity can be effectively controlled by engineering the oxide stacking sequence, which is a unique feature compared with existing charge-trap based synaptic devices and provides a new tuning knob for controlling synaptic device characteristics. By adopting a three-terminal transistor structure, the programming channel and reading channel are physically separated and the programming power consumption can be kept constantly low (∼50 pW) across a wide dynamic range of 10^5. This work demonstrates a complementary metal oxide semiconductor compatible approach to build power efficient synaptic devices for artificial intelligence applications.

1. Introduction

Conventional von Neumann computing paradigm is becoming increasingly inefficient in terms of speed and energy for data-intensive artificial intelligence applications, due to the physical separation of logic units and memory units [1–3]. Biological neural networks with an extreme-parallel architecture have constantly inspired new computing hardware, such as artificial neuron network (ANN), for in-memory computing [4–9]. Electrical signals in biological neurons originate from the exchange of charges across the plasma membrane through ion channels [10, 11]. The neuron membrane potentials can be effectively modulated by a transmembrane influx of ionic charges [12, 13], such as Na^+ and K^+. The powerful computational capabilities of neurons are achieved through controllable movement of these transmembrane charges. On the other hand, the most prevalent device structure to implement ANN is a two-terminal filament based memristor, typically made of metal-insulator-metal (MIM) structures [6, 14–23]. Anodic oxides [22, 24–33], (e.g. HfO_2, TiO_2, Ta_2O_5, MoO, WO, NiO, etc) have been widely exploited as

resistive switching media due to their good stability, retention and endurance performance. As atomically precise materials, a wealth of 2D materials have also been extensively studied as resistive switching medium to build memristors [34–47], including hexagonal boron nitride [35, 45], transition metal dichalcogenides [37, 48, 49], MXenes [39, 40], transition metal carbides [41, 50], and nitrides [51], among many others. These MIM memristors operate in different mechanisms than their biological counterparts, i.e. creation and rupture of conductive filaments [22]. Their synaptic weight is associated with the conductivity of two-terminal MIM channels, which can be continuously modulated by controlling the number of conductive filaments. The two-terminal design allows a crossbar array structure with compact footprint and cost-effectiveness [52]. However, the filament based memristor design is also embodied with limitations. Due to their two-terminal design, the programming and reading processes cannot be done simultaneously. This fails to faithfully emulate a natural synaptic response and adds to the complexity in the peripheral circuitry to control and coordinate learning and readout [30, 52]. In addition, in a two-terminal memristor, its writing power strongly depends on the channel conductance and can be quite high when the MIM channel is in the low resistance state (LRS) [6, 52]. To address these challenges, three-terminal synaptic transistors have been proposed and investigated. For instance, electrochemical 'iontronic' transistors use movable alkali metal ions to transport through a gel electrolyte for channel gating and to emulate biological synapses [53–55]. However, this approach is not complementary metal oxide semiconductor (CMOS) compatible due to the use of alkali metal ions. Being atomically thin, 2D semiconductors provide an excellent solid-state platform to develop synaptic transistors for neuromorphic applications [47, 56]. So far, researchers have mainly relied on the charge traps near 2D material surface or bulk trap states inside dielectric insulators to modulate the 2D channel conductivity [29, 57–60]. However, these charge traps are essentially random and difficult to control in terms of their location and polarity, which in turn limit critical device characteristics such as dynamic range of synaptic weight change and power consumption, etc.

Here we exploit the interfacial charges in a binary oxide (AlO_x/SiO_x) structure driven by Maxwell-Wagner instability to demonstrate an interfacial charge gated synaptic (ICGS) device, which adopts a three-terminal structure and uses MoS_2 as the channel material. Maxwell-Wagner instability is a well-studied mechanism of interfacial charge trapping in silicon CMOS devices with binary oxides as dielectrics [61–63]. Unlike the filament-based two terminal structure, we adopt a three terminal structure to decouple the writing channel from the resistive switching channel (figure 1(a)), which allows a constantly low writing power (∼50 pW) as the MoS_2 channel conductance. The channel conductance represents the synaptic weight of the artificial synapse and varies across five orders of magnitude. The binary oxide stack serves both as an interfacial charge host and gate dielectric. Gate voltage pulses, playing a similar role as the pre-synaptic action potentials, can effectively control the polarity and number of interfacial charges. Since the MoS_2 channel is atomically thin, the induced interfacial charges hold tight electrostatic control over the MoS_2 surface potential and result in synaptic weight adjustment over a wide dynamic range of 10^5. Control experiments confirm that the large tunability contributes from the interfacial trap states between binary oxides, instead of bulk trap states inside individual oxide layers. Importantly, we experimentally demonstrate that the excitatory and inhibitory polarity can be effectively switched by changing the binary oxide stacking sequence, which is a key feature of Maxwell-Wagner instability driven interfacial charging effect [61, 62, 64]. By controlling the amount and polarity of interfacial charges, the surface potential of the MoS_2 channel respond sensitively and results in synaptic weight adjustment, emulating the change of post-synaptic membrane potential through the bonding of neurotransmitters [13, 65]. Our approach presents a CMOS compatible method to build biorealistic memristors with ultralow power consumption.

2. Results and discussion

A binary oxide stack (10 nm AlO_x/10 nm SiO_x) was sequentially deposited on top of a doped Si substrate by atomic layer deposition (ALD) (figure 1(a)). The channel areas of the synaptic device were defined by electron beam lithography (EBL) using few-layer MoS_2 as the channel material (figure 1(b)). Details can be found in the section 4. We fabricated a dozen of ICGS devices with a channel length of 0.5 μm and channel width ranging from 5 to 10 μm. The optical microscopy image of a typical MoS_2 ICGS device is shown in figure 1(b). A train of pre-synaptic voltage pulses with an amplitude of 4 V and duration of 1 s is applied to the backgate. The post-synaptic current flowing through the MoS_2 channel is monitored during the process with a 10 mV drain bias (figure 1(a)). The experimental results show that positive pulses lead to effective depression (figure 2(a)). MoS_2 ICGS devices are selected with an initial channel current of ∼1 μA under zero gate bias. When a positive pulse (amplitude: +4 V; duration: 1 s) is applied to the backgate terminal, the channel current decreases during the pulse period. The inhibitory postsynaptic current is shown in figure 2(a). After the pulse is removed, the channel current drops to a lower value under zero gate bias than its initial current, exhibiting memory effects. Subsequent positive pulses cause

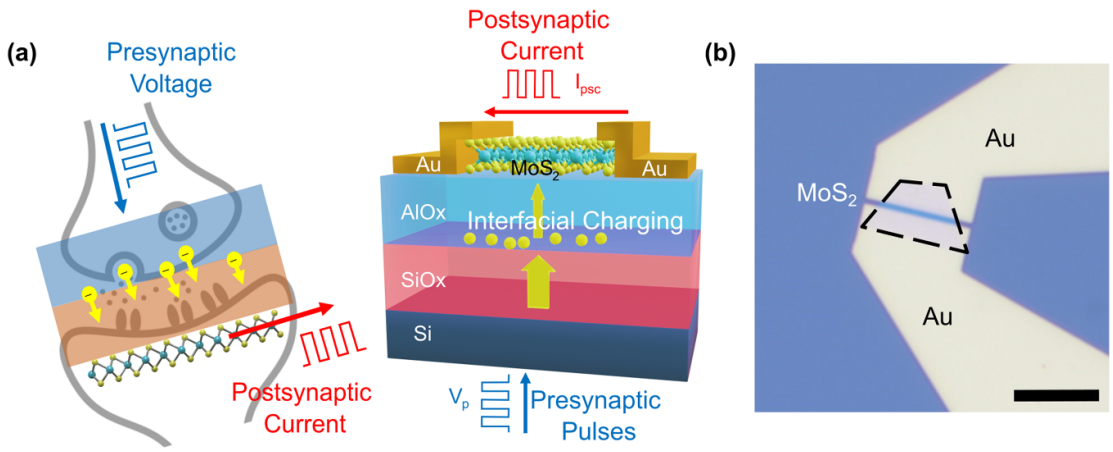

Figure 1. (a) Left: analogy with biological synapses. Right: schematic illustration of a three-terminal synaptic device with few-layer MoS_2 as the channel material on top of a stack of binary oxides (10 nm AlO_x/10 nm SiO_x). The substrate is heavily doped silicon. Pre-synaptic pulses are applied to the backgate Si substrate. The post-synaptic current flowing through the MoS_2 channel is measured. (b) An optical image of a typical MoS_2 synaptic device. Scale bar: 10 μm.

similar depression effects. The MoS_2 channel current under zero gate voltage decreases from ~1 μA to ~10 pA after 15 consecutive positive pulses applied to the backgate, achieving a dynamic resistive switching range of ~10^5. As shown in figure 2(b), negative pulses lead to effective potentiation in the MoS_2 ICGS device. The MoS_2 channel current is initialized to be about 500 pA and a train of negative pulses (amplitude: −4 V; duration: 1 s) is subsequently applied to the backgate. During the negative pulse, the MoS_2 channel current is reduced due to the N-type characteristics of MoS_2. However, after the negative pulse is removed, the channel current increases to about 1 μA under zero backgate bias. Subsequent negative pulses will lead to saturation in the channel current. The excitatory postsynaptic current is shown in figure 2(b). By reducing the duration of voltage pulses, the channel conductance of the MoS_2 ICGS device can be adjusted continuously both for potentiation and depression. As shown in figures 2(c) and (d), gradual decrease/increase of channel conductance is observed when a series of voltage pulses with a duration of 80 ms and an amplitude of +4 V/−4 V is applied. The synaptic weight, i.e. the channel conductance, can be further modulated by tuning pulse amplitude and duty cycle. As we increase the pulse amplitude from 2 V to 6 V, both inhibitory and excitatory synaptic weight tuning can be enhanced (figures 3(a) and (b), duty cycle is fixed at 60%). Similarly, as we increase the duty cycle from 20% to 80%, both inhibitory and excitatory synaptic weight tuning can be enhanced (figures 3(c) and (d), pulse amplitude is fixed at 4 V). For depression, the synaptic weight change saturates when the duty cycle exceeds 60%.

To better understand the resistive switching mechanism of the binary oxide based ICGS device, we also fabricate two groups of MoS_2 devices with 10 nm AlO_x only and with 10 nm SiO_x only as dielectric layers, respectively, for control experiments. The single oxide layer of AlO_x and SiO_x is deposited using the same ALD parameters as for the binary AlO_x/SiO_x dielectric layers. As shown in figures S1(a) and (b), the resistive switching behaviors in the AlO_x only and the SiO_x only device are negligible compared with binary oxide counterpart devices under the same pulse schemes. During the comparison test, the pulse duration is kept the same for all devices under test and the pulse amplitudes are adjusted to guarantee the same electric field strength generated for AlO_x, SiO_x and AlO_x/SiO_x dielectric layers. These results indicate the impact of bulk trap states inside the individual AlO_x and SiO_x dielectric layers is negligible. We attribute the strong excitatory and inhibitory effects to the interfacial charges generated near the binary oxide interface when the voltage pulses are applied, and the interfacial charges can electrostatically gate the MoS_2 channel and modulate its channel conductance over a wide dynamic range. Another important feature of the binary oxide ICGS devices is that the excitatory and inhibitory polarity can be switched by changing the oxide stacking sequence. As shown in figure 4, we experimentally found that, in the MoS_2/SiO_x/AlO_x/Si ICGS device, positive pulses result in potentiation and negative pulses lead to depression, which is opposite as the MoS_2/AlO_x/SiO_x/Si counterpart devices.

The generation of interfacial charging at the binary oxide interface can be explained by the Maxwell-Wagner instability theory. The Maxwell-Wagner instability is a widely found phenomenon in almost all binary dielectric systems with different compositions, such as silicon metal-oxide-semiconductor (MOS) and metal–nitride–oxide–silicon structures [61–63]. It was first discovered by Maxwell [66] in the 19th century and later investigated by Wagner [67]. Two layers of oxides with different compositions

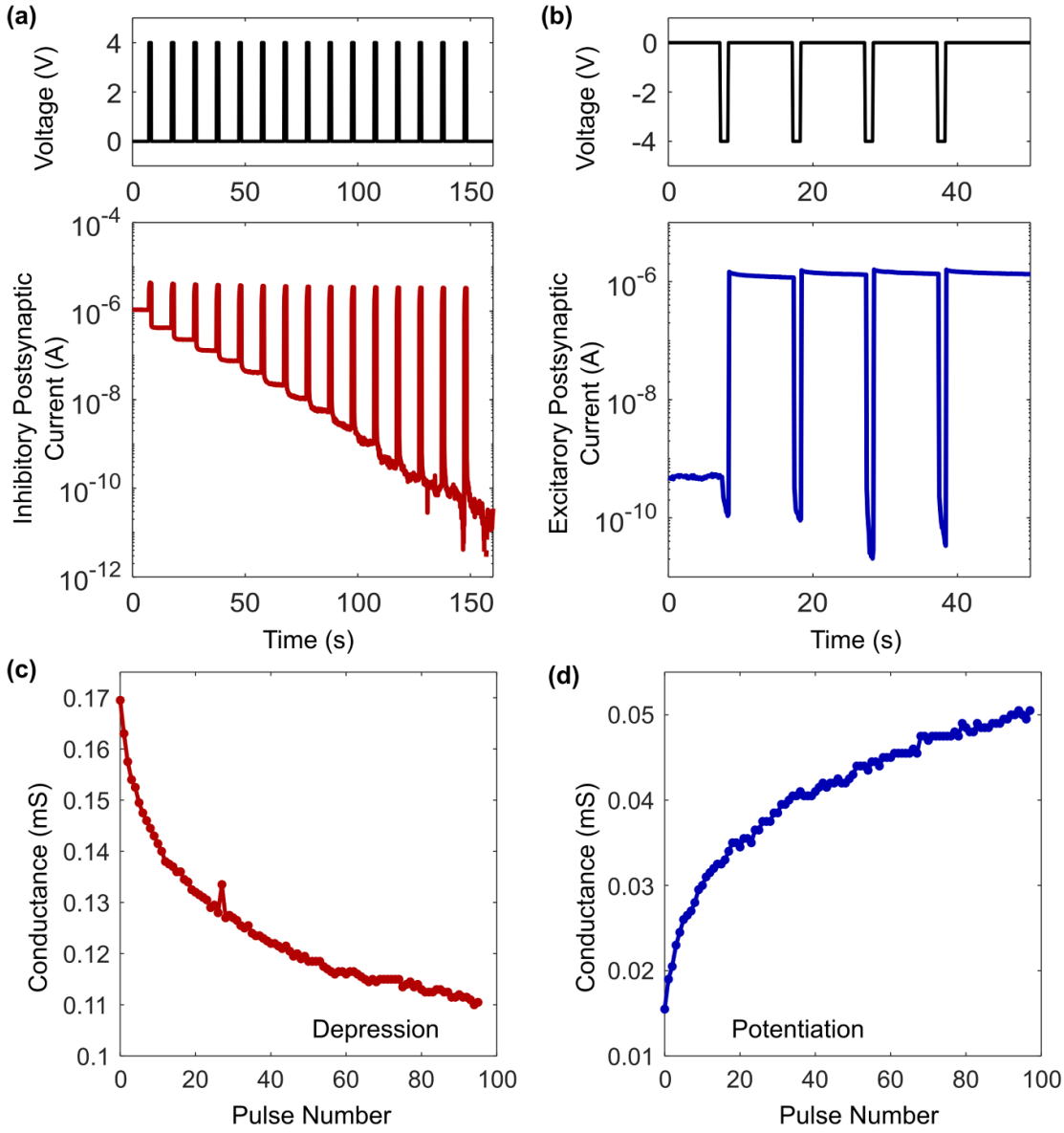

Figure 2. (a), (b) Transient current response in the MoS_2 channel when a train of pulses with amplitude of +4 V (a) and −4 V (b) is applied to the backgate terminal. The pulse duration for (a) and (b) is 1 s. The dwell time between two consecutive pulses is 9 s. Pulse frequency: 0.1 Hz. (c), (d) MoS_2 channel conductance as a function of pulse number. Pulse duration: 80 ms. Pulse frequency: 10 Hz. Pulse amplitude: +4 V (c) and −4 V (d). Both potentiation and depression can be achieved by controlling the pulse voltage polarity.

generally have different conductivities. Under a bias across a stack of binary oxides, there can be a discontinuity in current density across the interface between the two oxide layers, causing interfacial charges to accumulate. Figure 5(a) illustrates the charge distribution across the $MoS_2/AlO_x/SiO_x/Si$ gate stack under a positive presynaptic pulse V_p. The σ_{SiO_x} and σ_{AlO_x} represent the surface charge density of the SiO_x and AlO_x layers due to dielectric polarization, respectively. The σ represents the interfacial charge density accumulated at the SiO_x/AlO_x interface. The Q_1 and Q_2 are the charges accumulated at the two terminals of the gate capacitor. In steady state, the system should reach charge neutrality, so that $Q_1 + \sigma A - Q_2 = 0$, where A denotes the device area. Based on Gauss's law, the electric fields in the two dielectrics are given by

$$E_{SiO_x} = \frac{\frac{Q_1}{A} - \sigma_{SiO_x}}{\epsilon_0} \quad (1)$$

$$E_{AlO_x} = \frac{\frac{Q_2}{A} - \sigma_{AlO_x}}{\epsilon_0} \quad (2)$$

respectively, where ϵ_0 is the vacuum permittivity. The pulse voltage V_p can be calculated as $V_p = d_{AlO_x}E_{AlO_x} + d_{SiO_x}E_{SiO_x}$, where the d_{AlOx} and d_{SiOx} are the thickness of AlO_x and SiO_x layers, respectively.

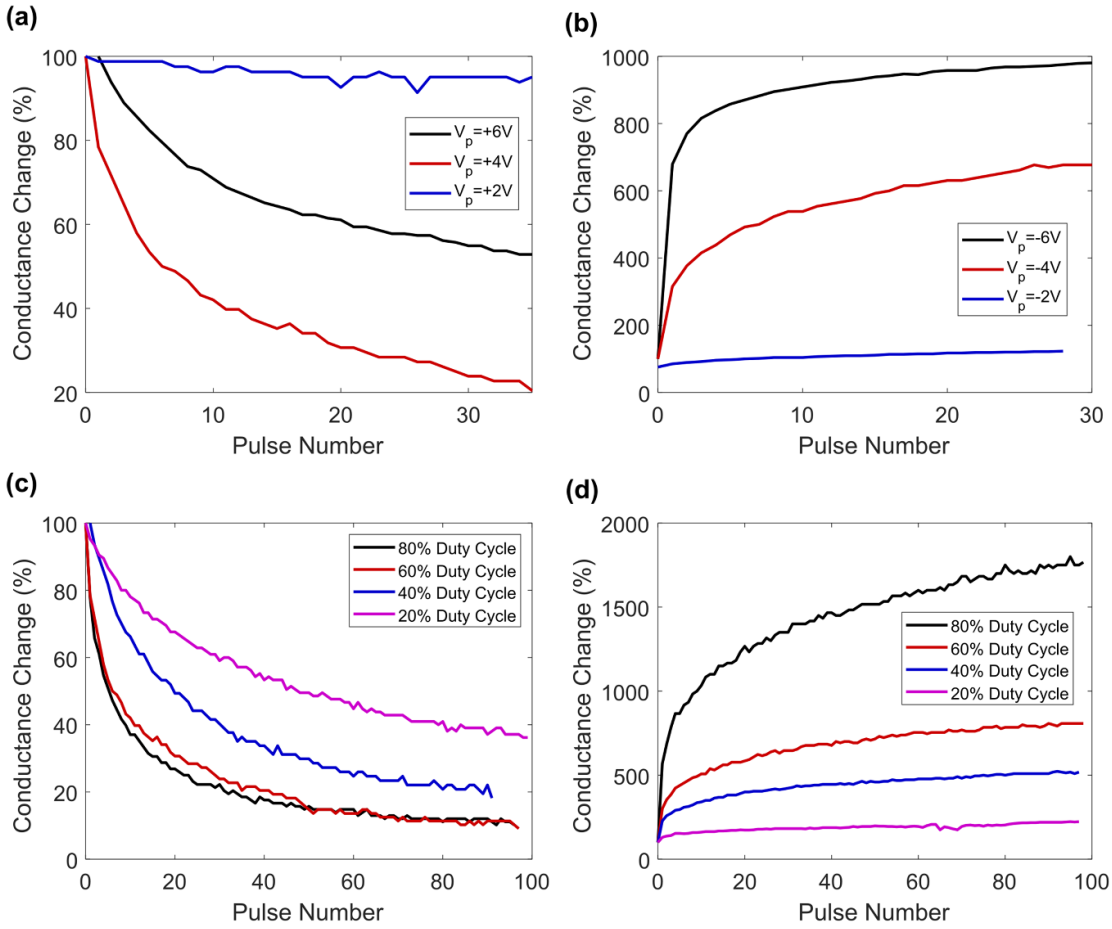

Figure 3. Dependency of synaptic weight update on voltage pulse amplitude and duty cycle. (a) Synaptic weight change as a function of inhibitory pulse number with different pulse amplitudes (blue: +2 V; red: +4 V; black: +6 V). Pulse frequency: 10 Hz. Pulse width: 60 ms. The gap between two adjacent pulses is 40 ms, i.e. the duty cycle is 60%. (b) Synaptic weight change as a function of excitatory pulse number with different pulse amplitudes (blue: −2 V; red: −4 V; black: −6 V). Pulse frequency: 10 Hz. Duty cycle: 60%. (c)-(d) Synaptic weight update as a function of inhibitory (c) and excitatory (d) pulse number with different duty cycles. Pulse amplitude: +4 V (c) and −4 V (d). Pulse frequency is 10 Hz for both (c) and (d).

Assuming that the dielectric polarization is linearly proportional to the electrical field, the surface charge density can be expressed as $\sigma_{\mathrm{SiO}x} = \epsilon_0 \chi_{\mathrm{SiO}_x} E_{\mathrm{SiO}_x}$ and $\sigma_{\mathrm{AlO}x} = \epsilon_0 \chi_{\mathrm{AlO}_x} E_{\mathrm{AlO}_x}$, where χ represents the corresponding dielectric susceptibilities. From the above equations, we can obtain the number of interfacial charges per unit area as

$$\begin{aligned}\sigma &= \epsilon_0 \left(1 + \chi_{\mathrm{AlO}_x}\right) E_{\mathrm{AlO}_x} - \epsilon_0 \left(1 + \chi_{\mathrm{SiO}_x}\right) E_{\mathrm{SiO}_x} \\ &= \epsilon_0 \left(\epsilon_{\mathrm{AlO}_x} E_{\mathrm{AlO}_x} - \epsilon_{\mathrm{SiO}_x} E_{\mathrm{SiO}_x}\right) \end{aligned} \quad (3)$$

where $\epsilon_{\mathrm{AlO}_x}$ and $\epsilon_{\mathrm{SiO}_x}$ being the relative permittivity of SiO_x and AlO_x, respectively. As a result, the polarity and quantity of the Maxwell-Wagner instability induced interfacial trapped charge depend on the permittivity and the strength of electrical fields in the two dielectric layers. This makes the interfacial charge density to be controllable by engineering the oxide materials and tuning external pulses. Therefore, we can engineer the interfacial trap charges to be significantly larger than bulk trap states inside individual oxides.

With positive pulses applied, the MoS_2 channel conductance decreases (figure 2(b)). Given the N-type characteristics of MoS_2, it indicates that negative interfacial charges are generated under positive pulses. We can therefore deduce that the interfacial charge density $\sigma = \epsilon_0 \left(\epsilon_{\mathrm{AlO}_x} E_{\mathrm{AlO}_x} - \epsilon_{\mathrm{SiO}_x} E_{\mathrm{SiO}_x}\right) < 0$ (when $V_{\mathrm{p}} > 0$). Considering that the relative permittivity of ALD deposited AlO_x(∼8–9) [68] is larger than that of ALD deposited SiO_x (∼3.9) [68], the electric field in the AlO_x layer must be smaller than that in the SiO_x layer. This holds true when the pulse polarity switches to negative. According to the model, the polarization of the interfacial charge is inversed under negative gate voltage, i.e. $\sigma = \epsilon_0 \left(\epsilon_{\mathrm{AlO}_x} E_{\mathrm{AlO}_x} - \epsilon_{\mathrm{SiO}_x} E_{\mathrm{SiO}_x}\right) > 0$ (when $V_{\mathrm{p}} < 0$), leading to positive charge accumulation under negative pulses. Thus, we should expect an increase in the channel conductance for N-type MoS_2, which agrees

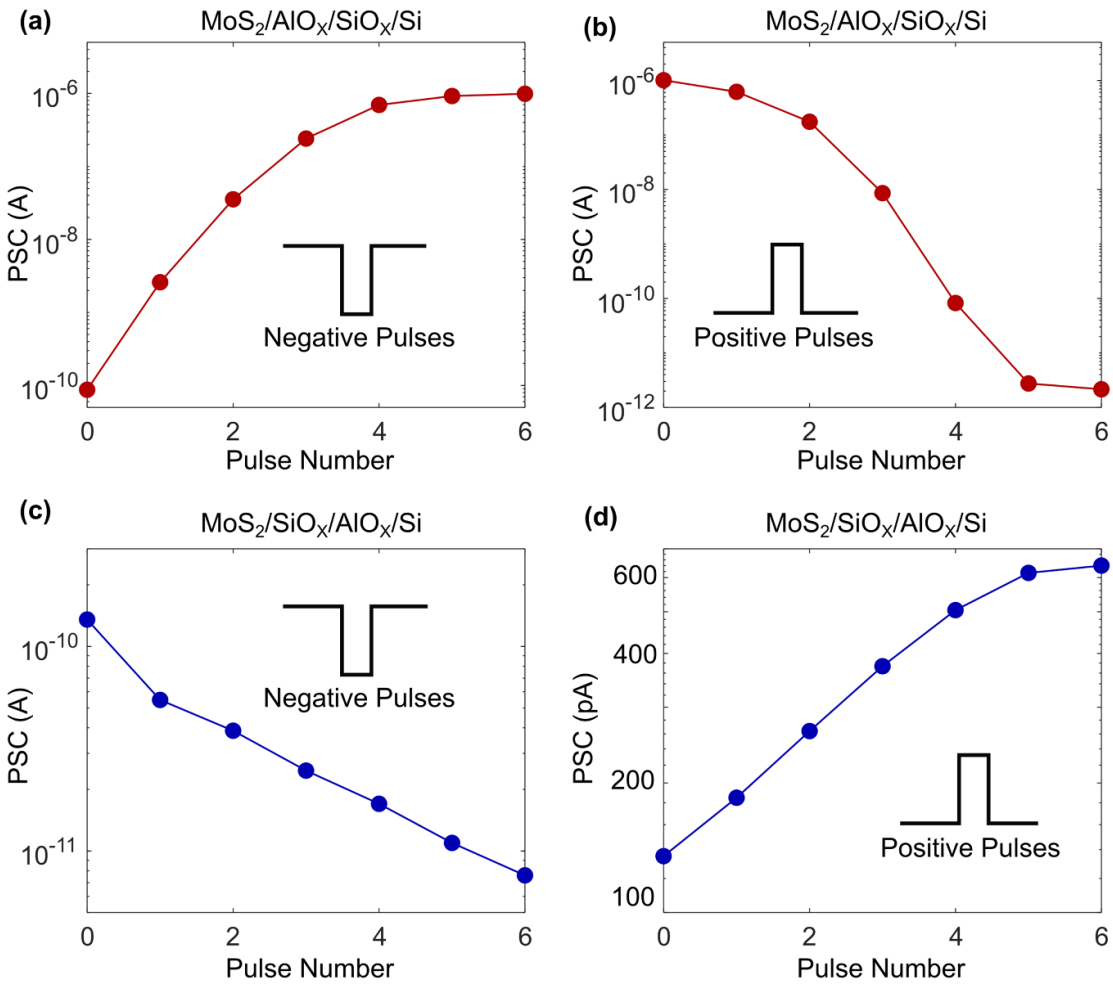

Figure 4. Performance comparison between MoS_2 ICGS devices with different oxide stacking orders. To reach the maximum dynamic range, six voltage pulses with 10 s duration and incremental pulse amplitudes are applied to the back gate terminal of each device. The amplitudes of the six voltage pulses start with 1 V with a step of 1 V. (a) (b) The MoS_2 channel current of a MoS_2/10 nm AlO_x/10 nm SiO_x/Si ICGS device as a function of gate pulse number during depression under negative pulses (a) and potentiation under positive pulses (b). (c), (d) The MoS_2 channel current of a MoS_2/10 nm SiO_x/10 nm AlO_x/Si ICGS device as a function of gate pulse number during depression under negative pulses (c) and potentiation under positive pulses (d). Different growth conditions of the dielectrics (e.g. substrate, surface roughness and composition) affect the deposition quality and thus the conductance of the dielectrics layers, which is believed to cause the difference in the dynamic range of the two devices.

well with our experimental data (figure 2(a)). Based on the model, if we reverse the stacking sequence of the binary oxide, the interfacial charge generated would become

$$\sigma^* = \epsilon_0 \left(\epsilon_{SiO_x} E_{SiO_x} - \epsilon_{AlO_x} E_{AlO_x}\right) \tag{4}$$

Consequently, positive σ^* would be generated under positive pulses, which should lead to increased channel conductivity. Negative σ^* would be generated under negative pulses, which should lead to decreased channel conductivity. That means the pulse polarity corresponding to potentiation and depression is expected to be reversed.

To experimentally verify this, we fabricate MoS_2 ICGS devices with a binary oxide stack of 10 nm SiO_x/10 nm AlO_x using the same ALD deposition parameters (i.e. AlO_x is deposited first and closer to the back gate). We found that these devices with reversed oxide sequence indeed exhibit opposite polarity in potentiation and depression processes compared to the original devices (figure 4). It further validates the Maxwell-Wagner instability model presented here. We also measured the programming current (i.e. dielectric leakage current) of the binary oxide based MoS_2 ICGS device and compared it with single oxide counterparts. As shown in figure 5(b), the dielectric leakage current remains constant (on the order of few pA) as the pulse gate bias increases in the single oxide devices. In the binary oxide device, however, the dielectric leakage current increases as the pulse gate bias increases, which indicates that a significant number of charges migrate in and out of the binary oxide stack and part of these charges can be trapped near the interface, as described by the Maxwell-Wagner model. This aligns well with both our model and the experimental data. The volatility of the ICGS device further supports the Maxwell-Wagner instability model. Maxwell-Wagner

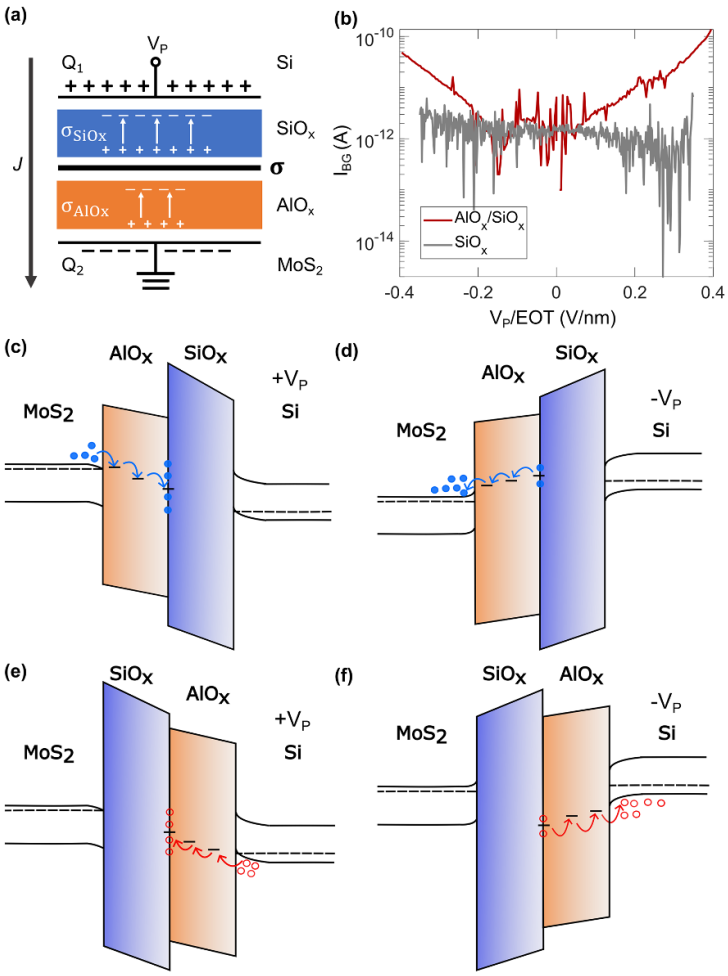

Figure 5. Net charge transport across the binary oxide stack. (a) Illustration of Maxwell-Wagner instability induced dielectric leakage current and interfacial charging in the $MoS_2/AlO_x/SiO_x/Si$ gate stack. (b) Dielectric leakage current measured in the $MoS_2/AlO_x/SiO_x/Si$ and $MoS_2/SiO_x/Si$ stacks under backgate bias. Positive value means current flowing from the Si gate to the MoS_2 channel, and vice versa. (c), (d) Band diagram of the $MoS_2/AlO_x/SiO_x/Si$ gate stack under positive (c) and negative (d) gate bias. The blue arrows indicate the electron transport direction. (e), (f) Band diagram of the $MoS_2/SiO_x/AlO_x/Si$ gate stack under positive (e) and negative (f) gate bias. The red arrows indicate the hole transport direction.

instability induced interfacial charges is supposed to exhibit time-dependent dynamics. The reason is that, at steady state with zero pulse bias applied, the dielectrics are no longer polarized and the electric fields inside oxides E_{SiO_x}, E_{AlO_x} will be zero. As a result, the interfacial charge $\sigma = \epsilon_0 (\epsilon_{AlO_x} E_{AlO_x} - \epsilon_{SiO_x} E_{SiO_x})$ will eventually relax to zero. Figures S2(a) and (b) confirm the time-dependent response of MoS_2 channel current after a negative and positive gate pulses are removed, respectively. To extract the time constant of this relaxation process, we measure the channel current in a 40 min period (supplementary information, figure S3) and the time constant is estimated to be 43.6 s.

The band diagrams in figures 5(c)–(f) can provide physical insights behind the excitatory and inhibitory effects of the binary oxide based MoS_2 ICGS devices. For the $MoS_2/AlO_x/SiO_x/Si$ stack under positive backgate pulses, a decrease in the channel conductivity indicates that there is negative charge accumulation at the interface that electrostatically gates the MoS_2 channel, contributed by electron injection from the MoS_2 channel to the oxide interface through trap-assisted tunneling. The trap-assisted tunneling process happens mainly through the AlO_x layer, probably because the trap states inside AlO_x are more than that in the SiO_x layer. A higher quality of ALD deposited SiO_x might originate from a better seeding on top of the silicon substrate. Given the thickness of oxide layers (10 nm AlO_x + 10 nm SiO_x) and the amplitude of pulses (i.e. 4 V), the direct tunneling current will be negligible. The net charge migration is illustrated in figure 5(c). Similarly, for the $MoS_2/AlO_x/SiO_x/Si$ stack under negative pulses, the band bending is in favor of electrons escaping from the interface traps to the MoS_2 channel through trap assisted tunneling (figure 5(d)). Therefore, the interfacial charge gating will enhance the channel conductivity. When the oxide stacking sequence is reversed, the charge transport is illustrated in figures 5(e)–(f). For the $MoS_2/SiO_x/AlO_x/Si$ stack under positive pulses, an increase in conductivity indicates that the dominating

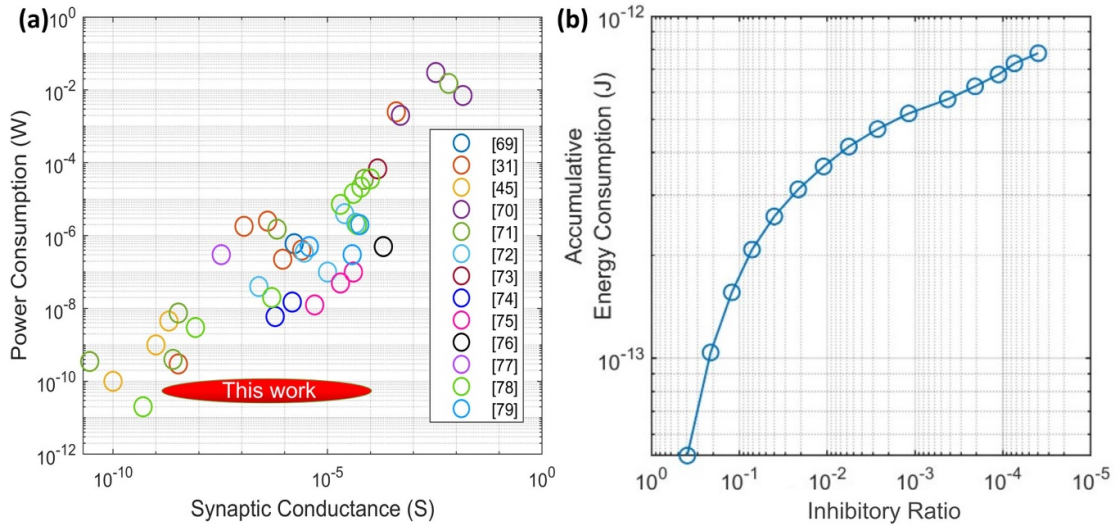

Figure 6. (a) Benchmark this work with state-of-the-art two-terminal memristive devices (open circles) in terms of programming power consumption at different synaptic conductance states. The literature data are from [31, 45, 69–79]. Each color represents a different reference. (b) The energy consumption of our synaptic device as a function of the inhibitory synaptic weight tuning ratio. The energy consumption is below 1 pJ as the synaptic weight is adjusted across ∼5 orders of magnitude.

charge transport is holes injected from the p-doped silicon substrate to the oxide interface due to trap-assisted tunneling through AlO_x (figure 5(e)). For the same stack order under negative pulses, the band bending is in favor of holes escaping from the oxide interface to the substrate and results in a reduced channel conductivity (figure 5(f)). We note that only the net charge accumulation paths are illustrated in figures 5(c)–(f).

Due to the separation of the programming channel (i.e. binary oxides) and the reading channel (i.e. MoS_2), our device can achieve an ultralow programming power consumption. Unlike the conventional two terminal memristors, the programming power consumption P_p is independent of resistive states of the synaptic device presented here. The programming power consumption P_p is kept around 50 pW while the synaptic conductance varies from ∼1 nS to ∼100 μS. We also benchmark the performance of our device with state-of-the-art synaptic memristors [35, 45, 69–79]. As shown in figure 6(a), our device has a clear advantage in terms of low programming power, especially when the synaptic device operates in the LRSs. For example, Chen *et al* demonstrated a Ag/h-BN/Ag threshold resistive switching memristor with compliance-current-controlled on/off ratio ranging up to 10^{11}. The device exhibited ultra-low P_p (∼40–80 fW) when the synaptic conductance is on the order of 100 fS. However, the P_p can rise to ∼0.4–0.7 μW when the synaptic conductance in about 2 μS [35]. Our device consumes about 10^7 lower P_p than the state of the art at the same synaptic conductance. It allows more precise control on the synaptic weight update at a given pulse width. This is the key advantage of the binary oxide based MoS_2 ICGS device with a three-terminal design, in which the programming and reading channels are separated. The reading power usually depends on the minimum measurable voltage and current resolution of instruments and does not fully reflect the inherent properties of synaptic devices. Therefore, the reading power consumption is not benchmarked here. Figure 6(b) shows the accumulative energy consumption as a function of the synaptic conductance change ratio during depression (normalized by initial conductance of 108 μS). It consumes less than 1 pJ of total energy to adjust the synaptic conductance across about five orders of magnitude.

It is worth noting that our MoS_2 ICGS devices differ from the conventional silicon charge-trap flash memory based synaptic devices in three folds. (1) In conventional charge-trap flash memory, the programming/erasing voltage polarity only depends on the doping type of channel semiconductor [80, 81], not on the stacking sequence of dielectrics. In this work, the depression and potentiation pulse polarity can be reversed by changing the stacking sequence of dielectrics, which provides new tuning knobs for synaptic weight modulation. (2) In charge-trap flash memory, the bulk defect/trap states play a dominating role in hosting injected carriers through Fowler–Nordheim tunneling or hot carrier effects [82, 83]. In our device, the interfacial defect/trap states near the binary oxide interface play a more important role than the bulk traps inside individual oxide layers. (3) The atomic thickness of the MoS_2 channel allows a tight electrostatic control by the interfacial charges induced by the Maxwell-Wagner instability. The atomically thin 2D channel and a tight electrostatic gate control translate to a wider dynamic range of resistive switching of the synaptic channel at a given amount of injected interfacial charges near the

binary oxide interface, compared to 3D bulk semiconductor channels made from silicon.

3. Conclusion

We have fabricated binary oxide based MoS_2 ICGS devices with ultralow programming power consumption (∼50 pW), which is independent of the synaptic conductance. This benefits from the physical separation of the programming channel and the reading channel. Induced by Maxwell-Wagner instability, interfacial charges near the binary oxide interface can be generated and modulated by pulses applied to the substrate. Through the electrostatic gating of the induced interfacial charges, the MoS_2 synaptic channel conductance can be tuned. Both potentiation and depression have been experimentally demonstrated. By reversing the oxide stacking sequence, the excitatory/inhibitory pulse polarity will also be reversed, which further validates the Maxwell-Wagner instability model. Due to the atomic thickness MoS_2 channel, the interfacial charge holds tight electrostatic control over the channel and leads to a wide resistive switching dynamic range of 10^5. Our method is also CMOS compatible and can be easily scaled up for system-level in-memory computing.

4. Methods

4.1. Fabrication of IGCS devices

We started with a 500 μm thick heavily doped silicon substrate, which also performs as the backgate electrode. The binary oxide layers (10 nm AlO_x/10 nm SiO_x) were deposited sequentially using ALD method at a temperature of 250 °C. Few-layered MoS_2 flakes were mechanically exfoliated on top of the binary oxide layers, from commercially available n-type molybdenum disulfide crystal (supplied by 2D Semiconductors) using Scotch tape. The source and drain contacts were patterned by a standard EBL process. Au was used as the contact metal with a thickness of 50 nm, using electron beam evaporation. To mitigate the damage of the evaporated Au to the MOS_2 surface, the first 5 nm Au was deposited at a rate of 0.5 Å s^{-1}, and the rest of Au was deposited at a rate of 5 Å s^{-1}.

4.2. Electrical characterization

The transient electrical measurements were conducted using a Keysight B1500A semiconductor parameter analyzer and a probe station. The waveform generator was connected to the Si back gate of the device under test to generate pulses using Keysight 33600 waveform generator. The MoS_2 channel current was measured by Keysight B1500, with a sampling rate of 100 μs. During the measurement, a reading voltage of 10 mV was constantly applied to the drain terminal.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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