A Silicon Photomultiplier Based Detection System with Integrated Feature Extraction

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***Abstract*—This paper presents a silicon photomultiplier (SiPM) based sensor with integrated feature extraction module. SiPMs are used in many applications such as time of flight measurements, fluorescence lifetime estimation, underwater wireless optical communication, quantum computing, high-resolution imaging, and particle physics. In order to facilitate signal processing such as timing, energy, and periodic events, feature extraction is integrated with the SiPM readout. The feature extractor consists of a peak detector, a sign bit generator, an integrator, a pulse width detector, and a digital output generator. The average power consumption is 2.12 mW.**

***Index Terms*—Silicon Photomultiplier (SiPM), Feature Extraction, Sensors, Single Photon Avalanche Diode (SPAD).**

I. Introduction

Silicon photomultipliers (SiPM) are used in applications such as quantum communication, high-energy physics, and medical imaging [1], [2]. Multiple parallel single photon avalanche photodiodes (SPAD), each with its own quenching resistor, make up a SiPM [3]. The raw SiPM signals must be converted into informative features by a feature extractor in order for them to be used in machine learning applications. The scheme is presented in Fig. 1. The features that have been extracted include time, amplitude, pulse shape, integral information, derivative insights, statistical measurements, and frequency domain components.

These carefully selected features offer a comprehensive representation for later machine learning techniques by encapsulating the various aspects of the SiPM signals. For example, time information allows for exact temporal analysis and random nature. Pulse shape characteristics help with event identification. Amplitude information indicates the energy of observed events [4]–[8]. Utilizing the information-rich nature of SiPM signals, these features can be integrated into machine learning models to improve analytical results and enable precise event classification, energy calculation, and other data-driven tasks.

By converting extracted features, such as peaks, derivatives, integrals, and pulse widths, into structured input vectors for a machine learning model, the feature extractor for SiPM signals easily interacts with machine learning. The model gains knowledge of patterns and correlations in the SiPM data through training on a labeled dataset, which makes precise predictions or classifications possible. Through this integration, the SiPM's capabilities are improved in a variety of applications, such as energy estimation and event classification. It also offers a strong framework for automated analysis and decision-making based on the intrinsic qualities of SiPM signals.

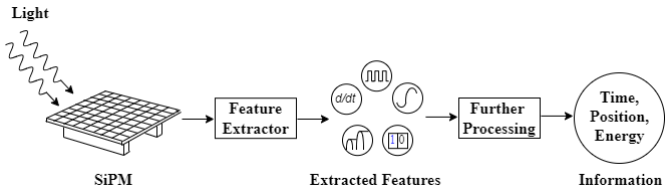


Fig. 1. SiPM feature extractor scheme.

Many SiPMs' output signals require processing and synchronous readout. Typically these use external FPGAs or DSPs [9]. The frameworks implemented include Time to Digital Converter (TDC), high-speed comparators, and off-chip resistors [10]–[13]. For digitization purposes, the read-out circuits can share an ADC between themselves [14]. Machine learning techniques are also used in SiPM-Based Detection and Discrimination. ML-based Power Spectral Density (PSD) approaches have been used in various scintillators and light sensors to explore the potential effects of this type of pulse shape discrimination [7].

Feature extraction systems are typically implemented using software or using digital signal processors and embedded systems. Integrating the feature extractor blocks on a single chip reduces the parasitics and increases the speed and throughput while optimizing size, weight, and power. The objective of this work is to create an on-chip feature extractor specifically for SiPMs. This has the potential to be applied in quantum computing, high-resolution photography, and basic particle physics research.

In this paper, a feature extraction system suitable for SiPM based detectors is presented. To the best of our knowledge, this is the first custom based feature extraction topology that can be implemented directly with the SiPM on the same chip. The paper is organized as follows. Section II illustrates the system design. Section III exhibits the simulation results and finally section IV draws the conclusion.

II. System Design

The system incorporates several sub-systems including the SiPM module and multiple feature extractor modules. The feature extractor unit includes a sign bit generator, an integrator,

a peak detector, a pulse width detector, and a digital signal generator. The overall system is shown in Fig. 2, while the individual circuit diagrams are shown in Fig. 3. The overall feature extractor topology is based off of [15].

A. Silicon Photomultiplier

A silicon photomultiplier, is a type of semiconductor photodetector composed of a parallel array of individual single-photon avalanche diodes (SPADs), each with its own quenching resistor. Due to the array arrangement, multiple photons can be detected simultaneously compared to a single SPAD deadtime.

Each SPAD operates in Geiger Mode in reverse breakdown with a bias applied that is above the breakdown voltage [16]. A Geiger Mode APD (or SPAD) operates in three modes, quiescent, discharge, and recovery. The diode is in reverse breakdown when it is in quiescent state. In this mode, it functions as an open switch. The diode stays in this state without any current flow unless a photon is absorbed or a dark event (for example due to thermal noise) occurs. If a photon is absorbed, electron hole pairs are generated and are accelerated due to the high electric field. Once activated, the avalanche mechanism is self sustaining. This means that a constant current flows through the device endlessly without quenching. This avalanche process is stopped by the quenching resistor, placing the device back into the recovery phase. While the avalanche is occurring and until the avalanche is quenched, the device cannot respond to any further incoming photons. This time is known as the deadtime.

The SiPM module is made of four SPADs, each with its own quenching resistor. More SPADs generally improve sensitivity, but may increase noise and crosstalk. Fewer SPADs may reduce sensitivity but can offer benefits in terms of size, cost, and other performance characteristics.

Fig. 3(a) shows the SPICE model to generate a realistic SPAD signal for simulations [17]. It consists of three switches, a voltage source, a resistor, and a capacitor. $V_{SPAD} = 7V$, $R_{SPAD} = 1k\Omega$, and $C_j = 4pF$ model the breakdown voltage, quenching resistor, and the junction capacitance respectively. When there is an incident photon on the system, there is an impact on the voltage controlled switches, S_1, and S_2. If the voltage is greater than the breakdown voltage of the SPAD, there is an avalanche of current flow in the diode. So, there is a sudden peak in the characteristic curve. After detecting the incident pulse corresponding to this peak, the system needs to reset in order to detect the next peak. This action is performed by the quenching resistor, R_{SPAD}.

The SiPM readout is based on a current mirror structure with two outputs [18]. The two output, fast and slow, mimic the fast and slow output of commercial analog SiPMs. The output current from the SiPM is mirrored by a current mirror with two outputs. The slow output is taken across a resistor, converting to convert into a voltage. The fast output is filtered through a high pass RC topology. The capacitor and resistor associated with this filter leads to faster charging and discharging.

B. Sign Bit Generation

The sign bit from the input signal can be obtained using the sign of the second derivative. A differentiator extracts the slope of the input signal. This is then passed through a second differentiator to determine the change in slope of the input signal. A comparator finally generates the sign bit of the signal.

Fig. 3(b) shows the differentiator which is based on an operational amplifier with RC feedback network. This detects the signal peak or maxima. The transistor sizes are $(W/L)_{D1} = (W/L)_{D2} = (W/L)_{D8} = \frac{1.8\mu}{360n}$, $(W/L)_{D3} = (W/L)_{D4} = (W/L)_{D5} = (W/L)_{D6} = (W/L)_{D7} = \frac{3.6\mu}{360n}$. The opamp is a standard 5 transistor OTA. The closed loop gain of this configuration is [19],

$$A_v = -\frac{R_F}{X_{C_{D1}}} = -2\pi f C_{D1} R_F \tag{1}$$

where R_F, and $X_{C_{D1}}$ denote the resistance of the feedback resistor, and the reactance of the input capacitor respectively, while C_{D1} represents the input capacitance value, and f indicates the frequency of the input signal.

Fig. 3(c) shows the designed comparator based on a 5-transistor Operational Transconductance Amplifier (OTA). The aspect ratio of the transistors are, $(W/L)_{C1} = (W/L)_{C2} = (W/L)_{C3} = (W/L)_{C4} = (W/L)_{C5} = (W/L)_{C7} = \frac{720n}{360n}$ and $(W/L)_{C6} = \frac{1.44\mu}{360n}$.

$$V_{comp_{out}} = \begin{cases} V_{DD} & V_{in} \geq V_{Ref} \\ 0 & V_{in} < V_{Ref} \end{cases} \tag{2}$$

Whenever the input signal goes above the reference voltage V_{Ref}, the comparator gives a high signal and vice-versa.

C. Integration

The integral of the SiPM output signal is another feature that needs to be extracted. This helps to determine the energy of the incident photons and the signal's amplitude. As there are two outputs from the SiPM, of which one is current mode, the integrator can also be helpful to obtain the total charge accumulated from the current output.

An op-amp was used to build the integrator in Fig. 3(d). The aspect ratios of the transistors are $(W/L)_{I1} = (W/L)_{I2} = (W/L)_{I8} = \frac{1.8\mu}{360n}$, $(W/L)_{D3} = (W/L)_{D4} = (W/L)_{D5} = (W/L)_{D6} = (W/L)_{D7} = \frac{3.6\mu}{360n}$. In this case, a capacitor is employed in the feedback loop to obtain an integrator response, while a resistor has been used in the inverting input. A large value resistor has also been employed in the feedback loop in parallel with the feedback capacitor to obtain better stability of the structure. Finally, the closed loop gain is [19],

$$A_v = -\frac{X_{C_F}}{R_{I1}} = -\frac{1}{2\pi f C_F R_{I1}} \tag{3}$$

where X_{C_F}, and R_{I1} denote the reactance of the feedback capacitor, and the resistance of the input resistor respectively, while C_F represents the feedback capacitance value, and f indicates the frequency of the input signal.

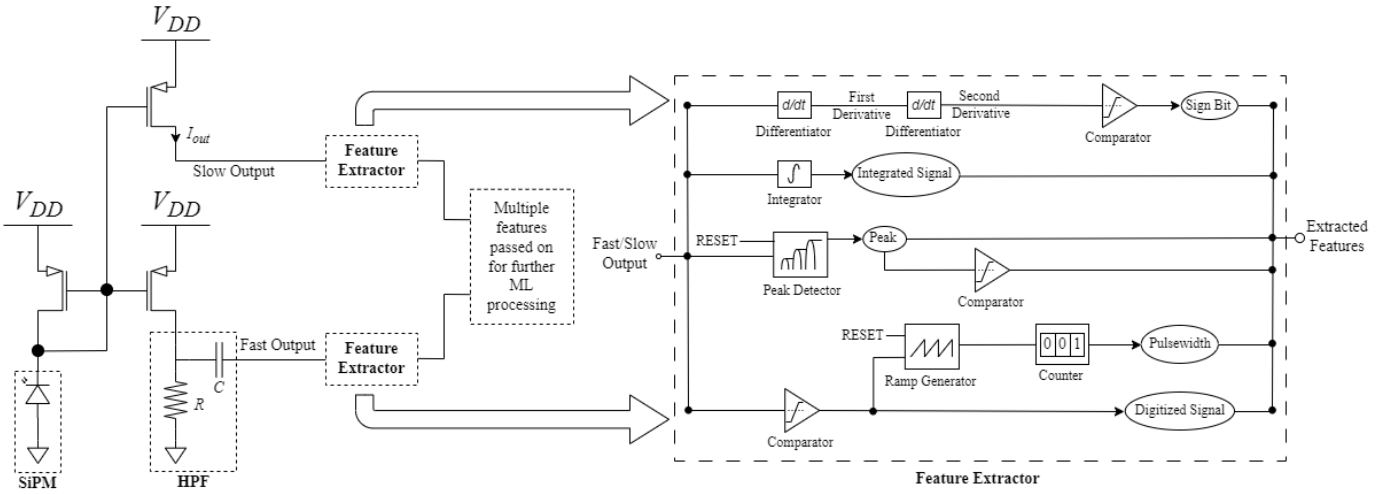


Fig. 2. Feature extractor for a SiPM based sensor consists of a sign bit generator, an integrator, a peak detector, a pulse width detector, and a digital signal generator.

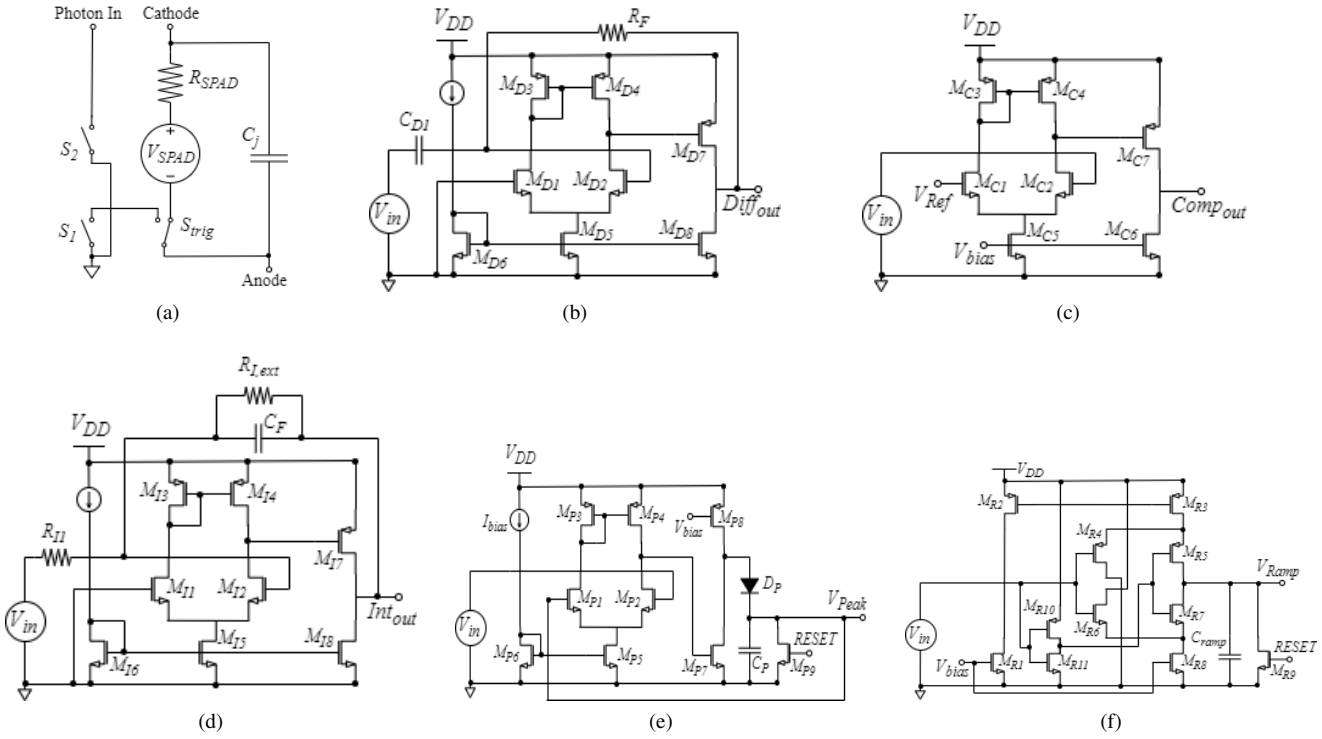


Fig. 3. Circuit topologies for individual feature extractor modules (a) SPAD model, (b) Differentiator, (c) Op-amp as a comparator, (d) Integrator, (e) Peak detector, and (f) Ramp generator.

D. Peak Detection

Fig. 3(e) shows the peak detector, consisting of a 5 transistor OTA with NMOS driving transistors, a NMOS common source amplifier with PMOS load, a diode, and a capacitor at the output terminal [15]. The aspect ratios of the transistors are, $(W/L)_{P1} = (W/L)_{P2} = (W/L)_{P7} = (W/L)_{P9} = \frac{1.8\mu}{360n}$, $(W/L)_{P3} = (W/L)_{P4} = (W/L)_{P5} = (W/L)_{P6} = (W/L)_{P8} = \frac{3.6\mu}{360n}$.

The capacitor needs to be discharged each cycle so that it could store the next information. This discharging process is operated by an NMOS switch (M_{P9}), controlled by a RESET signal.

This peak voltage is then passed though a comparator to obtain a digital output. Here, the same comparator of Fig. 3(b) is used, which treats the peak voltage above it as high and vice-versa.

E. Pulse Width Detection

Pulse width corresponding to the SiPM output signal can be obtained in multiple steps. In the beginning, the SiPM output will be passed through the comparator to obtain the digitized

output. Then, the rectangular signal output was fed as the input to the ramp generator. A counter keeps track of the time that the ramp generator takes to rise. The conversion time can be written as [20],

$$t_c = \left(\frac{v_{in}}{v_{ref}}\right)(2^N)(T_{CLK}) \tag{4}$$

where v_{in}, v_{ref}, N, and T_{CLK} denote the input voltage, reference voltage, number of bits, and time period of the clock signal respectively.

Fig. 3(f) shows the designed ramp generator, which would produce ramp signals with respect to its rectangular input, arriving from the comparator in the preceding block [15]. The aspect ratio of the transistors are, $(W/L)_{R1} = (W/L)_{R3} = (W/L)_{R4} = (W/L)_{R5} = (W/L)_{R10} = \frac{3.6\mu}{360n}$, $(W/L)_{R2} = (W/L)_{R6} = (W/L)_{R7} = (W/L)_{R9} = (W/L)_{R11} = \frac{1.8\mu}{360n}$, and $(W/L)_{R8} = \frac{14.4\mu}{360n}$.

An NMOS switch (M_{R9}) has been employed to discharge the output capacitor periodically to detect the next cycle, controlled by a reset signal. This reset signal has also been designed utilizing a comparator so that it provides zero voltage output when its input is above the reference level and vice-versa.

When the comparator input is high, the output is zero. As a result, the NMOS connected in parallel with the output capacitor turns off, and the capacitor gets charged and stores the input. When the comparator input is low, the reset NMOS turns on, and voltage across the output capacitor is zero, and it gets ready for storing the input of the next cycle.

The ramp signal will continue to rise while the input is high. By observing the height and length of the generated ramp signal, the pulse width of the rectangular input can be measured.

III. Results

All the simulations were performed in Cadence using a commercial 180 nm CMOS process. A SiPM output signal from a spice model has been fed as input to the blocks.

Fig. 4 illustrates multiple figures showing the response to a common input, which is the SiPM output signal. Fig. 4(a) is of the SiPM fast output. The pulse signals controlling the SPADs inside the SiPM, contain different time periods. Their time periods are set in such a way that they overlap to reflect different environmental scenarios. As a result, the SPAD output signal is varied in time and of different pulse height and width. When there is an incident photon or multiple photons, the SiPM output pulse responds with varying height and width.

Fig. 4(b), and Fig. 4(c) show the 1^{st}, and 2^{nd} derivative of the SiPM output respectively. Here, C_{D1}, R_F, and I_{bias} are 1pF, 5kΩ, and 10μA respectively. Whenever there is a pulse in the SiPM output, the differentiator shows a sharp rising response. Then, it goes into a rest state until the next pulse. The ripple seen in the derivative output is due to the capacitive factor, which comes into play from the input capacitor of the integrator circuit. The differentiation of the SiPM signal is significant for the timing information of the pulse, edge detection, pulse shape analysis, and noise reduction purposes.

Fig. 4(d) shows the sign bit, that is the comparator response after the 2^{nd} derivative. The comparator uses a reference voltage of 600mV. The overall sign bit generation scenario can be described in the following manner. When there is an incident of a single photon or multiple photons, the SiPM responds to that accordingly, varying its pulse height and width with respect to the number of incident photons. The first and second derivative respond to this SiPM output. The sign bit is finally generated after performing thresholding of the second derivative. In summary, a sign bit is generated whenever there is a photon incident on the SiPM. This is significant in Time-to-Digital Conversion (TDC), data compression, improving sensitivity, and digital signal processing.

Fig. 4(e) shows the integration output of the SiPM signal. Here, $R_{I,ext}$ is used as the large value resistor of 100kΩ, to obtain improved stability of the circuit. C_F, R_{I1}, and I_{bias} are valued at 1pF, 10kΩ, and 10μA respectively. Charge accumulation, number of incident photon, and pulse area parameters are determined by this. This is useful to determine the energy of the signal.

Fig. 4(f) shows the peak detector output from of the SiPM signal. A bias voltage, V_{bias} of 200 mV has been used here, while bias current, I_{bias} being 10μA. Then it is passed through a comparator to provide a digital output, which can be seen in Fig. 4(g). The reference voltage of the comparator is 700 mV. There are multiple peaks in the SiPM signal and the comparator has just one reference voltage. As a result, if the reference is set as the lowest peak voltage, the higher peaks' thresholding would provide wider pulse. If the reference is set as the highest peak value, lower peaks would not be detected by the comparator. The comparator output provides the time instance of the SiPM output signal peak, while the peak detector output gives the actual value of the signal peak. Peak detection is important for Time-of-Flight (ToF) measurements, threshold setting, time resolution enhancement, and noise rejection.

Fig. 4(h) shows the comparator output of the SiPM signal, with respect to a reference voltage of 600 mV. This is also taken as the digitized output of the SiPM signal. This provides all the benefits of a digital signal over an analog SiPM signal. This can be advantageous in quantization, precision, data storage, and transmission.

The comparator output, illustrated in Fig. 4(h), is followed by a ramp generator. The ramp generator output is seen in Fig. 4(i). The bias voltage of the ramp generator, V_{bias} has been set as 1.8 V while the output capacitor, C_{ramp} being 20pF. The ramp generator response changes its height and width with respect to the input from the comparator. The height and width of the ramp generator is directly proportional to the SiPM pulse.

The initial simulations have been verified by post-layout analysis. It can be seen from the figure that both of the plots are similar, though there are some deviations in the post-layout. These are due to parasitic elements present in the layout and

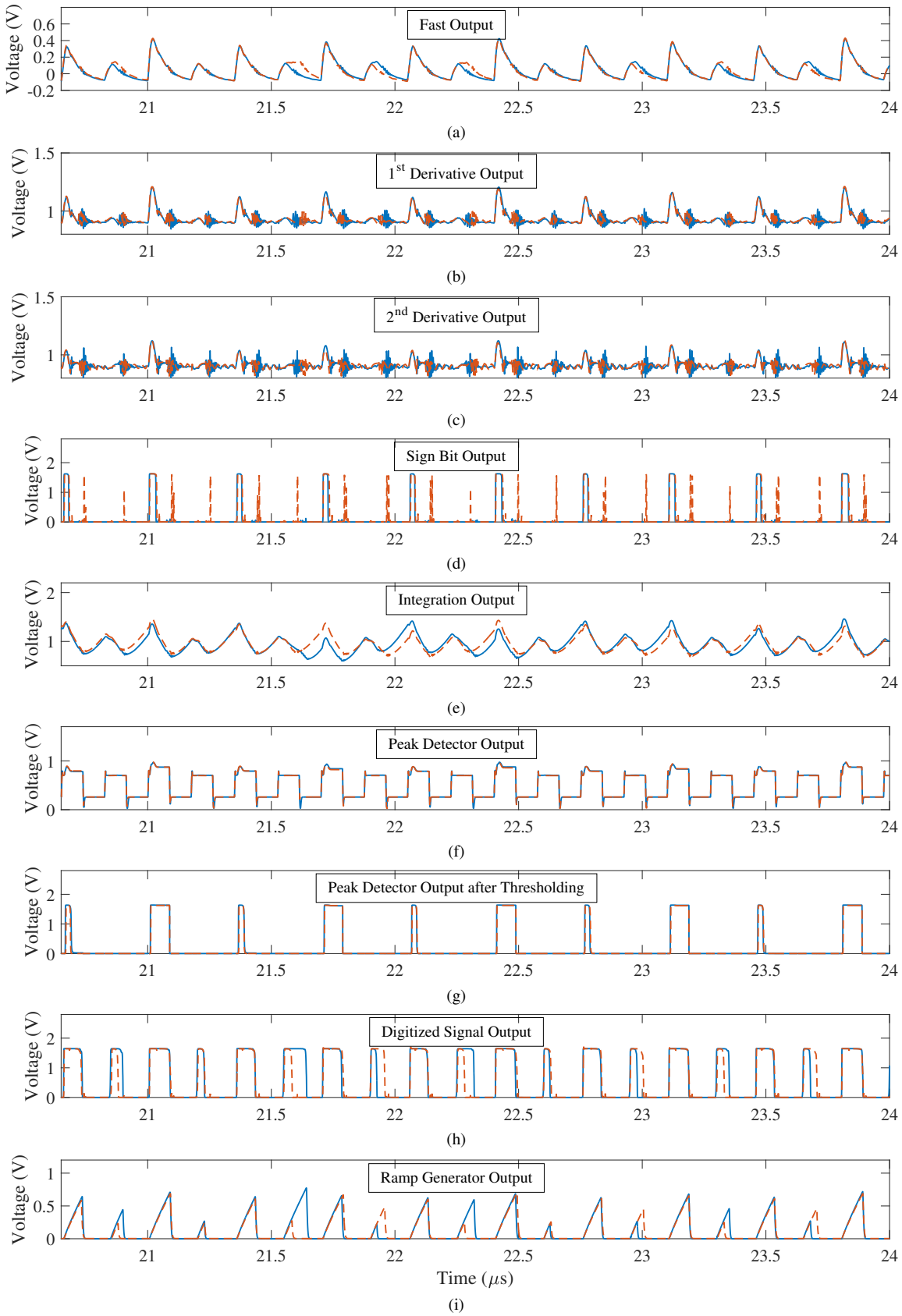
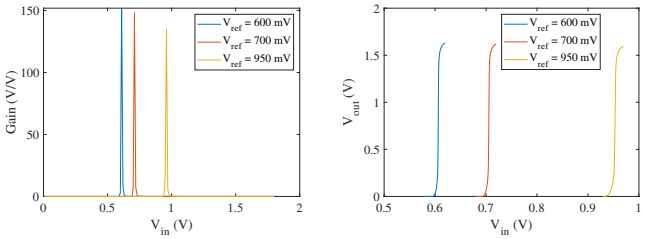


Fig. 4. Simulated output of the (a) SiPM, (b) differentiator, (c) double derivivative, (d) sign bit (e) integrator, (f) peak detector, (g) thresholding after the peak detector, (h) digitization, and (i) ramp generator response after the comparator; where solid and dashed lines represent the simulation and post-layout analysis respectively.



(a) (b)

Fig. 5. Characteristics of the comparators, (a) Gain, and (b) Resolution

the performance can be improved by optimizing the layout.

An op-amp was used for the differentiator, the integrator, and the comparator. The op-amp has an open loop gain of 51dB, a phase margin of 50°, and a slew rate of 8.9 V/μs.

There are three comparators used in the system, to generate the sign bit, to perform the thresholding of the detected peak, and to obtain digitized output. They have reference voltages of 950 mV, 700 mV, and 600 mV respectively. The characteristics of the comparators are shown in Fig. 5. They show gain values of 134.68, 148.26, and 151.92 respectively. The comparators have resolution values of 10 mV, 5 mV, and 2 mV respectively. This is obtained by observing the transition period of the comparator output around the reference voltage.

IV. Conclusion

This paper presented a feature extractor for a SiPM signal which can be integrated on the same chip with the readout circuit. The feature extractor has several units including the differentiator, integrator, peak detector, ramp generator, and sign bit generator. These features can be used to extract multiple features such as maxima location and value, total charge accumulation, signal peak, pulse width, and digitized output. In association with machine learning techniques, these can aid in determining the nature particles or communication protocols. These information can be utilized in various applications such as medical imaging, particle physics, optical communication, and fluorescence lifetime estimation. The average consumed power of the system is 2.12 mW.

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References

[1] R. Bellini, G. L. Montagnani, M. Carminati, D. D. Vita, and C. Fiorini, "Laser-based Scintillator Crystal Emulator for Optical Testing of SiPM Readout Technologies," in *IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings*, Sydney, NSW, Australia, 2018, pp. 1–3.

[2] M. H. U. Habib and N. McFarlane, "A Perimeter Gated Single Photon Avalanche Diode based Silicon Photomultiplier as Optical Detector," in *IEEE International Midwest Symposium on Circuits and Systems*, Fort Collins, CO, USA, 2015, pp. 1–4.

[3] D. Renker and E. Lorenz, "Advances in Solid State Photon Detectors," *Journal of Instrumentation*, vol. 4, no. 04, p. P04004, 2009.

[4] D. Meier, S. Mikkelsen, J. Talebi, S. Azman, G. Mæhlum, and B. E. Patt, "An ASIC for SiPM/MPPC readout," in *IEEE Nuclear Science Symposuim & Medical Imaging Conference*, Knoxville, TN, USA, 2010, pp. 1653–1657.

[5] M. Farhan, A. Y. Rahman, and N. McFarlane, "A pH Sensing System with Security Enhanced Cryptographic System," in *IEEE 66th International Midwest Symposium on Circuits and Systems*, Tempe, AZ, USA, 2023, pp. 947–951.

[6] C. S. Levin, S. H. Maramraju, M. M. Khalighi, T. W. Deller, G. Delso, and F. Jansen, "Design Features and Mutual Compatibility Studies of the Time-of-Flight PET Capable GE SIGNA PET/MR System," *IEEE Transactions on Medical Imaging*, vol. 35, no. 8, pp. 1907–1914, 2016.

[7] M. Durbin, M. A. Wonders, A. T. Lintereur, and M. Flaska, "Application of a Novel Machine Learning Approach to SiPM-based Neutron/Gamma Detection and Discrimination," in *2019 IEEE Nuclear Science Symposium and Medical Imaging Conference*, Manchester, UK, 2019, pp. 1–2.

[8] C. Fu, A. Di Fulvio, S. Clarke, D. Wentzloff, S. Pozzi, and H. Kim, "Artificial Neural Network Algorithms for Pulse Shape Discrimination and Recovery of Piled-up Pulses in Organic Scintillators," *Annals of Nuclear Energy*, vol. 120, pp. 410–421, 2018.

[9] B. Wu, Y. Wang, Q. Cao, J. Kuang, M. Wang, and X. Zhou, "An FPGA-based Time Sampling Charge Measurement Method for TOF-PET Detectors," in *2019 IEEE International Instrumentation and Measurement Technology Conference*, Auckland, New Zealand, 2019, pp. 1–5.

[10] E. Venialgo, N. Lusardi, A. Geraci, K. O'Neill, S. Gnecchi, C. Jackson, S. Brunner, D. Schaart, and E. Charbon, "An Order-statistics-inspired, Fully-digital Readout Approach for Analog SiPM Arrays," in *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop*. Strasbourg, France: IEEE, 2016, pp. 1–5.

[11] V. Vinayaka, S. P. Namboodiri, A. Roy, and R. J. Baker, "Segmented Digital SiPM," in *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems*, Dallas, TX, USA, 2019, pp. 1118–1121.

[12] N. Lusardi, F. Garzetti, S. Salgaro, N. Corna, E. Ronconi, A. Costa, A. Geraci, E. Ripiccini, F. Gramuglia, T. Milanese, C. Bruschini, and E. Charbon, "FPGA-based SiPM Timestamp Detection Setup for High Timing Resolution TOF-PET Application," in *IEEE Nuclear Science Symposium and Medical Imaging Conference*, 2021, pp. 1–5.

[13] C. Ma, X. Dong, L. Yu, W. Wang, X. Zhao, X. Li, Z. Huang, G. Wu, L. Lu, and H. Chen, "Design and Evaluation of an FPGA-ADC Prototype for the PET Detector Based on LYSO Crystals and SiPM Arrays," *IEEE Transactions on Radiation and Plasma Medical Sciences*, vol. 6, no. 1, pp. 33–41, 2022.

[14] Y. Tang, R. Zhang, and J. Chen, "A Low-power 16-Channel SiPM Readout Front-end with a Shared SAR ADC in 180 nm CMOS," in *2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology*, Kunming, China, 2020, pp. 1–3.

[15] K. A. A. Mamun and N. McFarlane., "Integrated Real Time Bowel Sound Detector for Artificial Pancreas Systems," *Sensing and Bio-Sensing Research*, vol. 7, no. 2, pp. 84–89, 2016.

[16] F. Rahman, M. Smalley, S. Hicks, M. S. Ara Shawkat, and N. McFarlane, "A Multimodal Hand Gesture Recognition System utilizing PPG and Impedance Sensors," in *IEEE Biomedical Circuits and Systems Conference*, 2023, pp. 1–5.

[17] F. Zappa, A. Tosi, A. D. Mora, and S. Tisa, "SPICE Modeling of Single Photon Avalanche Diodes," *Sensors and Actuators A: Physical*, vol. 153, no. 2, pp. 197–204, 2009.

[18] Y. Tang, Q. Fan, Y. Feng, H. Deng, R. Zhang, and J. Chen, "A Low-Power SiPM Readout Front-End with Fast Pulse Generation and Successive-Approximation Register ADC in 0.18 μm CMOS," in *2019 IEEE International Symposium on Circuits and Systems*, Sapporo, Japan, 2019, pp. 1–4.

[19] E. Kennedy, *Operational Amplifier Circuits: Theory and Applications*, 1 1988.

[20] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 8 1997.