Electrical Transport in Al-Si/Al-Ge Nanojunction Schottky Barrier Field Effect Transistors

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Abstract

Understanding the electronic transport of metal-semiconductor heterojunctions is of utmost importance for next-generation nanoelectronics with device functionalities beyond the capabilities of conventional field effect transistors, plasmon-enhanced optoelectronics and quantum applications. Here, we provide an in-depth discussion of the transport mechanisms in Si and Ge nanowires embedded in Schottky barrier field effect transistors. Key for the fabrication of these devices is the selective and controllable solid-state metal-semiconductor exchange of Si and Ge nanowires into Al, enabling high-quality monolithic and single-crystalline Al contacts. To investigate the transport in Al-Si and Al-Ge heterostructures, detailed and systematic electrical characterizations are carried out by bias spectroscopy in the temperature regime between T = 77.5 K and 400 K. In this respect, the transport mechanisms in the scope of transfer and output characteristics analysis have been investigated and the transconductance and activation energy have been extracted. Thereof a crucial difference of Fermi level pinning was noticed. Whereas the Al-Si system showed symmetric effective Schottky barriers, the Al-Ge system revealed a highly transparent contact for holes due to Fermi level pinning close to the valance band, where charge carrier injection saturation by a thinned effective Schottky barrier. Moreover, thermionic field emission limits the overall electron conduction, indicating a distinct Schottky barrier for electrons.

Introduction

Nanowire (NW) based Schottky barrier (SB) metal-semiconductor-metal (MSM) heterostructures are highly interesting for various emerging applications in nanoelectronics, quantum electronics and optoelectronics that benefit from their unique physical, electrical and photonic/plasmonic properties. Regarding fabrication, the concept of SB devices benefit of the lack of required doping as well as subsequent high-temperature processes.[1–3] Remarkably, most metal-semiconductor junctions show a certain degree of ambipolar characteristic of charge carrier injection of electrons and holes into the semiconductor, allowing versatile areas of "Beyond Moore" applications.[4,5] Especially, nanoelectronic devices, which injection capabilities highly rely on the quality and reproducibility of their nanojunctions profit of these attributes. Another important and emerging field is plasmon-enhanced optoelectronics, such as photodetectors with increased bandwidth or monolithic plasmon detectors.[6,7] Lately, metal-semiconductor heterojunctions also got relevant for quantum applications, as superconductor-semiconductor hybrid devices such as Josephson junction field effect transistors used for superconducting qubits.[8–10]

In this respect, Al draw high attention to both group IV semiconductors, Si and Ge, due to its unique and reliable diffusion mechanism in comparison to other metals,[11,12] which tend to form intermetallic phases, as e.g. NiSi[13] or NiGe.[14] Moreover, utilizing Al allows subsequent annealing steps for precise definition of the semiconducting channel, whereas most silicides and germanides tend to change their phases, leading also to variations in the electric behavior of the metal-silicide/germanide-semiconductor heterostructure. Also in terms of modern CMOS integration nanoscale Al suits well, due to its monocrystalline nature that facilitates a high structural and electrical quality, which is in strong contrast to the known deficiencies of bulk and layer Al-Si/Ge systems, that are plagued by void-formation, spiking and electromigration driven reliability concerns. Another crucial technological aspect of Al-group IV heterojunctions is the formation of an abrupt interface, allowing precise scaling and positioning of potential top-gates (TGs). Importantly, gated SB heterostructures show

unique transfer characteristics fundamentally different to metal-semiconductor-oxide FETs (MOSFET), allowing to investigate the transport mechanism of electrons and holes into the semiconductor as well as in the semiconductor.[15,16] Utilizing this experimental methodology, the SB shape and its transmissivity can be modulated by varying bias conditions, allowing to analyze the transport characteristic of the metal-semiconductor heterostructure in more depth. Investigating the output characteristics of the obtained nanostructures also the activation energy, i.e. the injection capability of charge carriers into the semiconductor, can be estimated.[11,17] Certainly, theoretical TCAD modelling of the metal-semiconductor interface would even allow a detailed analysis of the charge carrier injection contributions, as thermionic (TE), thermionic-field (TFE) and field emission (FE),[18] which in an experimental approach can be merely didactically interpreted.

Due to superior NW growth methods and thus stable device characteristics, bias spectroscopy in respect to transfer and output characteristics can be executed, allowing a detailed experimental analysis of the transport properties of Al-Si-Al and Al-Ge-Al heterostructures. Till now an in-depth electronic transport investigation of Al-group IV metal-semiconductor heterostructures is still missing. Having physically and electrically equal Al leads to Si/Ge however provides unique insights, that might be useful for future applications of SBFETs with monolithic Al contacts for various applications.

Results and discussion

In this study, Si and Ge NWs are contacted by single-crystalline Al leads, where a rapid thermal annealing (RTA) process leads to the desired MSM heterostructures (cf. methods section).[11,19] Note that the integrated Si NWs are prior to integration passivated with a 9 nm thick thermally grown SiO_2. Around the Ge NWs a 10 nm thick atomic layer deposited (ALD) Al_2O_3 is grown. Importantly, these passivation layers also act as high-quality gate oxide. Especially, Ge NWs are pristine to exhibit strong transient electric characteristic

dependencies due to the presence of Ge_xO_y at the semiconductor-high-κ (here: Al_2O_3) interface.[20–22] In this context, charge carrier trapping at the Ge_xO_y layer leads to a severe shift of the threshold voltage.[23] To minimize these effects, Ge NWs with phenyl ligand surface passivation originating from the diphenylgermane precursor have been used (cf. methods section). After drain/source contact formation (here: Al) a TG, consisting of Ti/Au, covering the interfaces and the semiconducting channel is fabricated and thus constituting a SBFET.[1,3] The 3D illustration in Figure 1 shows the thereof fabricated device. Additionally, the discussed gate-stack of the Al-Si-Al device is shown in Figure 1a and of the Al-Ge-Al device in Figure 1b. Importantly, the same materials – except of the semiconductor and gate oxide – were used, allowing an appropriate comparison of the Al-group IV heterostructures. Applying a bias voltage to the drain/source contacts as well as the TG allows to operate the device in different regimes, enabling detailed investigations of the transport mechanism of the proposed material systems.

Bright field (BF) and high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) images of the Al-Si interface (cf. Figure 1a) reveal the atomically sharp and monolithic nature of the diffusion mechanism, which was executed at a temperature of T = 773.15 K. In equal measure, but at a temperature of 673.15 K, the Al-Ge exchange mechanism is initiated (cf. Figure 1b). Remarkably, even at a lower temperature a monocrystalline and abrupt interface between Al and Ge is achieved. Note that detailed investigations on the Al-Si as well as on the Al-Ge exchange mechanism were carried out in the past.[11,12]

Figure 2a shows the obtained transfer characteristics of the proposed Al-Si/Ge-Al SBFETs, sweeping the voltage V_{TG} from 5 V to −5 V and applying drain/source biases V_{DS} ranging from 0.25 V to 2 V. Analyzing the general appearance of the two sets of curves (Al-Si vs. Al-Ge) reveals one of the main differences between the two material systems integrated in the proposed SBFET architecture. In the Al-Si-Al system a relatively equal electron (I_D at $V_{TG} = 5$ V) and hole (I_D at $V_{TG} = -5$ V) current is evident, whereas the hole transport ($V_{TG} < 0$ V) in the Al-Ge-Al system is dominant in comparison to the electron current.

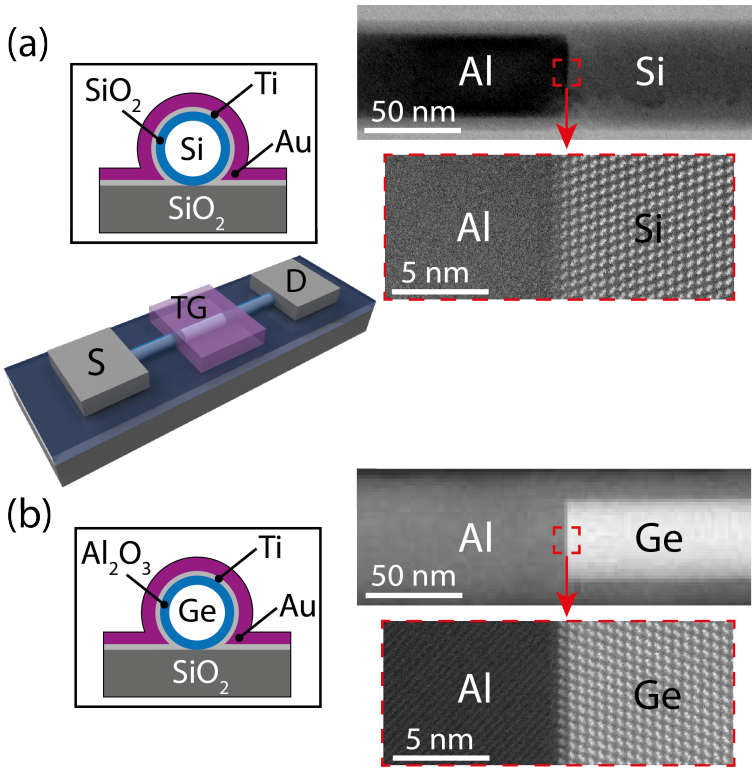

Figure 1: The 3D illustration schematically shows the SBFET architecture, where (a) shows the used gate stack of the Al-Si and (b) of the Al-Ge material system. Additionally, BF and HAADF STEM images show the monocrystalline and abrupt interface of the metal-group IV semiconductors.

This can be attributed to the difference in the Fermi level pinning of the two systems, where the Fermi level at the Al-Si interface pins relatively midgap of the Si bandgap, leading to a dedicated electron and hole SB.[24] In contrast, the Al-Ge interface has the Fermi level pinning close to the valence band, leading to dominant hole injection and thus to a transparent quasi-ohmic contact.[24,25] Additionally, the significantly lower bandgap of Ge (E_g(Ge) = 0.67 eV) in comparison to Si (E_g(Si) = 1.12 eV) gets evident, observing the on- as well as off-currents. Another important aspect gets evident observing the steepness of the slopes (cf. Figure 2b (Si) and Figure 2c (Ge)). Especially, in the p-branch of the Al-Si-Al device a kink at the kink voltage V_K is observable, indicating the transition from TE (charge carrier injection over the barrier) to TFE/FE (charge carrier injection via tunneling),[15] where the violet dashed line indicates the TE slope and the blue dashed line the TFE/FE slope. Interestingly, V_K shifts from -1.95 V at $V_{DS} = 0.25$ V to $V_K = -1.16$ V at $V_{DS} = 2$ V as the bands are stronger bent by increasing V_{DS} and thus TFE/FE should dominate the charge carrier injection. Remarkably, this transition was already shown in simulations.[26,27] Due to the use of stable Si NWs and high-quality SiO_2 as gate oxide it is possible to consider it here as well. Figure 2b shows the extracted slopes (dV_{TG}/dI_D) of the Al-Si SBFET in the two regimes. Importantly, in the TE transport the SB height dominates the injection. Thus, the slope remains constant (violet symbols) in the range of ≈0.4 V/dec. In contrast, when TFE/FE is getting dominant the slope gets more shallow in comparison to TE due to tunneling transport.[17] However, with higher applied drain/source bias (blue symbols: p-type and red symbols: n-type), the slope approaches values ranging from ≈1.3 V/dec at V_{DS} = 0.25 V to ≈0.6 V/dec at V_{DS} = 2 V. Due to stronger band bending induced by higher applied biases, the tunneling barrier gets thinner and thus enables more efficient injection of charge carriers. In contrast, the Al-Ge SBFET does not exhibit a kink in the slope, due to the quasi-ohmic contact for the injection of holes (cf. Figure 2c). Nevertheless, the kink could also be evident, however could fall into the noise floor and thus is not visible in the I/V data. Remarkably, here the slope increases with higher applied bias, due to the reduced

bandgap leading to a significant increase of the off-current caused by an increased number of charge carriers in the channel screening the transition from TE to TFE/FE. In contrast to the relatively symmetric slopes of the n- and p-branch of the Al-Si SBFET devices, here the slopes differ, which is an indication of different injection capabilities of electrons and holes.

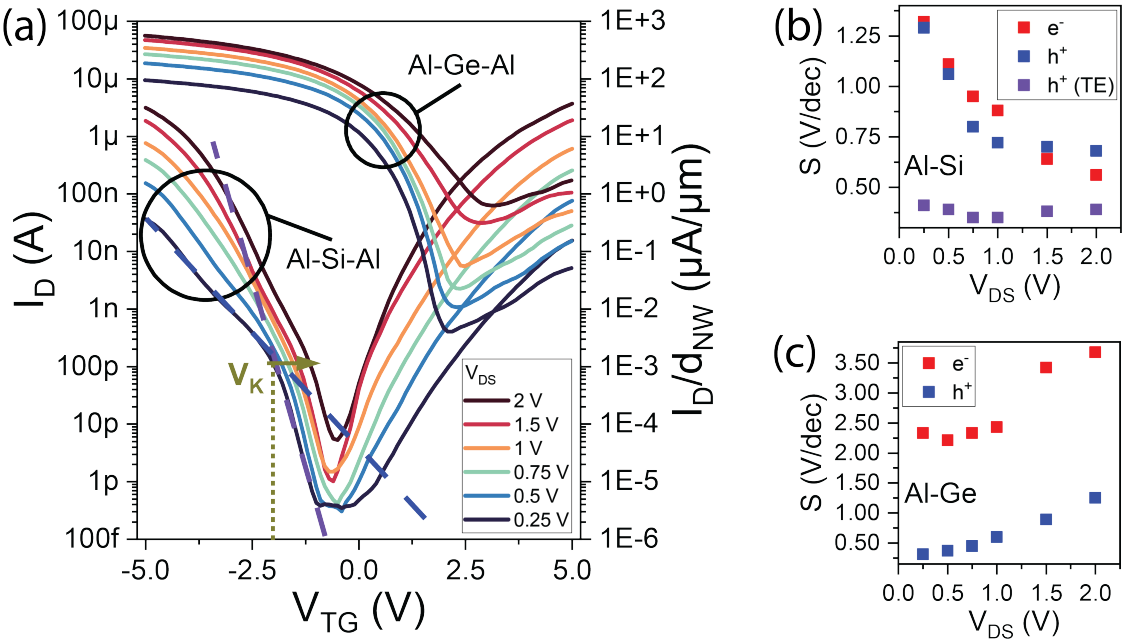

Figure 2: (a) Transfer characteristics at different V_{DS} at T = 295 K of the Al-Si and Al-Ge SBFET. Especially, for $V_{DS} = 0.25$ V at $V_{TG} = -1.95$ V of the Al-Si SBFET a kink is evident, indicating the transition from TE to TFE/FE. (b) Extracted slopes of the Al-Si SBFET. The violet symbols show the slopes in the TE regime. (c) Slopes of the Al-Ge SBFET increasing with higher applied bias V_{DS} due to the reduced bandgap of Ge.

Further analyzing the transfer characteristics (cf. Figure 2a) allows to extract the transconductance $g_m = dI_D/dV_{TG}$. Consequently, giving a qualitative measure of the input to output response in terms of the slope and thus gives an in-depth insight on the transport phenomena of the proposed material systems. Figure 3 shows the transconductance g_m extracted in dependence of V_{DS} ranging from 0.1 V to 2 V and V_{TG} ranging from −5 V to 5 V for the Al-Si (Figure 3a) and the Al-Ge (Figure 3b) SBFETs. Interestingly, analyzing the Al-Si SBFET, an asymmetric $|g_m|$ value at $|V_{TG}| = 5$ V is evident which correlates with the transfer characteristic shown in Figure 2. Observing the slope at high $|V_{TG}|$, where especially the n-branch tends to saturate in comparison to the p-branch. Here, $|g_m|$ values

of 313 nS (4.35 µS/µm) and 1.27 µS (17.64 µS/µm) are achieved in the n- and p-type branch, respectively. Another important feature of the Al-Si SBFET is the steady slope of g_m, even at $|V_{TG}| = 5\,V$, required for electronic devices, as e.g. amplifiers.[28] In contrast to the Al-Si SBFET, the transconductance g_m of the Al-Ge SBFET shown in Figure 3b shows no steady slopes, but a degradation of g_m in strong accumulation of the p-branch. Interestingly, such a degradation is typically visible in SBFETs with distinct barriers at certain bias conditions.[16] In general, g_m degradation is also caused by surface roughness scattering and series resistance. However, in the Al-Ge SBFET the Fermi level pins close to the valence band (see inset in Figure 3b) and thus enables efficient injection of holes into the semiconductor. In this case, the saturation and consequently the degradation gets evident for any bias condition. Therefore, it can be deduced that the highly transparent (quasi-ohmic) junction with phonon scattering in the Ge channel is the predominant factor in this context.[29] Moreover, higher g_m values are reached in the p-branch of the Al-Ge SBFET with 2.44 µS (32.53 µS/µm) in comparison to the Al-Si SBFET (1.27 µS), which can be attributed to steeper slopes of the p-branch transfer curves (cf. Figure 2b,c). Note that the degradation in strong accumulation leads to a maximum $g_m = 4.43\,\mu S$ (59.07 µS/µm) at $V_{TG} = -1.19\,V$. Due to weak electron conduction – in consequence of a distinct barrier for electrons – g_m merely reaches a value of 2.6 nS (0.03 µS/µm) at $V_{TG} = 5\,V$.

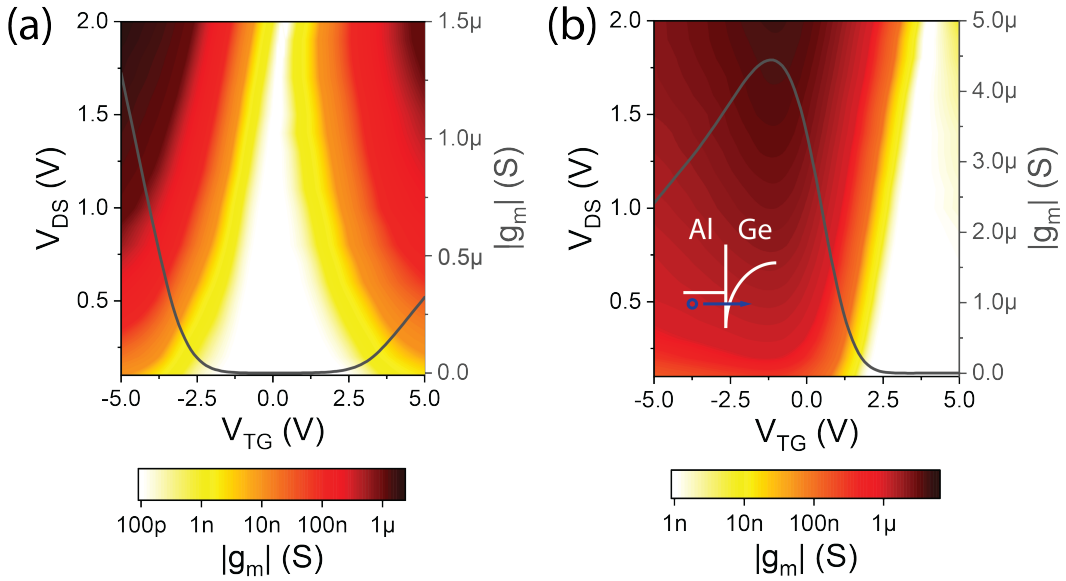

Figure 3: Transconductance $|g_m|$ maps with V_{DS} ranging from 0.1 V to 2 V derived from transfer characteristics of an (a) Al-Si and an (b) Al-Ge SBFET. Additionally, g_m vs. V_{TG} at $V_{DS} = 1$ V is plotted and indicated on the right grey y-axis in both plots. The inset in (b) depicts strong Fermi level pinning close to the valence band of the Al-Ge junction.

Figure 4 shows the temperature dependent transfer characteristics of both, the Al-Si and Al-Ge SBFET at $V_{DS} = 1$ V. Again due to the relatively symmetric Fermi level pinning of Al to Si, a symmetric transport, with $V_{TG} = 0$ V being the vertical symmetry axis is evident. Note that the insets shown in Figure 4a illustrate the band diagrams in the corresponding V_{TG} regimes. Importantly, at $V_{TG} = 0$ V dedicated barriers for electrons as well as holes are evident, leading to low off-currents in the fA-regime (minimum resolution of the measurement equipment). Elevating the temperature leads to an increased off-current due to thermally excited charge carriers. However, considering the current in the n- and p-branch stable operation modes are observed over the investigated temperature regime from 77.5 K to 400 K, proving the excellent thermal operation stability of the Al-Si material system in the investigated regimes. The Al-Ge system, shown in Figure 4b, reveals strong temperature dependencies, which can be attributed to the reduced bandgap in comparison to Si as well as strong Fermi level pinning close to the valence band, leading to a high contribution of thermally excited charge carriers. Moreover, these facts get evident observing the off-

current, which increases at lower temperatures in comparison to the Al-Si material system and distributes over a wider V_{TG}. Considering the current in the p-branch, remarkably high values in the 10 µA-regime are evident, further revealing dominant p-type characteristic of the Al-Ge SBFET.

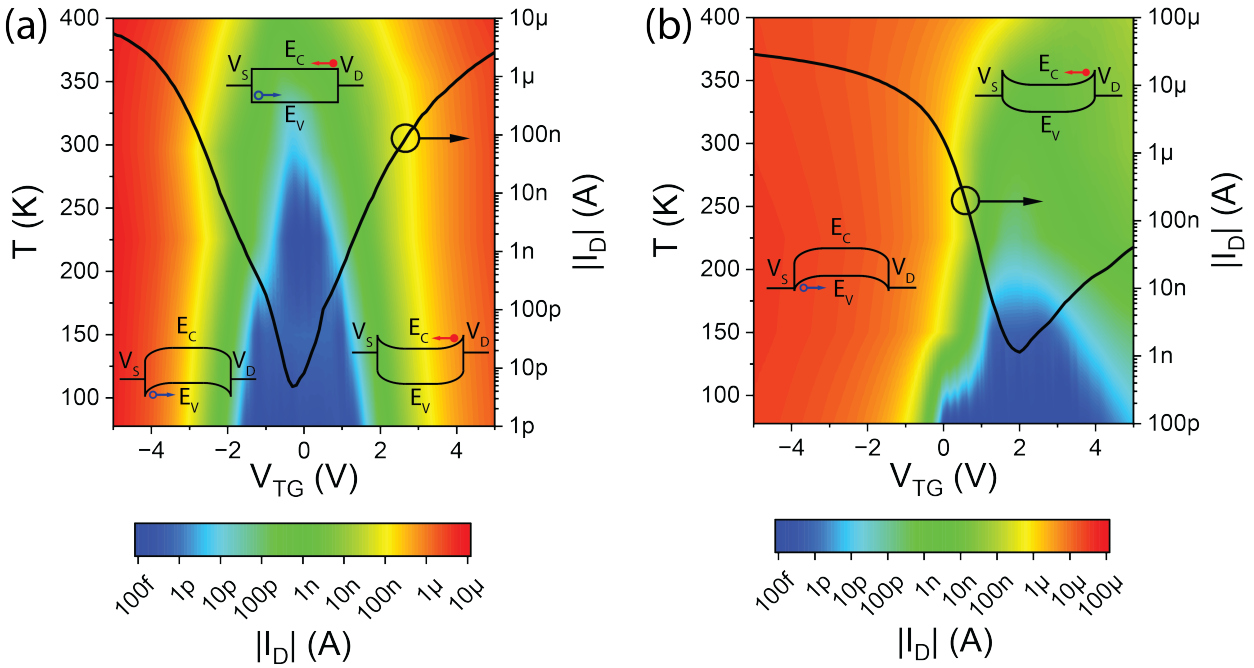

Figure 4: Temperature dependent transfer characteristic maps of an (a) Al-Si and an (b) Al-Ge SBFET at $V_{DS} = 1\,V$. The black curve belonging to the right y-axis shows the transfer characteristic at T = 295 K. The insets illustrate the band diagrams in the corresponding transport regimes.

For more detailed investigation, the output characteristics at different temperatures for the Al-Si and Al-Ge SBFET are analyzed in Figure 5. The inset in Figure 5a (Al-Si at T = 77.5 K) illustrates the three main contributions relevant for charge carrier injection. Here, TE is the contribution originating from charge carriers injected over the barrier into the semiconductor. Importantly, this contribution increases with elevated temperatures due to thermally excited charge carriers overcoming the barrier. Next, FE is considered, which is the contribution originating from the Fermi level pinning of the metal into the semiconductor through tunneling. Here, the charge carriers exhibit minimal potential energy, but are efficiently injected in case of high biases (here: $|V_{DS}| = 2\,V$ and $|V_{TG}| = 5\,V$) consequently

leading to strong band bending and thus thinner tunneling barriers enabling efficient injection of charge carriers trough tunneling. In this context the transmissivity in case of FE – and considering WKB approximation – T_{FE} is given as $T_{FE} \approx \exp\left(-\frac{4\sqrt{2m^*}\Phi^{3/2}}{3q\hbar\varepsilon}\right)$, where m^* is the tunneling effective mass, Φ is the Schottky barrier height and ε is the electric field, which directly influences the barrier width. Finally, TFE is a mixed transport mechanism of TE and FE, where charge carriers tunnel through the remaining SB. Again, applying higher biases, i.e. thinning the tunneling barrier, allows an efficient injection via this transport mechanism. The output characteristics of the Al-Si SBFET (cf. Figure 5a) again reveals a vertical ($V_{DS} = 0\,V$) and a horizontal ($V_{TG} = 0\,V$) symmetry axis, further proofing the symmetrical nature of the Al-Si system. At $T = 77.5\,K$ charge carrier transport is merely possible via TFE and FE, due to frozen out charge carriers not being able to overcome the barrier caused by the lack of thermal excitation. However, elevating the temperature thus thermally exciting charge carriers leads to carrier injection even at lower bias voltages. In comparison, the Al-Ge SBFET only exhibits one vertical symmetry axis at $V_{DS} = 0\,V$ due to its asymmetric Fermi level pinning. At $T = 77.5\,K$ only a negligible increase of the current with increasing $|V_{DS}|$ is observable, which is related to minimal thermal excitation and the dominance of the quasi-ohmic contact between Al and Ge. This behavior also gets evident considering the output maps at elevated temperatures, as V_{TG} does not influence the on-state of the p-branch significantly. In contrast the current in the n-branch increases due to the presence of a dedicated barrier and thus a more pronounced TE contribution in consequence of thermally excited charge carriers.

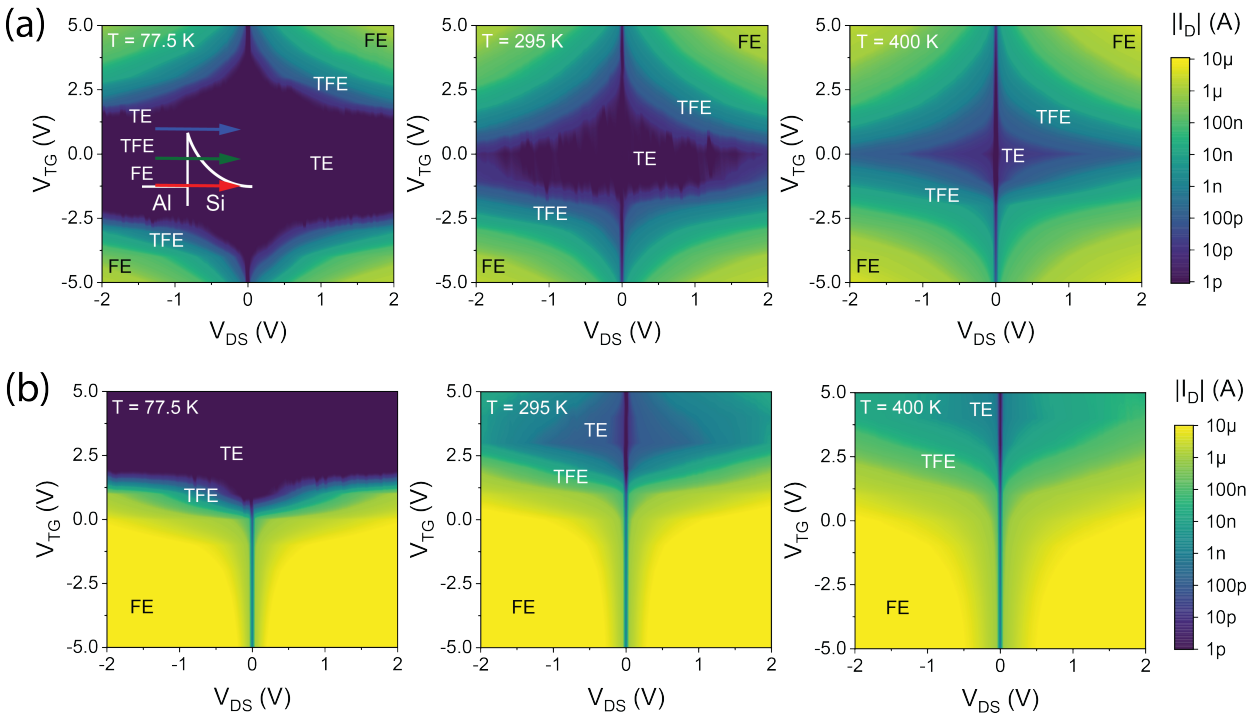

Figure 5: Output characteristic maps in dependence of the applied TG voltage V_{TG} at T = 77.5 K, 295 K and 400 K for an (a) Al-Si and an (b) Al-Ge SBFET. TE, TFE and FE regimes are didactically inserted at the corresponding regimes. The inset in (a) illustrates the transport mechanism for the Al-Si material system.

Finally, processing the output I/V data used in Figure 5, the activation energy of the material systems can be visualized (see Figure 6). The basis for the calculation is the TE current model adapted to be suitable for the experimental approach used here. Hence, the voltage between the metal and semiconductor cannot be considered due to the experimental setup and a simplified model needs to be applied, which is valid for an applied bias voltage exceeding $3k_BT/q$ (76 mV at T = 300 K). Consequently, $J_{TE}(T) = A^*T^2 \exp\left(\frac{-E_a}{k_BT}\right)$, where J_{TE} is the measured current density, A^* is the effective Richardson constant, T is the corresponding temperature and E_a is the total effective activation energy.[30] Note that this model does not allow to distinguish between the proposed transport mechanisms, as in the experimental setup the total current is measured and thus merely gives an estimation of E_a. Rearranging the equation accordingly, a Richardson plot is obtained allowing to deduce the activation energy, i.e. the energy required to inject charge carriers into the semiconductor. Using this approach, the V_{TG}-dependent intrinsic activation energy is obtained (cf. insets in Figure 6) by fitting E_a to $V_{DS} = 0$ V. Moreover, performing a separate measurement with a wider V_{DS} range and without fitting to $V_{DS} = 0$ V a map in dependence of V_{TG} and V_{DS} can be created as shown in Figure 6. As shown in the map and in the inset, the activation energy E_a of the Al-Si SBFET (cf. Figure 6a) exhibits positive values at any measured operation point, indicating barriers for electrons and holes, further demonstrating the relative midgap pinning of Al to Si. Remarkably, considering the intrinsic E_a (cf. inset Figure 6a) a vertical symmetry axis at $V_{TG} = 0$ V is visible. Especially in the off-state of the Al-Si SBFET a relatively high activation energy is evaluated corresponding well with previously shown results. In comparison the Al-Ge SBFET shown in Figure 6b exhibits negative E_a values for hole conduction, further supporting the exhibition of quasi-ohmic contacts in the p-branch.[31] Observing electron conduction at positive V_{TG} a dedicated barrier gets evident. Moreover, a shift of the off-state into the n-branch takes place, further enhancing the p-branch and thus favouring hole conduction. Additionally, the use of Al_2O_3 as gate oxide (cf. Figure 1b) is further pushing the Al-Ge SBFET in p-mode operation.

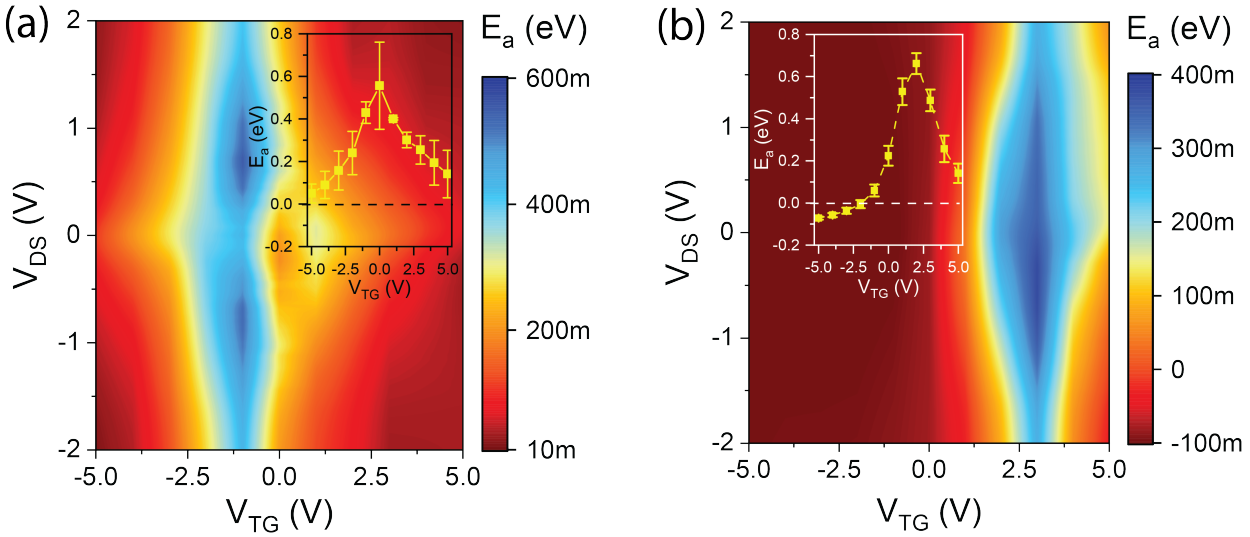

Figure 6: Activation energy maps deduced from output I/V data over temperature of the (a) Al-Si and of the (b) Al-Ge SBFET. The insets show the intrinsic activation energy in dependence of V_{TG}. The error bars represent the standard deviation of the measured data of three similar devices for both material systems.

Conclusions

In conclusion, we have analyzed Al-Si and Al-Ge based SBFETs in terms of temperature dependent bias spectroscopy and provide an in-depth analysis of the involved electronic transport mechanisms. Remarkably, using monocrystalline Al as drain/source contacts allows to compare the transport properties of Si and Ge SBFFETs. Importantly, output and transfer characteristic measurements and systematic evaluations allow to investigate the effects of Fermi level pinning, which in the Al-Ge SBFET leads to dominant p-type conduction and quasi-ohmic contacts for hole conduction, while Si based SBFETs show equal charge carrier injection capabilities of electrons and holes. Evaluating transconductance g_m and activation energy E_a maps, the influence of the Fermi level pinning is further supported and in detail analyzed. Most notably, the presented investigations of the bias and temperature dependent transport in Al-Si and Al-Ge nanojunctions contributes to a better understanding of metal-group IV based Schottky barrier field effect transistors, which are highly anticipated for the implementation of electronic device functionalities beyond the capabilities of conventional

field effect transistors and CMOS devices in general.

Methods

Si NW growth

The ⟨112⟩ oriented Si NWs were grown in a home-built, hot-wall chemical vapor deposition (CVD) system using silane (SiH_4, Voltaix), hydrogen chloride (HCl anhydrous; Matheson TriGas 5N research purity grade), and hydrogen (H2, Matheson TriGas, 5N semiconductor grade) as the carrier gas following protocols similar to those reported previously.[32] Au nanoparticle catalysts of diameter 80 nm (Sigma-Aldrich) were immobilized on growth substrates composed of Si wafers with 600 nm thermal oxide (NOVA Electronic Materials) by functionalization of the substrate with poly-L-lysine (Sigma-Aldrich) followed by functionalization with Au nanoparticles. Substrates were cleaned in a UV-ozone cleaner and inserted in a 1-inch quartz-tube furnace (Lindberg Blue M) for growth by CVD. NW growth was nucleated at 753 K with 2 standard cubic centimeter per minute (sccm) of SiH_4, 4 sccm of HCl, and 194 sccm of H_2 at 20 torr total reactor pressure for 20 min, and these conditions were maintained for an additional 80 min to reach the desired NW length of 20 µm. The Si NWs have diameters d_{NW} of ≈70 nm. Subsequent to the growth, the Si NWs were thermally oxidized at T = 1174 K in O_2 atmosphere for 3 min and annealed for another 3 min in N_2 atmosphere to employ a high-quality 9 nm thick SiO_2 gate oxide.

Ge NW growth

The Ge NWs were grown on Ge (111) single crystal substrates by low-pressure CVD in a cold-wall reactor. The substrates were placed on a graphite susceptor and the temperature adjusted by high frequency heating. Prior to use, the substrates were coated with a 1 nm thick Au film by sputtering. The Ge substrate was heated to 748 K under dynamic vacuum before diphenylgermane (DPG; 40 mg DPG reservoir at 295 K; process pressure < 10 mbar to 3 mbar) was introduced to the CVD chamber for 20 min to 30 min. The Au seeds act as catalytic sited for the precursor decomposition. DPG decomposition in absence of the

metal for substrate temperatures up to 774 K has not been observed, which prevents tapering of NWs in the investigated growth temperature window of 624 K to 774 K. Similar growth procedures using the same precursor under LPCVD conditions have been reported in literature.[33,34] After disconnecting the precursor supply and a 10 min waiting period, the substrates were cooled down to room temperature. The stability of the synthesized Ge NWs against degradation such as surface oxidation etc. over time and formation of very reliable interfaces in post-growth processing can be related to surface termination with phenyl ligands originating from the precursor. Similar effects have been described in the growth of Ge NWs using a co-feed of GeH_4 with GeH_3CH_3 leading to a reduced tapering tendency by surface termination with the alkyl ligands.[35,36] While Ge-H remains reactive and cleaves under reduced pressure, the stability of the Ge-aryl bond passivates the NWs surface. After the growth of the ≈70 nm thick Ge NWs, they were conformally coated with 10 nm of Al_2O_3 by atomic layer deposition at a temperature of T = 474 K.

SBFET fabrication

The passivated Si/Ge NWs were drop-casted onto a 100 nm thick thermally grown SiO_2 layer atop of a 500 µm thick highly p-doped Si substrate. Al contacts to the Si/Ge NWs were fabricated by a combination of electron beam lithography, 15 s of BHF (7:1) etching to remove the SiO_2-/Al_2O_3-shell at the contact area, 125 nm Al sputter deposition and lift-off techniques. A successive thermally induced exchange reaction by rapid thermal annealing at a temperature of T = 774 K / T = 674 K in forming-gas atmosphere initiates the substitution of Si/Ge by Al. After annealing, the semiconductor channel length was approx. 1 µm in length with a NW diameter of approx. 90 nm for the Si NWs and 40 nm for the Ge NWs (without passivation). Facilitating this heterostructure formation scheme allows the integration of single-crystalline monolithic Al-Si / Al-Ge NW heterostructures. The Ω-shaped Ti/Au top-gate covering the interfaces as well as semiconductor is fabricated, using a combination of electron beam lithography, Ti/Au evaporation (10 nm Ti, 100 nm Au), and

lift-off techniques.

BF and HAADF STEM

BF STEM was performed on Al-Si-Al NW heterostructures fabricated on 40 nm thick Si_3N_4 membranes using a probe-corrected FEI Titan Themis, working at 200 kV. The Al-Si interface in the shown images is viewed along the [110] direction of observation of the Si crystal. Martien: Description of Al-Ge interface investigations

Electrical measurements

The electrical measurements were performed using a combination of a semiconductor analyzer (HP 4156B) and a probe station. To minimize the influence of ambient light as well as electromagnetic fields, the probe station is placed in a dark box. For applying the bias voltage the following holds: $V_{DS} = V_D - V_S$ and $V_D = -V_S$. Temperature dependent measurements as well as measurements to extract the activation energy were performed in a vacuum using a cryogenic probe station (LakeShore PS-100) and a semiconductor analyzer (Keysight B1500A).

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R.B. and M.S. performed the device fabrication and conducted the electrical measurements. M.I.d.H and Z.S.M. carried out the TEM measurements and analysis. C.G.E.M. and J.C. have grown the used Si NWs. S.B. has grown the used Ge NWs. M.S. and W.M.W. conceived the project and contributed essentially to the experimental design. All authors analyzed the results and agreed on the manuscript. The authors gratefully acknowledge financial support by the Austrian Science Fund (FWF): project No.: I 5383-N. The NW synthesis was supported by grant DMR-2121643 from the U.S. National Science Foundation. The authors further thank the Center for Micro- and Nanostructures for providing the cleanroom facilities.

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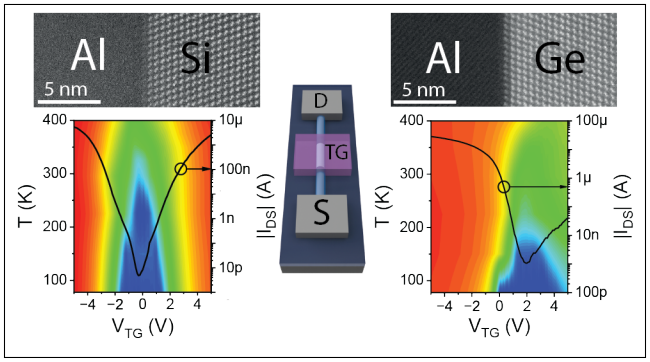
TOC Graphic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