A Pseudo-Adiabatic Switched-Capacitor Gate Driver for Si and GaN FETs Achieving >5x Power Reduction

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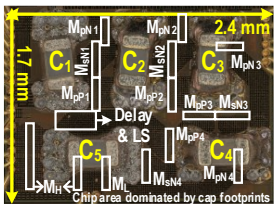
Conventional gate drivers use resistive or current-limited charging and discharging of reactive gate energy, resulting in hard-switching power loss – an important limitation on converter efficiency [1]-[4]. Shown in Fig. 1, this work uses a fast, tunable switched-capacitor (SC) converter to step the gate voltage waveform in smaller increments, reducing charge sharing losses through pseudo-adiabatic switching and recovering gate energy in flying capacitors. Using a 5-level SC driver, the design uses all low-voltage (1.2V 130nm SOI) CMOS to generate the stepped $5V_{pp}$ gate waveform from a ~1V supply. By using fast control and sub-ns tunability of each switching step, the design achieves 2-7x reduction in gate drive power while still maintaining fast gate and drain voltage rise/fall times (slew rates). The SC stage timing is used to mitigate (parasitic) gate loop inductive effects, ringing, and overshoot, providing different modes of operation that allow new opportunities and tradeoffs between power savings switching transient speed.

Shown in Fig. 2, the SC converter operates in 6 switching states: in S0, all parallel switches (blue) are on; V_G is shorted to 0V by M_L (the power FET is off). In S1, M_H turns on, connecting V_G to V_{IN}. In S2, M_{sN1} turns on such that $C_{2..5}$ are in series with V_{IN} to drive V_G to $2V_{IN}$. In successive states S3..5, the flying capacitor array is switched in binary segments, stepping V_G in integer increments up to $5\times V_{IN}$. Step-down is the reverse of step-up such that charge returns to $C_{1..5}$ until V_G=0V. While conceptually similar to [5], this design is over 1000x faster with sub-nS tunability of switching steps; the binary switching scheme for the small (01005 die attach) capacitors can be shown to maximize capacitor utilization, such that the summed volume (energy) of all $C_{1..5}$ capacitors is no more than would be required for the bootstrap capacitor of a conventional gate driver. Smaller voltage steps reduce impulsive hard-charging (CV^2) loss by the number of steps. During discharge (turn off), the flying capacitors recover a large fraction (up to 80%) of gate energy. For comparison, we use the metric *power reduction factor* PRF; higher PRF indicates the reduction in *real supply power* P_{IN} relative to a conventional hard-switching gate driver.

An important feature of this work is the high-resolution tunability of each switching step, illustrated in Fig. 2. The rise and fall times are set by durations $t_{1..4}$ and $t_{5..8}$ respectively, each duration set by an independent 5-bit delay line with step size (per-tap resolution) from ~50ps to 5ns. By tuning $t_{1..8}$ independently, the SC gate driver can provide quantized shaping of V_G and/or control the gate waveform. In low-Q scenarios (low L_P or high R_G), the driver can operate in fast- and slow-switching limits (FSL/SSL) with a tradeoff between the faster rise time (FSL) and higher power savings (SSL: max PRF~5). Switch timing can also be adjusted near Miller-plateau levels to moderate V_{DS} slew rates depending on the threshold voltage.

In high-Q (high L_P, low R_G) scenarios, switch timing can be adjusted to reduce or eliminate inductive ringing (overvoltage of V_G), but can also provide other benefits. Specifically, adjusting $t_{1..3}$ allows the converter to operate in different modes. In ultrafast (UF) mode, timing intervals $t_{1..3}$ are short such that gate current I_G (which flows through parasitic nH-range gate inductance, L_P) ramps up quickly, maximizing the V_G slew rate. Interval t_4 is adjusted such that I_G resonates to zero and the last step happens when the gate voltage reaches its final value (eliminating overshoot). While the slew rate is fast, RMS current is high, resulting in lower power savings (PRF). In constant peak current (CPC) mode, $t_{1..4}$ are adjusted such that peak current is the same in each stepping interval – reducing RMS current and increasing power savings but with longer rise time. In zero-current-switching (ZCS) mode, each step is tuned to leverage resonance of L_P with C_G to minimizing gate driving loss but with longer rise time. Thus the topology allows tradeoffs between gate and drain slew rates and power savings, which can be optimized for different scenarios.

Shown in Fig. 3, to circumvent static-CMOS (or RC) delay limitations, the design uses a tunable 32-stage domino-delay-line multiplexor structure. Reset by synchronous CLK signal, when $\bar{S}_i$ falls, M_{PD} turns on with pull-down strength set by V_{DDA}, discharging parasitic capacitance at the floating node, the unit delay passing down the domino chain, pulling up delay signals $S_{d<1:32>}$ which are recovered to full logic levels by dynamic inverters. These pass to two-stage 32:1 multiplexors setting each of the four $t_{1..4}$ and $t_{5..8}$ timing intervals for step up/down gate signals. Thus, delay resolution (base time) is set by V_{DDA} with 5b digital control setting times $t_{1..4}$ and $t_{5..8}$. Low logical effort of the domino circuit allows fast but accurate delay generation with down to ~50ps tunability.



Die micrograph.

To maintain extreme low-latency and low-skew timing of floating switching cells, a single-input-dual-output (SIDO) level shifting scheme was used to pass the control signals for floating switches in different domains. The pulse-latch-based level shifter uses a single cascode structure with multiple outputs: $V_{aL/bL}$ w.r.t. $V_{P,k}$, and $V_{aH/bH}$ w.r.t. $V_{P,k+1}$. Thus, on switching, the same pulse triggers latches for switches M_{pN} (SP_L in k^{th} domain) and M_{sP}/M_{pP} (SP_H in the k+1th domain) to ensure reliable and fast switching. Using all low-voltage (1.2V-rated) devices, switching cells are powered directly from flying capacitors and floated in deep-trench SOI wells. Powertrain switches are sized for net pull-up/down resistance $R_{PU/PD} \approx 0.3\Omega/0.1\Omega$ respectively; low resistance allows for high peak drive currents (>3A *average* pull-up) and strong off-state holding.

Fig. 4 shows measured transient waveforms and power consumption when driving the low-R_G GaN FET (EPC2067). Double pulse testing explores both gate and drain loop considerations. To benchmark, the LTC4440 was used for comparison as it allows isolated measurement of gate power separate from quiescent bias power. Both test setups use identical layouts but have a modest, yet unavoidable parasitic gate loop inductance (L_p ~2.5nH); while the LTC4440 uses resistance to damp inductance, the proposed circuit uses voltage step tuning to minimize overshoot. The switching modes and tradeoffs described in Fig. 2 were also explored and characterized.

In double-pulse testing, UF mode achieved gate rise times of ~10 ns (drain fall time ~1.8ns) for Q_G ~ 20nC without inductive overshoot (~2x faster than LTC4440). Importantly, this was achieved while cutting gate-drive power in half (PRF~2x) relative to the hard switching gate driver. With slightly slower transitions, CPC mode achieved gate rise times of ~18ns (2.8ns drain fall time) with ~3x reduction in gate drive power. Using ZCS mode (maximally leveraging resonance of the SC stage with L_p), gate risetime is ~40ns (~8-10ns drain fall time) but reducing power by 7x. Fig. 5 shows example testing with a large (Q_G~50nC) SiFET in a buck converter configuration with and without zero-voltage switching (ZVS). Due to high gate resistance R_G~2Ω (internal to the device), the gate loop inductance L_P is sufficiently damped such that the SC driver operates in SSL-FSL regimes. Differences in power savings arise due to location of the miller plateau, leading to slightly higher benefit when the power device is switched at zero V_{DS} (ZVS). At comparable rise times to the LTC4440, gate drive power is half (PRF~2) without ZVS and one third (PRF~3) with ZVS. In SSL (slower rise time) PRF increases to ~3-5 depending on ZVS (which impacts Miller charge and associated power savings).

The design is implemented in 130nm RF SOI CMOS with die area ~4.1mm^2 (mainly limited by die-attach 01005 capacitors; total utilized active area is < 1.5mm^2). Shown in Fig. 6, compared to previous work, this work achieves between 2-7x reduction in gate drive power (depending on scenario and operating mode). Importantly, it is able to do this while achieving rise/fall times (gate and drain slew rates) comparable to SOA gate drivers, even when tested with relatively larger (higher Q_G) Si and GaN devices. While some prior works test with higher voltage devices this has minimal impact on gate drive characterization. Thus, the advantages of tunable multi-level SC gate driving may extend to a number of applications, converters and power device technologies.

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References:

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[3] S. -Y. Li *et al*., ISSCC, 2023.
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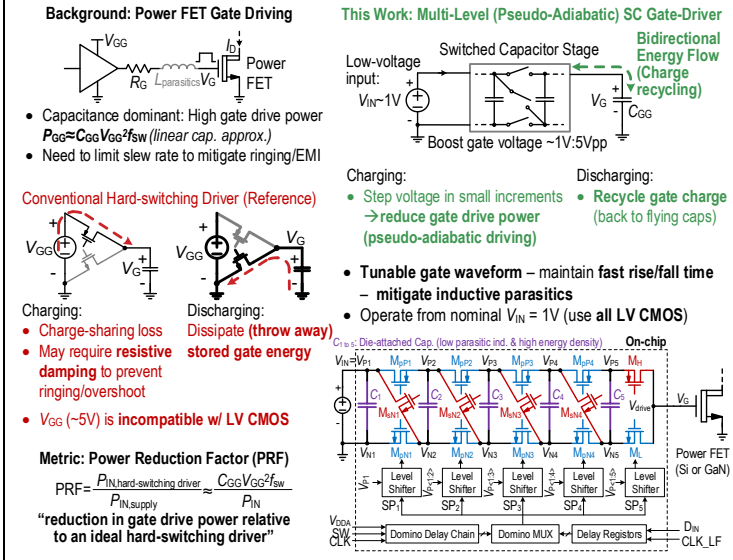


Fig. 1. High-level architecture and gate drive considerations

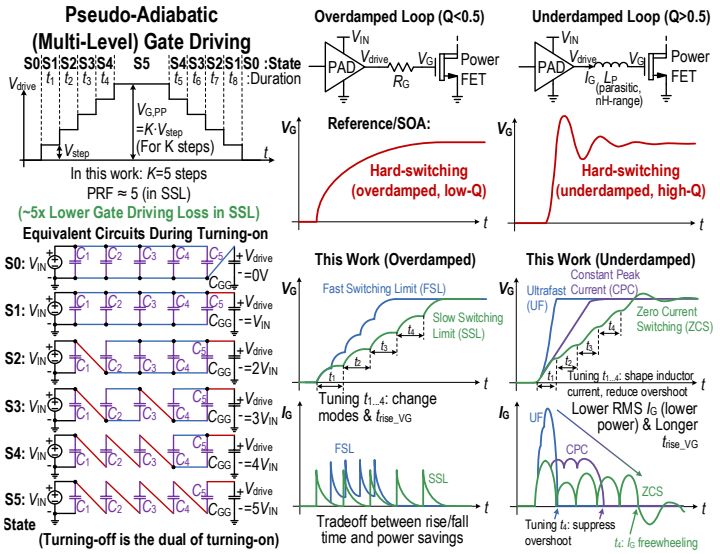


Fig. 2. Gate drive tunability: SSL, FSL and resonant timing

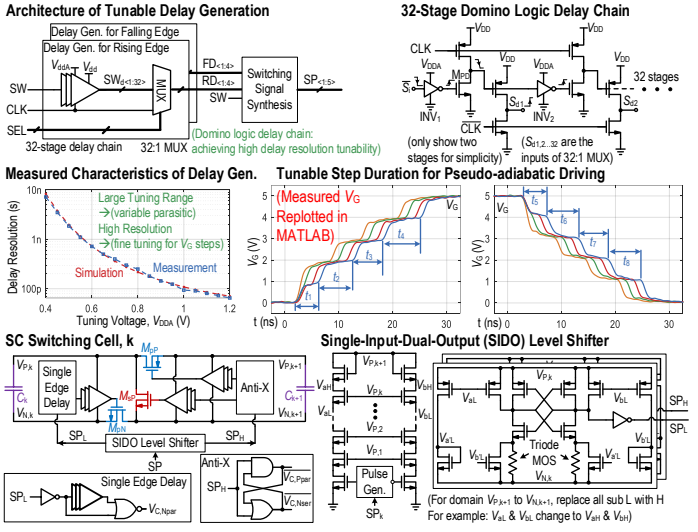


Fig. 3. Delay generation, gate waveform control and single-input-dual-output level shifter

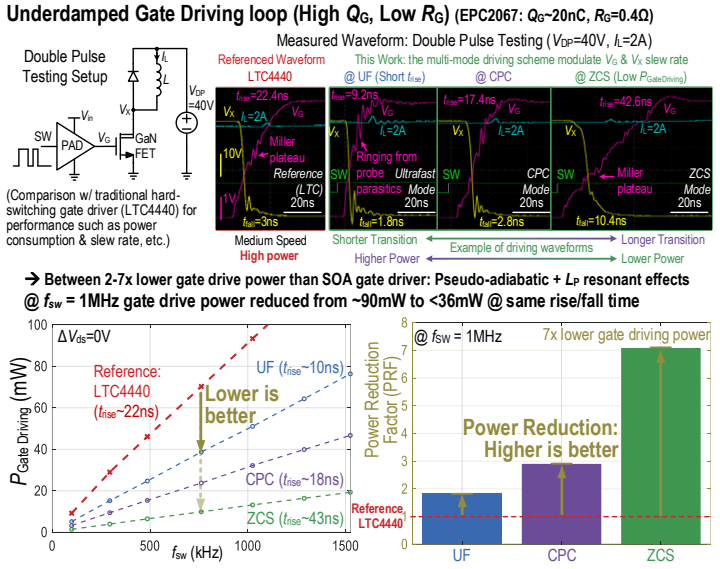


Fig. 4. GaN FET: transient waveforms and power reduction factor

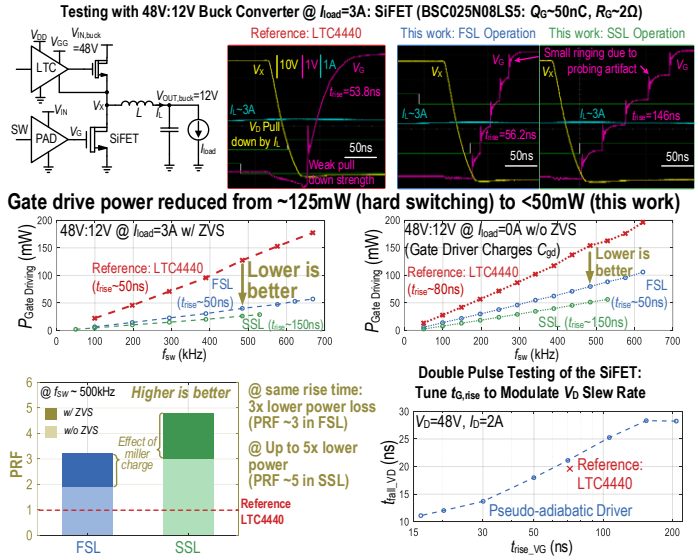


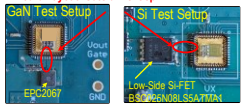
Fig. 5. Testing 48V:12V buck: results and power reduction.

Spec	[1] Seidel ISSCC18	[2] Ke ISSCC16	[3] Li ISSCC23	Reference Gate Driver	This work
Highlighted features	3-level, soft-charging, HV cap energy storage	Bootstrap balancing, t_{dead} modulation	High CMTI isolated gate driver	Hard-switching Driver (LTC4440)	Multi-Mode Pseudo-adiabatic driving
Technology	180nm BCD	350nm HV BCD	GaN-on-Si	N/A	130nm RF-SOI
Power Device	Discrete GaN	Discrete GaN	Discrete SiC	Discrete GaN & Si	Discrete GaN & Si
V_G up slew	7.1V/7.9ns(1,3) (0.9V/ns)	5V/2ns(1,3) (2.5V/ns)	26V/200ns(1,3) (0.13V/ns)	5V/22.8ns (0.22V/ns)	5V/9.2ns(3) (0.5V/ns)
Q_G up slew ($I_{G,ave,max}$)	11.6nC/7.9ns(1) (1.5A)	0.13nC/2ns(1) (65mA(1))	N/A	49nC/53.8ns (0.9A)	49nC/15ns (3.3A)
$Q_{G,max}$	11.6nC	0.13nC	N/A	49nC	49nC
V_{ds} down slew rate	80V/2.8ns (29V/ns)	40V/1.2ns (33V/ns)	1.7kV/200ns(1) (8.5V/ns)	40V/3ns (13V/ns)	40V/1.8ns(4) (22V/ns)
PRF	N/A	0.51(2)	N/A	0.96(2,5)	~7 (high-Q loop) ~5 (low-Q loop)

(1) Estimated from reported data and plots;
(2) Estimated PRF w.r.t. reactive power calculated by $Q_{gs}V_{gs}f_{sw}$;
(3) V_G slew rate depends on the total gate charge of the power FET under test and the driver output impedance, here only consider the voltage slew rate;
(4) V_{ds} slew rate depends on the power FET under test, ΔV_{ds}, and parasitic in the testing set-up;
(5) LTC4440 has PRF close to the ideal hard-switching driver (PRF=1), which makes it a good reference

Devices	Series Number	Specifications
Flying capacitor	GRMMDXR60J105ME05	015008, 6.3V, C_{eff}=796nF (derated to 1V), 0.03mm³
Power GaN FET	EPC2067	40V, V_{th}=1V, R_G=0.4Ω, 4.8mm³ @ V_{gs}=5V: $R_{ds,on}$=1.55mΩ, Q_G=17.1nC
Power Si FET	BSC025N08LS5ATMA1	80V, V_{th}=1.7V, R_G=1.7Ω, 30mm³ @ V_{gs}=4.5V: $R_{ds,on}$=2.6mΩ , Q_G=44nC

Board Layout: Gate drive loop



- Small gate loop w/ L_P ~ 2.5nH;
- GaN FET is high-Q → can leverage resonant effect;
- Si FET has high internal R_G ~ 2ohm → FSL/SSL operation (limits $t_{rise/fall}$)

Fig. 6. Comparison to past work and components list