A Miniaturized Platform for a Modular High-Voltage Electrostatic Actuator Driver

Yanqiao Li
Thayer School of Engineering
Dartmouth College
Hanover, USA
Yanqiao.Li.TH@dartmouth.edu

Bahlakoana Mabetha
Thayer School of Engineering
Dartmouth College
Hanover, USA
Bahlakoana.Mabetha.TH@dartmouth.edu

Jason.T.Stauth
Thayer School of Engineering
Dartmouth College
Hanover, USA
Jason.T.Stauth@dartmouth.edu

***Abstract*—High voltage drivers are needed for electrostatic and piezoelectric actuators in small-scale electromechanical systems such as microrobotics and haptics. This paper presents a miniaturized platform for a modular switched-capacitor-based driver, implemented in a 180 nm HV-SOI CMOS integrated circuit (IC), that uses less than 5 μA quiescent current per chip and includes an auxiliary (magnetic) boost converter to interface with low-voltage ($\sim$2.5 - 3.7 V) batteries. The platform allows multiple PCB modules to stack in series voltage domains, extending drive voltages to the kilovolt-range, beyond the process and buried-oxide (BOX) limits of a single chip. Compared to past work with the same IC [1], the improved platform achieves >100$\times$ volume reduction and >30$\times$ weight reduction; with eight boards stacked, the system can provide peak-peak drive voltages up to 3 kV from a 3.7 V supply (voltage conversion ratios VCR > 800), delivering and recovering $\sim$1 W reactive power with over 97% efficiency.**

***Index Terms*—DC-DC Converter, switched capacitor, boost converter, piezoelectric actuator.**

I. Introduction

Ultralight-weight, small-volume, high-voltage (HV) drivers for electrostatic actuators including piezoelectric, silicon microelectromechanical systems (MEMs) and dielectric elastomers are needed for a variety of applications including robotics, haptics, and ultrasound [2]–[5]. Electrostatic force transducers require high drive voltages (often hundreds of volts to kV) to charge the bulk dielectric of the actuator [6]. As only a small fraction of the stored electric-field energy is used for mechanical force transduction and high-quality actuators have relatively low resistive or dielectric loss, these actuators present as dominantly capacitive [7], and require a large magnitude of reactive power relative to the real power used for mechanical work or dissipated as loss [6]–[8].

In many applications, including small-scale robotics, the actuator-drive system may be constrained to small size ($<1\,\mathrm{cm}^3$) and weight (<1 g), yet may require operation from low-voltage primary (2.5-3.7V) batteries. This motivates a need to achieve very high voltage conversion ratios (VCRs) in order to provide the high drive voltage required by the actuator technology. Past work has also outlined the need to achieve efficient delivery and recovery of reactive energy [9].

This work was funded in part by the Defense Advanced Research Projects Agency (DARPA) under award number HR001119C0040 and the National Science Foundation (NSF) under award number 2216552.

Electrostatic drivers have significantly different performance criterion than conventional DC-DC and DC-AC power converters, which provide mainly real power to the load. To better capture the benefits and quantify the performance when delivering predominantly reactive power, alternative metrics have been proposed [10]:

$$Q_{\mathrm{X}} = \frac{P_{\mathrm{X}}}{P_{\mathrm{loss}}},\ \eta_{\mathrm{X}} = \frac{P_{\mathrm{X}}}{P_{\mathrm{X}} + P_{\mathrm{loss}}} = \frac{Q_{\mathrm{X}}}{Q_{\mathrm{X}} + 1}, \tag{1}$$

where Q_{X} is termed the *effective quality factor* and η_{X} is the *reactive power efficiency* of the driver. In (1), $P_{\mathrm{X}} = C_{\mathrm{X}} V_{\mathrm{drive}}^2 f_{\mathrm{drive}}$ is the reactive power processed by the converter, where C_{X} is the capacitance of the load, V_{drive} is the peak-to-peak output voltage swing, f_{drive} is the frequency of the load charging-discharging cycle, and P_{loss} is the total power loss of the converter. Effective quality factor Q_{X} captures the delivery and recovery of reactive energy (like in a resonant system) and is higher if real power loss in the driver is small. Metric η_{X} quantifies the efficiency of delivering (and recovering) reactive power to provide a perspective similar to real power efficiency which is bounded by 100%.

Past work in the actuator-driver space includes hard-switching drivers and linear amplifiers [11]–[14], magnetic-based unidirectional [15]–[17] or bidirectional boost converters [18], [19] and reconfigurable switched-capacitor (SC) converters [9], [20]. Ideal hard-switching or linear amplifier drivers do not have a mechanism to deliver or recover reactive power efficiently and are limited to $Q_{\mathrm{X}} < 1, \eta_{\mathrm{X}} < 50\%$. Unidirectional drivers can charge capacitive loads efficiently, but can not recover energy, such that $Q_{\mathrm{X}} < 2, \eta_{\mathrm{X}} < 66.7\%$. While bidirectional drivers based on magnetic boost converters are feasible, these are challenging due to the need for high-voltage bidirectional switches and poor scaling of magnetic components to small size. Finally, past work on reconfigurable switched capacitor drivers [9], [20] did not provide an interface to low voltage batteries or scalability beyond the process limits of a given semiconductor technology.

This work builds on a recently published, bidirectional switched-capacitor-based actuator-drive IC that included an auxiliary boost converter to interface with low-voltage primary batteries [1]. The IC uses a 180 nm deep-trench SOI CMOS integrated circuit with an active area-to-handle wafer (burried-

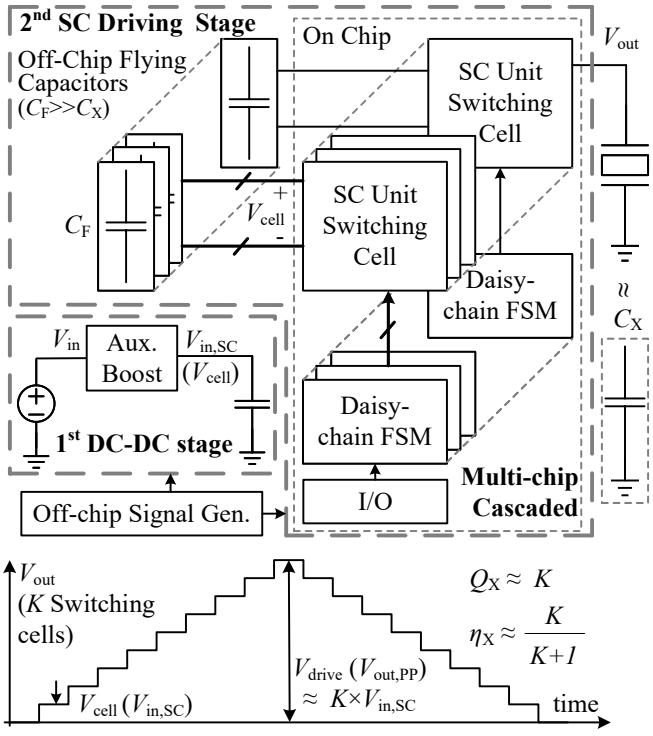

Fig. 1. High-level architecture and operation.

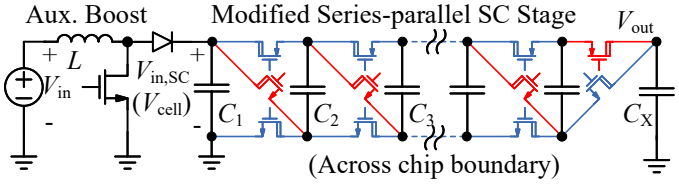

Fig. 2. The power train of the driver: auxiliary boost drives a modified series-parallel SC converter.

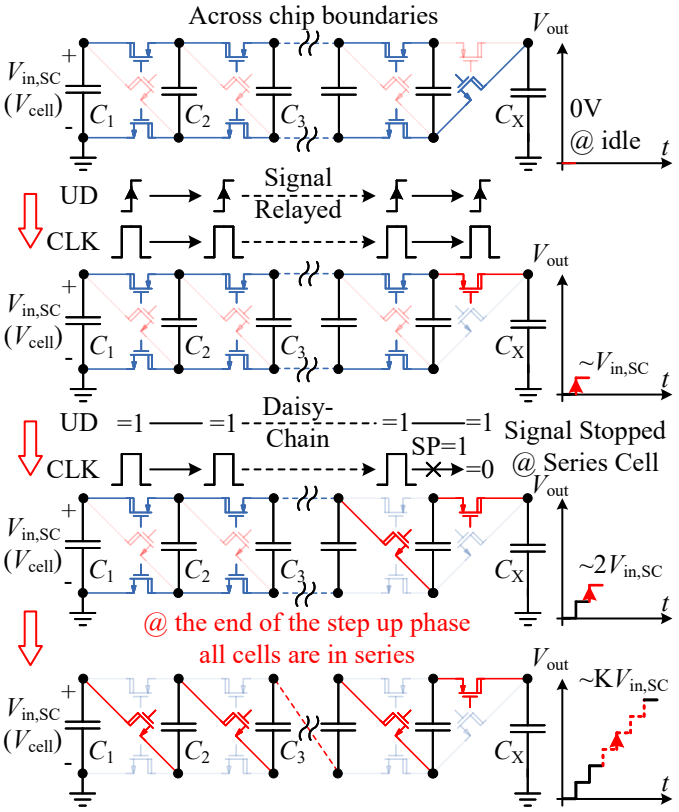

Fig. 3. Switching cells sequentially switch to series state during step up phase according to the control signal relayed through the daisy-chain.

oxide BOX) process voltage rating of 400 V. The chip is designed to be stacked in series voltage domains to increase the addressable voltage range of the converter, extending beyond the BOX breakdown limit, with switching control passed up the SC-chip stack through a daisy-chain communication network. While details of the IC were presented in [1], this paper presents a significantly improved PCB interposer platform which reduces size and weight, while allowing scalability to higher voltages. Further test and implementation results are also provided, outlining the benefit of the bidirectional SC + auxiliary boost, chip-stackable converter.

II. Two-Stage Hybrid Actuator Driver

A. Architecture Overview

Fig. 1 shows the high-level architecture of the two-stage driver system [1] which includes an auxiliary boost converter to drive a bidirectional series-parallel SC voltage multiplier. The SC stage is designed to 'stack' or connect in cascade with additional chips to extend voltage multiplication to higher voltage levels. The IC includes on-chip switches, gate driving, level shifting, distributed control, biasing and I/O circuitry. With off-chip passive components, the auxiliary boost converts the battery voltage ($V_{\text{in}} \approx 2.5 - 3.7\,V$) to an intermediate voltage ($V_{\text{in,SC}} \approx 20 - 30\,V$), which is the input voltage of the SC stage. The SC stage uses sequential series-parallel reconfiguration of the flying capacitors to multiply $V_{\text{in,SC}}$, driving the actuator voltage in small steps.

Fig. 2 shows a simplified schematic of the SC + boost converter. Each of the switching cells comprises three switches, which control the series/parallel state of a single flying capacitor. Each flying capacitor can be independently switched in parallel (blue switches on) or series (red switch on) with adjacent flying capacitors in the stack. By sequentially switching to series during step-up, or parallel during step-down, the converter steps the actuator voltage in small increments $\Delta V_{\text{out}} \approx V_{\text{in,SC}}$ (waveform shown in Fig. 1), which reduces hard-charging loss ($C\Delta V^2 f$) and allows flying capacitors to recover a large fraction of the electric-field energy stored in the actuator during step down. As discussed in [1], [9] this can be described as a pseudo-resonant (or pseudo-adiabatic) driving process for dominantly capacitive loads.

B. SC-stage + Boost Converter Operation

Fig. 3 illustrates the operation of the multi-chip SC driver during the step up phase. Control signals UD (Up/Down) sets whether the converter is stepping up or down; CLK (clock)

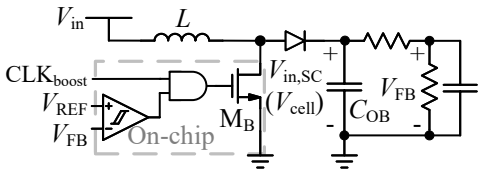

Fig. 4. The auxiliary boost is controlled by a comparator with hysteresis.

triggers the up/down switching events; SP (Series/Parallel) indicates whether the next SC cell is in the series or parallel state. These signals are relayed though the daisy-chain up and down the stack and are used by distributed finite state machine (FSM) controllers in each cell to synchronize switching.

In Fig. 3 (top), all flying capacitors are in parallel (blue switches on) and $V_{\rm out} = 0$ V. With UD set to 1, at the rising CLK edge (each relayed through the daisy chain), the last SC switching cell switches to series and $V_{\rm out}$ steps to $\sim V_{\rm in,SC}$. With UD held at 1, at each successive CLK edge, this process repeats with each SC cell sequentially switching to series and $V_{\rm out}$ increases by $\sim V_{\rm in,SC}$ at each step until $V_{\rm drive} \sim K \cdot V_{\rm in,SC}$, where K is the total number of switching cells. The step down process follows the reverse switching sequence: after UD switches to 0, the switching cells switch to the parallel state one-by-one in the reverse order of step up. In ideal slow-switching limit (SSL) operation, neglecting biasing and control power in the SC stage and loss in the boost stage, the ideal performance metrics from (1) follow as:

$$Q_{\rm X} \approx K,\ \eta_{\rm X} \approx \frac{K}{K+1}. \tag{2}$$

Shown in Fig. 4, the auxiliary boost converter provides the input voltage, $V_{\rm in,SC}$, of the SC stage and provides a first (regulated) voltage conversion step, allowing the converter to operate with low voltage inputs, $V_{\rm in} \sim$ 2.5 - 3.7 V. The boost converter operates in a discontinuous burst-mode operation, synchronized with a clock signal, $\rm CLK_{boost} \sim$ 1 MHz. The output of the boost stage $V_{\rm in,SC}$ is divided down and compared to reference voltage $V_{\rm REF}$. With the addition of a hysteresis band, the comparator sets the upper bound and lower bound of the $V_{\rm in,SC}(t)$ to be $V_{\rm cell,max}$ and $V_{\rm cell,min}$, respectively, as shown in the Fig. 5. At time t_0, $V_{\rm in,SC}$ is lower than $V_{\rm cell,min}$, $\rm M_B$ is turned on when $\rm CLK_{boost}$ goes high to magnetize the inductor. When $\rm CLK_{boost}$ goes low, the inductor is demagnetized to charge $C_{\rm OB}$. This operation repeats until $V_{\rm in,SC}$ is higher than $V_{\rm cell,max}$ at time t_1. $\rm M_B$ is kept off and $C_{\rm OB}$ discharges until $V_{\rm in,SC}$ is lower than $V_{\rm cell,min}$, time t_2 at which point the auxiliary boost starts to work again. Since the auxiliary boost only turns on when $V_{\rm in,SC}$ is lower than a threshold value, burst mode operation helps the converter maintain high efficiency across a wide load range with low quiescent power.

C. Performance Impact of the Auxiliary Boost Converter

Fig. 6 shows the general model for the two-stage driver from Fig. 2 where the output of the boost converter is the input of the SC stage. In two-stage operation, the boost converter

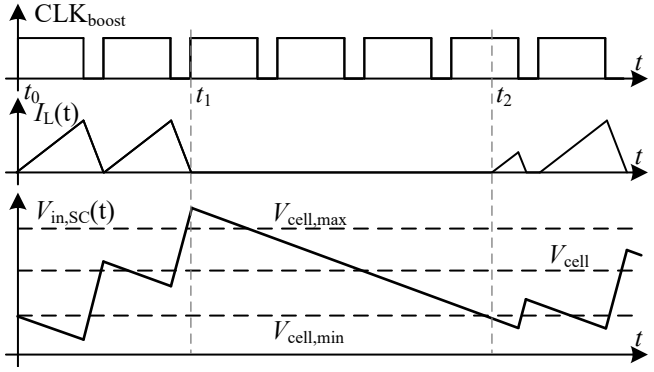

Fig. 5. The representative waveform of the burst mode auxiliary boost.

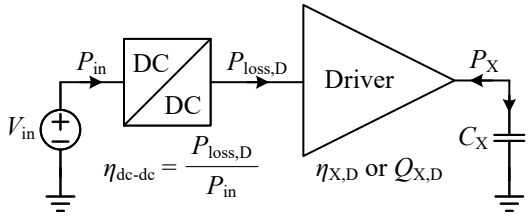

Fig. 6. A general model of a two-stage hybrid driver with its first stage achieving dc-dc voltage conversion and the second stage process the reactive power flowing between the load and the driver.

provides power to 'recharge' flying capacitors as needed when they are in parallel with the boost output. The power required to recharge these capacitors is the *real power* or loss $P_{\rm loss,D}$ of the SC stage when providing reactive power $P_{\rm X}$ to the load.

Considering the general model in Fig. 6, the impact of the boost converter efficiency is easily calculated. Here we treat the first stage as a generic DC-DC converter with real power efficiency $\eta_{\rm dc-dc}$ which is the ratio of the real power loss of the driver stage $P_{\rm loss,D}$ to real input power $P_{\rm in}$, drawn from the system power supply $V_{\rm in}$. Using (1), the combined metrics of the two-stage driver can be expressed as:

$$Q_{\rm X,tot} = \frac{P_{\rm X}}{P_{\rm in}} = Q_{\rm X,D} \cdot \eta_{\rm dc-dc}, \tag{3}$$

$$\eta_{\rm X,tot} = \frac{\eta_{\rm dc-dc} \cdot \eta_{\rm X,D}}{1 - \eta_{\rm X,D} + \eta_{\rm dc-dc} \cdot \eta_{\rm X,D}}, \tag{4}$$

where $Q_{\rm X,D}$ and $\eta_{\rm X,D}$ are the effective quality factor and reactive power efficiency of the SC driver stage. Combining this with the ideal expressions in (2), these go as:

$$Q_{\rm X,tot} \approx K \cdot \eta_{\rm dc-dc}, \tag{5}$$

$$\eta_{\rm X,tot} \approx \frac{K \cdot \eta_{\rm dc-dc}}{1 + K \cdot \eta_{\rm dc-dc}}. \tag{6}$$

Thus, (5) and (6) show that the boost converter efficiency penalty is reduced by the SC stage which efficiently delivers and recovers reactive power. Another way to view this is that the boost efficiency only impacts real power (loss) in the driver stage; if reactive power is supplied efficiently (with low-loss, or high $Q_{\rm X}$), then the overall impact on system power

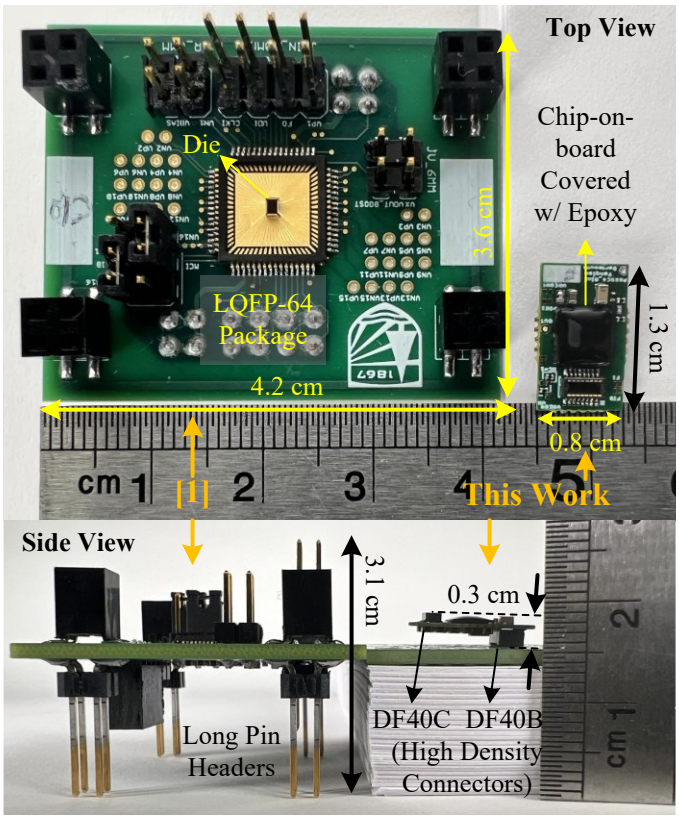

Fig. 7. Size comparison of assembly in this work to assembly in [1]

loss of the boost converter is small. For example, as will be shown later, for a driver (4-chip cascaded SC converter) with $\eta_{\mathrm{X,D}} = 97.7\%$ ($Q_{\mathrm{X,D}} = 42$), factoring in the efficiency of the dc-dc stage (auxiliary boost converter) of 85.9%, the reactive power efficiency of the overall converter drops to 97.3%, or only 0.4% lower than the SC stage alone. While this efficiency penalty is minor, the boost converter provides the additional advantages of allowing operation with low- and variable-voltage inputs, it provides a portion of the overall voltage conversion ratio (VCR) of the converter, and provides regulation of the $V_{\mathrm{in,SC}}$ input voltage.

III. Implementation and Assembly

Fig. 7 shows a comparison of the printed circuit board (PCB) interposer assembly of this work compared to the assembly used in [1]. A major difference is the significantly ($>100\times$) smaller volume and ($>30\times$) lower weight of the per-chip interposer module. Size and weight reductions were achieved using chip-on-board assembly of the integrated circuit and small form-factor, 2 mm-tall, 0.4 mm-pitch high density connectors DF40B (receptacle) and DF40C (plug). These connectors are used for board-board stacking to achieve modular high-voltage driving. Additional size reduction was achieved with fewer test pins, the use of blind vias and an overall more streamlined board layout.

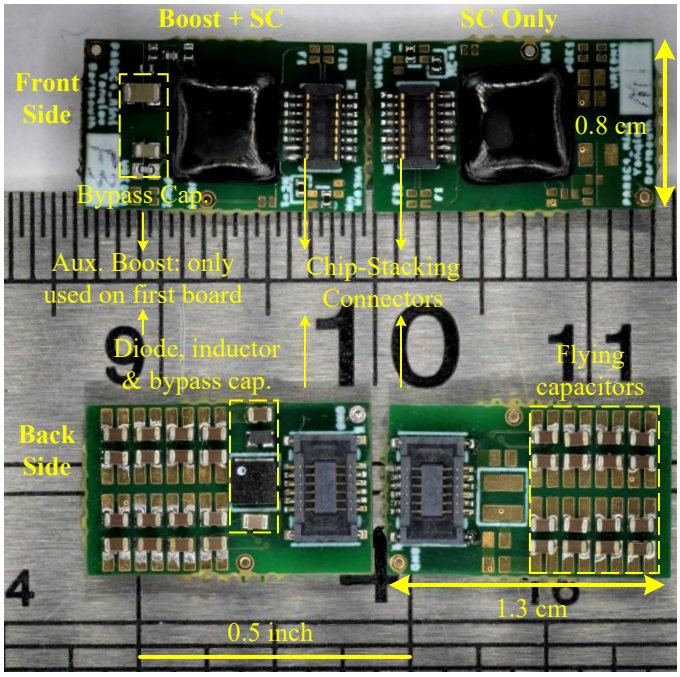

Fig. 8. The two sides of the 1 cm^2 interposer for the converter.

A. Assembly Details

Fig. 8 shows the top and bottom of the assembled platform. Each PCB interposer includes the custom IC with a 16-stage SC converter and off chip flying capacitors. The IC is mounted chip on board and epoxy covered requiring only 20 mm^2 and 1 mm height. Off chip passive components include 16×0402 capacitors (GRM155R61E225KE11D: 207 nF derated at 25 V) for the SC stage (one being a bypass capacitor for the first cell). Since each switching cell only needs to process 20 to 30 V ($V_{\mathrm{in,SC}}$), flying capacitors can be closely spaced without high-voltage breakdown or arcing issues. The boost converter passive components include an inductor (XPL2010, 100 μH, 8.5 Ω), diode (BAS40L 0402), bypass capacitor (0603, 27 μF). However, when stacking chips (connecting board assemblies as in Fig. 9), only the first chip assembly requires the boost converter (the remaining chips in the multi-board stack only require the SC stage) so the boost converter does not add much to the overall weight and volume. The weight breakdown of the assembled board is shown in Table I. It is seen that the interposer itself still dominates the weight; the connectors and epoxy coating on the die are also major contributors. Overall, the passive components themselves are relatively minor contributors to overall system size and weight. Thus there is still significant room to reduce the overall size with a smaller/thinner interposer and assembly strategy.

B. Assembly Connections and Operation

Fig. 9 shows an example of a 4-board stackup. The high density connectors are used for signal and power forwarding as well as mechanical support for the stackup. The input power source (V_{in} and GND) and off-chip control signals (UD,

TABLE I
WEIGHT BREAKDOWN FOR THE ASSEMBLY.

Component	Note	Weight
Components for SC Stage	16x Flying capacitors	~50 mg
Components for Aux. Boost	Inductor, diode, bypass capacitors, etc	~40 mg
Connectors	Plug and receptacle	~60 mg
Chip	Die and epoxy	~30 mg
Bare interposer	4-layer FR4, 0.5 mm-thick, 1 oz Cu	130 mg
Total SC only	One assembled board	270 mg
Total SC+Boost	One assembled board	310 mg

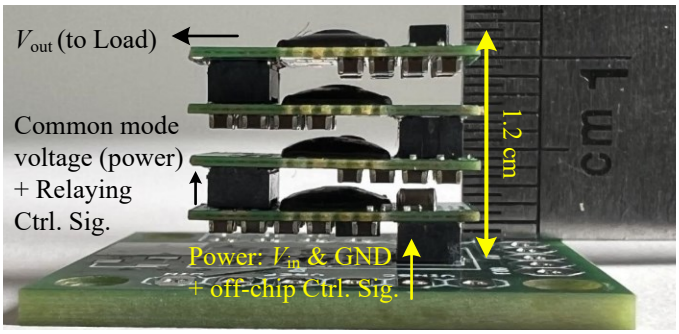

Fig. 9. Photo of 4-board stack, which can achieve 3.7 V-to-1.5 kV conversion.

CLK, $\text{CLK}_{\text{boost}}$, etc) are connected from the bottom side of the first (bottom) board. At the board-board boundaries, the connectors are used to pass the common mode voltage for power forwarding (charge flow through flying capacitors) and control signals along the daisy chain for signal forwarding. The height of the connector ensures there are enough spacing between the flying capacitors on the back side of the top board and the die epoxy on the front side of the bottom board. Since there are components on the front side of the first board (bypass capacitors for auxiliary boost), to prevent accidental electrical short to the flying capacitors on the back side of the second board, a small kapton tape spacer can be inserted for insulation; this is less of an issue for the remaining boards in the stack as they don't require the boost converter and have additional spacing between flying capacitors and the board underneath. With the stacked board configuration, voltage increases from bottom to top and the high-voltage output (V_{out}) is taken from the top of the stack.

IV. Experimental Results

A. Converter Characterization

Fig. 10 shows an oscilloscope screen shot of relevant transient waveforms for the platform running with four-boards stacked (i.e. the configuration shown in Fig. 9). Here, the system is driving a 1 nF load capacitor to 1.5 kV peak-peak, powered from a a 3.7 V input with the auxiliary boost running to provide $V_{\text{in,SC}} = 23V$. It is seen that the boost converter (V_{X} node waveform) mainly switches when the output of the SC stage is increasing (charging the load). This corresponds

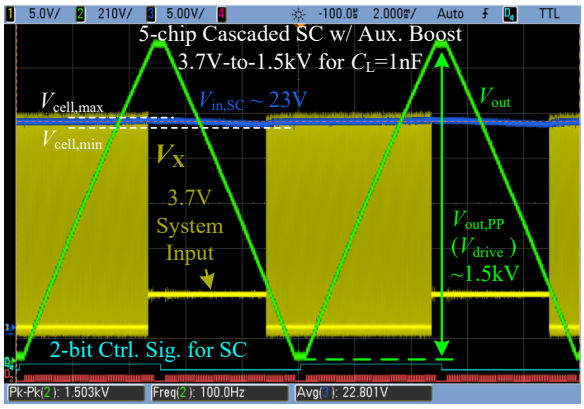

Fig. 10. The 4-board stack up achieving 3.7 V-to-1.5 kV voltage conversion.

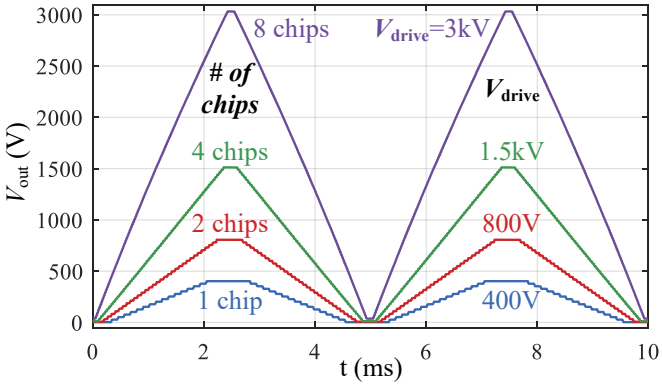

Fig. 11. Measured output waveform for different number of chip stacks.

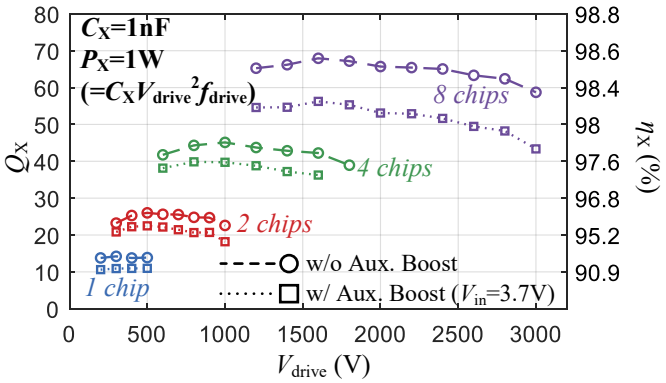

Fig. 12. Multiple chip stack, measured performance Q_{X} and η_{X}.

to when power is flowing out of the SC stage and so the boost stage is working to maintain $V_{\text{in,SC}}$ above the minimum limit shown in Fig. 5. When the SC stage is discharging the output, reactive energy stored in the load is recovered by flying capacitors so that the boost converter is idle.

By cascading multiple chips together, the maximum drive voltage V_{drive} is extended (Fig. 11), and Q_{X} and η_{X} are improved due to the higher number of switching cells (switching steps) according to (2). This is verified by Fig. 12 which shows performance metrics in (1) for different numbers of

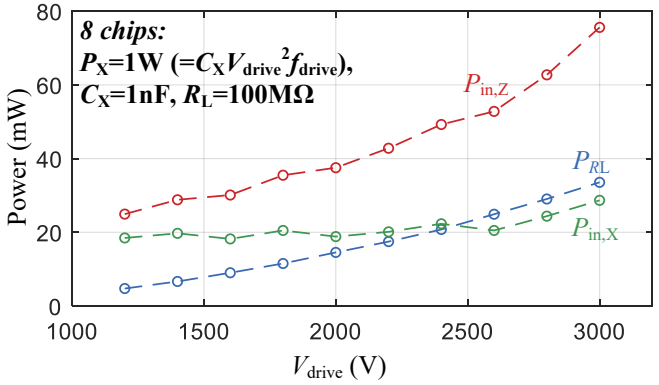

Fig. 13. The measured power processed by the converter at different driving voltage when delivering 1 W reactive power

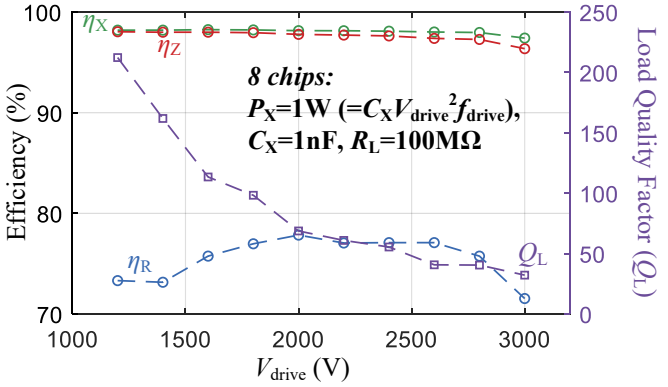

Fig. 14. The measured efficiency of the converter and the quality factor of the loading at different driving voltage

chips stacked. This figure includes measurements with the auxiliary boost (running from 3.7 V supply) and without the boost converter (running from a fixed 20-30 V benchtop power supply). In all cases the converters drive load capacitance $C_X = 1$ nF; drive frequency is scaled to provide reactive load power $P_X = 1$ W. Without the boost converter, the single-chip (not stacked) achieves $Q_X \sim 14$ ($\eta_X \sim 93\,\%$), while 8 chips-stacked can provide V_{drive} up to 3 kV with $Q_X \sim 59$ ($\eta_X \sim 98\,\%$). With the auxiliary boost running from 3.7 V, the reactive power efficiency only drops $< 1\,\%$, which maintains $\eta_X > 97\,\%$ for the 8-stack 3 kV converter.

B. Probe Loading Effect & Delivering Real Power

One consideration in the high-voltage driver system is the measurement effect of the oscilloscope as this can add significant real power due to resistive loading effects. The input impedance of the probe can be modeled as a resistor (R_P) and capacitor (C_P) in parallel. In this work, the high-voltage (20 kV) probe, P6015A, with input resistance (R_P) of 100 MΩ and input capacitance (C_P) of 3 pF is used to measure V_{out}. While probe capacitance is negligible, the resistive loading of the probe can be significant. Fig. 13 shows power drawn from the input supply V_{in} with an 8-chip stack providing 1 W reactive power to a 1 nF load versus peak-peak load voltage, V_{drive}. Here, $P_{in,Z}$ is total input power, P_{RL} is input power required to drive the probe resistance, and $P_{in,X}$ is power required to drive only the reactive load. It is seen that for high drive voltages, power required to drive the probe itself can dominate power required to drive the reactive load. Because real power can not be processed the same way as reactive power, even a small real power loading effect can have a significant effect on apparent converter performance.

While this is mainly a measurement artifact, it does motivate a treatment that considers delivering both real and reactive power. Such may be the case for certain actuators that have high leakage or resistive losses, or otherwise operate with low quality factor. This can be captured by modifying (1) to consider complex power efficiency:

$$\eta_Z = \frac{P_X + P_R}{P_X + P_R + P_{loss,R} + P_{loss,X}} = \frac{P_X + P_R}{P_X + P_{in,Z}}, \qquad (7)$$

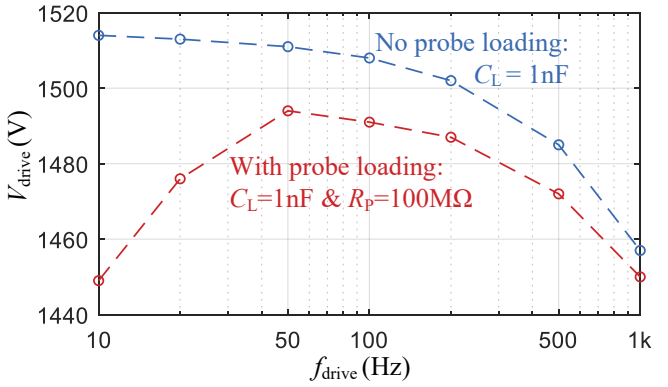

Fig. 15. The simulated driving voltage across the load with and without the probe loading for 4 chip stack-up

where P_X is the bidirectional reactive power flowing between the driver and the load, P_R is the delivered real power to the load, $P_{loss,R}$ is the power loss of the converter when delivering real power P_R, $P_{loss,X}$ is the power loss of the converter when processing the bidirectional reactive power P_X, and $P_{in,Z}$ is the total power drawn from the power supply when delivering both real power and bidirectional reactive power to the load. Expressions for the load quality factor, Q_L, real power efficiency, η_R, and reactive power efficiency, η_X may be expressed as:

$$Q_L = \frac{P_X}{P_R}, \quad \eta_R = \frac{P_R}{P_R + P_{loss,R}}, \quad \eta_X = \frac{P_X}{P_X + P_{loss,X}} \qquad (8)$$

The complex power efficiency, η_Z can be also derived as:

$$\eta_Z = \frac{Q_L + 1}{Q_L + 1 + (\frac{1}{\eta_X} - 1)Q_L + (\frac{1}{\eta_R} - 1)}, \qquad (9)$$

which shows that for a high Q load ($Q_L >> 1$, real power is negligible), $\eta_Z \approx \eta_X$; and for a low Q load ($Q_L << 1$, mainly delivering real power), $\eta_Z \approx \eta_R$. For the same operating condition as Fig. 13, delivering 1 W reactive power to 1 nF load, Fig. 14 shows the η_Z, η_X, η_R of the converter, and the Q_L of the loading condition (note that to maintain 1 W reactive power, drive frequency is scaled, thus Q_L changes with drive

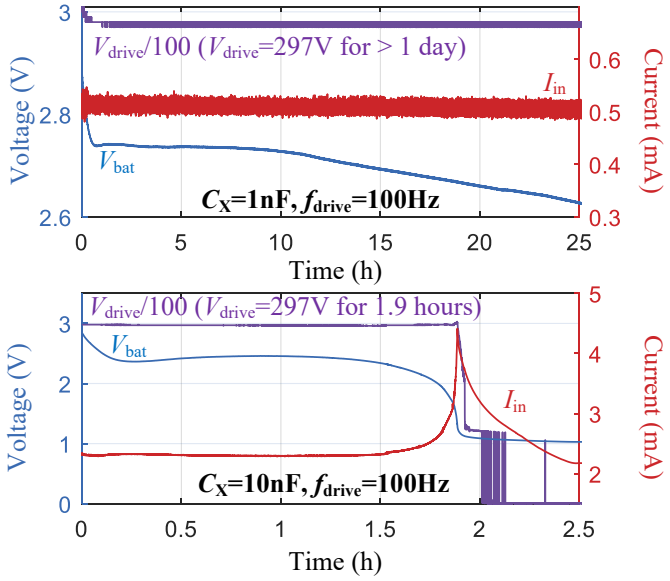

Fig. 16. Coin cell battery (CR-1025) operation and lifetime testing.

voltage). At lower V_{drive}, the power dissipated on the probe is low (Q_{L} is high as f_{drive} is high). The η_{Z} is very close to η_{X}. However, as Q_{L} goes down, η_{Z} starts to deviate from η_{X}. In addition, Fig. 14 shows that the real power efficiency of the 8-chip cascaded converter is $\sim$75 % when delivering 10's mW real power at kV drive voltages.

The analysis above assumes that the process of delivering real power and delivering reactive power is independent. However, these two process can affect each other, especially with the resistive loading from the probe (R_{P}), the V_{drive} could be lower as R_{P} discharges flying capacitors. Fig. 15 presents the simulation results of the V_{drive} of a 4-chip cascaded converter with or without the loading from the probe. It shows that at low frequency, the effect of R_{P} discharging flying capacitors (resulting in lower driver voltage) is more significant. However, as drive frequency (and reactive power) increase, the loading effect is (relatively) less significant.

C. Runtime testing with a CR-1025 coin-cell battery

Another test completed with the platform was runtime testing with a small coin-cell battery. Testing was completed with a lithium primary battery, CR-1025 (3 V, 30 mAh, 10 mm diameter, and 2.5 mm height), used as the input of the boost converter while driving 1 nF and 10 nF COG capacitors at 100 Hz f_{drive} and 300 V V_{drive}. Fig. 16 shows how the battery voltage (V_{bat}), input current of the converter (I_{in}), and the V_{drive} on the load capacitor changes over time.

For the 1 nF load, the converter was able to run over 24 hours (one day). The peak-peak drive voltage remains at $\sim$300 V throughout, with the boost converter providing regulation as the battery discharges. As this test requires constant measurement, the input power includes both reactive power to the 1 nF load and real power delivered to the oscilloscope probe. Notably, the long drive time illustrates

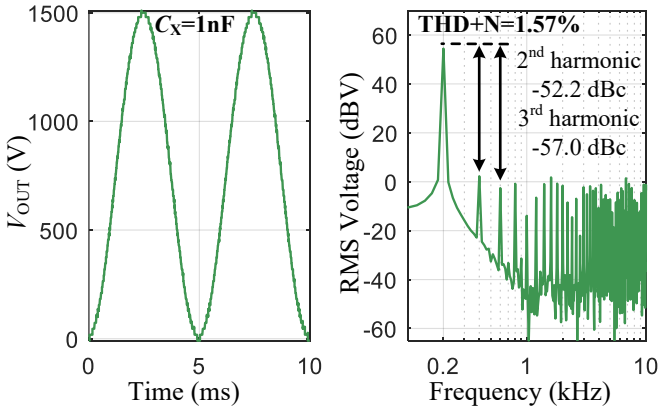

Fig. 17. Sinusoidal waveform synthesis and total harmonic distortion (THD).

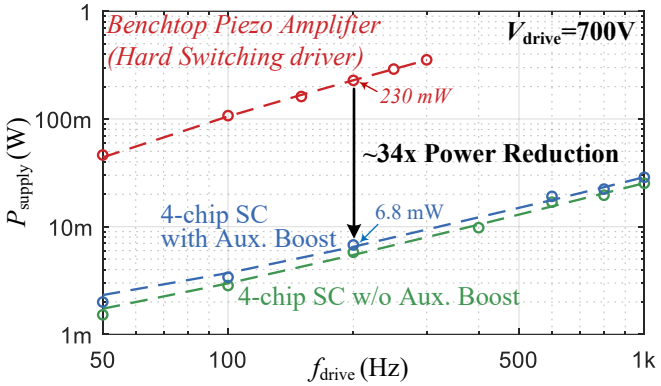

Fig. 18. Comparison to a benchtop piezo-amplifier: power consumption reduced over 34×.

the relatively low quiescent power of the integrated circuit. Each chip uses *less than 5 μA quiescent current* for the entire 16-stage SC converter (including level shifters, daisy-chain communication, FSM control, biasing, and padring I/O). While the boost converter does use additional power for gate driving, comparator and resistor divider, this does not add significantly to overall quiescent power.

When driving the heavier 10 nF load, the converter was able to run for over 1.5 hours until the battery was fully discharged. Again, the peak-peak drive voltage remained regulated throughout the test with the boost stage compensating for the lower battery voltage. This highlights the benefit of the pseudo-resonant driver: while a large quantity of reactive power is required ($\sim$90 mW for the 10 nF case), the real power drawn from the battery is much lower (6 mW), allowing longer run time and lower battery discharge.

D. Other testing: sinusoidal waveform synthesis and comparison to a benchtop piezo-amplifier

Other testing completed with the platform was arbitrary waveform synthesis and measurement of total harmonic distortion (THD), as well as a power consumption comparison to a benchtop piezo-amplifier. Waveform synthesis is relatively easy to do with the reconfigurable SC stage as it operates

like a thermometer coded digital-analog converter (DAC). In particular, there is interest in spectrally pure (sinusoidal) drive waveforms which can minimize audible harmonics and may be interesting for ultrasound and haptics applications.

To construct a sinusoidal waveform, a timing sequence for the step up and step down process was encoded on the FPGA controller. The timing sequence is simply a map of delayed CLK signals that correspond to the naturally sampled step-up/down intervals. Fig. 17 shows the 4-chip cascaded converter driving a 1 nF load with a sine wave at 1.5 kV V_{drive}. Spectral analysis shows good linearity with the second and third harmonics suppressed by over 50 dBc; It shows that with 60 discrete voltage levels, the converter can achieve total harmonic distortion and noise (*THD+N*) of 1.57 %, which is only slightly worse than a ideal 60-level DAC (*THD+N* = 1.36 %).

Fig. 18 shows the power consumption of the two-stage driver and a benchtop piezo-amplifier (Trek PZD700) while driving a piezoelectric actuator, Thor Labs PA40ND5 ($\sim$ 2 nF), at 700 V, the maximum output voltage of the piezo-amplifier. It shows that this converter consumes $\sim 34\times$ lower power compared to the piezo-amplifier which is a lossy linear amplifier. Two plots are shown to illustrate the difference in power consumption both with and without the auxiliary boost converter. Importantly, it is seen that while the boost converter does increase power consumption, the difference is negligible compared to the benefit of the overall solution compared to the (lossy) linear piezo amplifier.

V. Conclusion

This work presented an interposer-based miniaturized platform for a modular switched-capacitor converter with auxiliary boost to provide 3.7 V-to-3 kV voltage conversion with over 1 W reactive power. Compared to the same circuit in [1], this platform achieved $>100\times$ volume reduction and $>30\times$ weight reduction by using chip-on-board packaging for the IC and high density low-profile connectors. Energy efficient operation of the converter was demonstrated by operating with a 1 cm coin-cell battery: when driving a light load (1 nF), the converter was able to run over 24 hours. Various other testing was completed, showing capabilities for spectrally pure sinusoidal waveform synthesis and over $\sim 34\times$ lower power consumption than a bench-top piezo-amplifier.

References

[1] Y. Li, B. Mabetha, and J. T. Stauth, "A 3.7V-to-1kV chip-cascaded switched-capacitor converter with auxiliary boost achieving $>$ 96% reactive power efficiency for electrostatic drive applications," in *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, 2023, pp. 1–3.

[2] B. Donald, C. Levey, C. McGray, I. Paprotny, and D. Rus, "An untethered, electrostatic, globally controllable MEMS micro-robot," *Journal of Microelectromechanical Systems*, vol. 15, no. 1, pp. 1–15, 2006.

[3] D. K.-C. Liu, J. Friend, and L. Yeo, "A brief review of actuation at the micro-scale using electrostatics, electromagnetics and piezoelectric ultrasonics," *Acoustical Science and Technology*, vol. 31, no. 2, pp. 115–123, 2010.

[4] I. M. Koo, K. Jung, J. C. Koo, J.-D. Nam, Y. K. Lee, and H. R. Choi, "Development of soft-actuator-based wearable tactile display," *IEEE Transactions on Robotics*, vol. 24, no. 3, pp. 549–558, 2008.

[5] K. Jayaram, J. Shum, S. Castellanos, E. F. Helbling, and R. J. Wood, "Scaling down an insect-size microrobot, HAMR-VI into HAMR-Jr," in *2020 IEEE International Conference on Robotics and Automation (ICRA)*, 2020, pp. 10 305–10 311.

[6] M. Karpelson, Gu-Yeon Wei, and R. J. Wood, "A review of actuation and power electronics options for flapping-wing robotic insects," in *2008 IEEE International Conference on Robotics and Automation*, 2008, pp. 779–786.

[7] M. Karpelson, G.-Y. Wei, and R. J. Wood, "Driving high voltage piezoelectric actuators in microrobotic applications," *Sensors and Actuators A: Physical*, vol. 176, pp. 78–89, 2012.

[8] E. Steltz, M. Seeman, S. Avadhanula, and R. Fearing, "Power electronics design choice for piezoelectric microrobots," in *2006 IEEE/RSJ International Conference on Intelligent Robots and Systems*, 2006, pp. 1322–1328.

[9] Y. Li, B. L. Dobbins, and J. T. Stauth, "An optically powered, high-voltage, switched- capacitor drive circuit for microrobotics," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 3, pp. 866–875, 2021.

[10] Y. Li, B. Mabetha, and J. T. Stauth, "Sequential-drive switched-capacitor circuits for electrostatic loads: Modeling and comparison," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021, pp. 1–8.

[11] J. S. Rentmeister, M. H. Kiani, K. Pister, and J. T. Stauth, "A 120-330 V, sub-μA, 4-channel driver for microrobotic actuators with wireless-optical power delivery and over 99% current efficiency," in *2020 IEEE Symposium on VLSI Circuits*, 2020, pp. 1–2.

[12] C. Bellew, S. Hollar, and K. Pister, "An SOI process for fabrication of solar cells, transistors and electrostatic actuators," in *TRANSDUCERS '03. 12th International Conference on Solid-State Sensors, Actuators and Microsystems. Digest of Technical Papers (Cat. No.03TH8664)*, vol. 2, 2003, pp. 1075–1078 vol.2.

[13] M. Lok, E. F. Helbling, X. Zhang, R. Wood, D. Brooks, and G.-Y. Wei, "A low mass power electronics unit to drive piezoelectric actuators for flying microrobots," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3180–3191, 2018.

[14] J. James, V. Iyer, Y. Chukewad, S. Gollakota, and S. B. Fuller, "Liftoff of a 190 mg laser-powered aerial vehicle: The lightest wireless robot to fly," in *2018 IEEE International Conference on Robotics and Automation (ICRA)*, 2018, pp. 3587–3594.

[15] S. Park, A. Goldin, and J. Rivas-Davila, "Miniature high-voltage DC-DC power converters for space and micro-robotic applications," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2007–2014.

[16] T. Xie, M. R. Oltra, and H.-P. Le, "A 5kV/15W dual-transformer hybrid converter with extreme 2000x conversion ratios for soft mobile robots," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1548–1552.

[17] B. Mabetha, Y. Li, B. L. Dobbins, and J. T. Stauth, "Analysis and implementation of a cm-scale switched capacitor converter for low power, kilovolt-range applications," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 208–213.

[18] S. Chaput, D. Brooks, and G. Wei, "A 3-to-5V input 100V_{pp} output 57.7mW 0.42% THD+N highly integrated piezoelectric actuator driver," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 360–361.

[19] H. Cheng, Z. Zheng, P. Kumar, Y. Chen, and M. Chen, "Hybrid-SoRo: Hybrid switched capacitor power management architecture for multi-channel piezoelectric soft robot," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1338–1344.

[20] Y. Li, B. Dobbins, and J. T. Stauth, "A decentralized daisy-chain-controlled switched-capacitor driver for microrobotic actuators with 10× power-reduction factor and over 300V drive voltage," in *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, vol. 64, 2021, pp. 474–476.