A Modular Switched-Capacitor Chip-Stacking Drive Platform for kV-Level Electrostatic Actuators

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***Abstract*—This work presents a switched capacitor (SC) actuator driver implemented in 180 nm silicon-on-insulator (SOI) CMOS that uses multi-chip stacking to extend drive voltages beyond the process limits of a single chip. Building on past work, the SC stage uses a modified-series-parallel architecture to step the actuator drive voltage sequentially, reducing hard charging losses and recovering energy stored in the bulk dielectric of representative piezoelectric and other electrostatic transducers. The design uses an auxiliary (inductor-based) boost converter in the first chip to interface with low-voltage primary battery inputs while providing regulation. Multi-chip stacking allows modularity and scalability to kV-level drive voltages with low-voltage control signals relayed through a floating daisy-chain network. With a single chip using <5 μA quiescent current, the design provides voltage conversion ratios VCR>100, converting 3.7 V to over 400 V. In a demonstration with eight chips stacked in a miniaturized interposer platform, the design can convert 3.7 V to 3 kV (VCR>800), delivering up to 1 W reactive power with over 97% efficiency.**

***Index Terms*—DC-DC Converters, microelectromechanical systems (MEMS), switched capacitor, boost converter, robotics.**

I. Introduction

HIGH-voltage electrostatic actuator drivers are needed in a variety of mm- and cm-scale electromechanical applications from soft-robotics and haptics to optics, microfluidics and telecommunications [2]–[8]. While electrostatic actuators including piezoelectric transducers, silicon microelectromechanical systems (MEMs), dielectric elastomers, and electroactive polymers have advantages compared to conventional electromagnetic motors, they present unique challenges to the power electronics drive system [7]–[9].

Among the challenges and potential bottlenecks in electrostatic drive systems is *the need for high-voltage drive signals* which may range from hundreds of volts to several kV peak-peak depending on the actuator technology [8]–[12]. In many cases, these systems are powered from a low-voltage battery or system supply, motivating *extreme voltage conversion ratios* (VCRs). Finally, as illustrated in Fig. 1, a major difference compared to traditional motor-drive and DC-DC conversion applications is that electrostatic loads are typically dominated by the capacitive impedance of a bulk dielectric [8]–[10]. Thus, *drive electronics must supply significant reactive energy to the dielectric capacitance* C_X; in most cases reactive energy is much larger than real energy, either dissipated as loss or used for real mechanical work [10], [12].

This work is an extension of conference paper [1] "A 3.7V-to-1kV Chip-Cascaded Switched-Capacitor Converter with Auxiliary Boost Achieving > 96% Reactive Power Efficiency for Electrostatic Drive Applications," IEEE International Solid- State Circuits Conference (ISSCC) 2023. This work was funded in part by the Defense Advanced Research Projects Agency (DARPA) under award number HR001119C0040 and the National Science Foundation (NSF) award number 2216552.

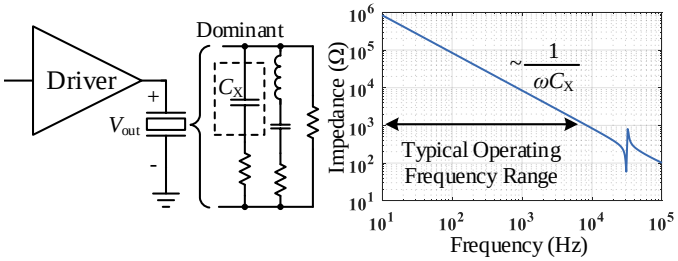
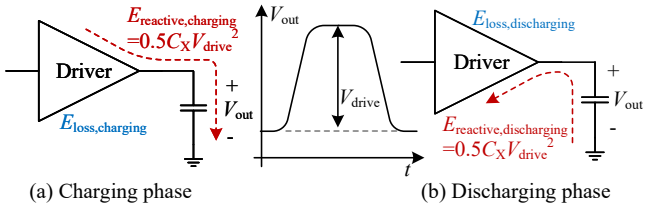


Fig. 1. General model of driving a electrostatic actuator with a representative actuator impedance model.



(a) Charging phase (b) Discharging phase

Fig. 2. Energy flow in a dominantly capacitive actuator.

Fig. 2 shows a conceptual system where the driver provides a peak-peak drive voltage V_{drive} to the actuator load; with dominant load impedance C_X, reactive energy of $E_X = \frac{1}{2}C_X V_{\text{drive}}^2$ is required to charge the bulk dielectric and provide sufficient electric-field to complete mechanical actuation. During the discharging phase, the driver needs to absorb this stored reactive energy. Thus electrostatic drive applications are significantly different than conventional power management circuits (i.e. DC-DC and DC-AC converters) that primarily delivery real power to the load [8], [10].

To quantify the effectiveness of delivering and recovering reactive energy, here we used metrics: effective quality factor Q_X and reactive power efficiency η_X, defined in [12] as

$$Q_X = \frac{P_X}{P_{\text{loss}}} = \frac{C_X V_{\text{drive}}^2 f_{\text{drive}}}{P_{\text{loss}}}, \tag{1}$$

$$\eta_X = \frac{P_X}{P_X + P_{\text{loss}}} = \frac{Q_X}{Q_X + 1}, \tag{2}$$

where P_X is the total reactive power across both charging and discharging phases, P_{loss} is the total real energy loss in the drive circuit across the charge-discharge cycle, C_X is the

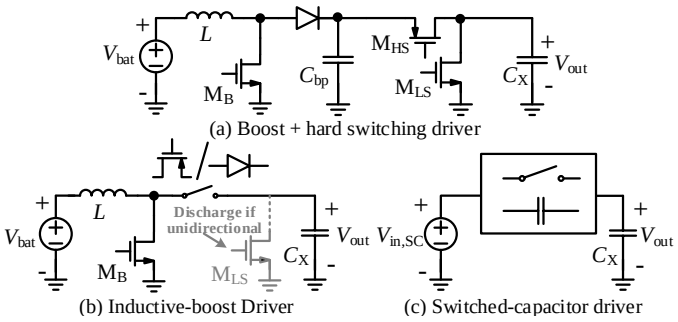


Fig. 3. Schematic representation of past work.

effective load capacitance, V_{drive} is the peak-to-peak output voltage and f_{drive} is the actuation frequency[1].

Fig. 3 shows simplified schematics of representative actuator drivers used in past work including hard-switching [13], [14] or linear amplifier [15]–[17] drivers, unidirectional [18]–[21] or bi-directional magnetic boost converters [22], [23], and reconfigurable switched capacitor approaches [24], [25]. Hard switching or linear amplifier approaches require a first stage boost converter to provide a fixed high-voltage supply. Lacking an efficient charge delivery (and recovery) mechanism, such topologies dissipate all reactive energy, resulting in an upper bound of $Q_{\text{X}} < 1$ and $\eta_{\text{X}} < 50\%$ (lower when factoring power loss in the additional HV boost converter). Unidirectional boost converters, including topologies which use diode-based SC voltage multipliers [18]–[20] can charge the reactive load efficiently, but can't recover energy during discharge, limiting $Q_{\text{X}} < 2$ and $\eta_{\text{X}} < 66\%$. Bidirectional boost converters can deliver and recover energy, but are challenging due to tradeoffs among inductor size, switching frequency and power loss [26], and require high-voltage-rated switching devices [27]. Such topologies are difficult to use with primary (non-rechargeable) batteries as recovered energy must be returned to the supply unless additional energy storage is used [24].

Pure switched capacitor (SC) drive circuits using the bidirectional, reconfigurable topology in Fig. 4 have been explored in past work [24], [25]. The switched-capacitor approach has multiple benefits compared to pure-inductive boost converters. Notably, it uses small, high energy-density capacitors to reduce overall passive component volume and weight [28], and can use all low-voltage switches that can be implemented in an integrated circuit (IC). Additional advantages relate to its ability to efficiently deliver and recover reactive energy by stepping the voltage across C_{X} in small increments. As discussed in [12], assuming N switching cells and flying capacitors, the converter sequentially steps the drive voltage in increments of $V_{\text{cell}} \approx V_{\text{in,SC}}$ (the flying capacitor and/or input voltage). The smaller step size reduces hard-charging loss by roughly the number of steps N when charging $V_{\text{out,pp}} = V_{\text{drive}} \approx N \cdot V_{\text{in,SC}}$. Thus, ideally $Q_{\text{X}} = N$ and $\eta_{\text{X}} = N/(N+1)$.

[1]In (1) and (2), P_{loss} only considers circuit losses in the driver, and discludes any real power delivered to the load. This is because real loss and power used for mechanical work in high-Q (e.g. piezoelectric) actuators is load-dependent, difficult to quantify, and typically much smaller than reactive power [8], [10]. However, a treatment which considers real power and its (typically small) impact on driver performance is provided in [12].

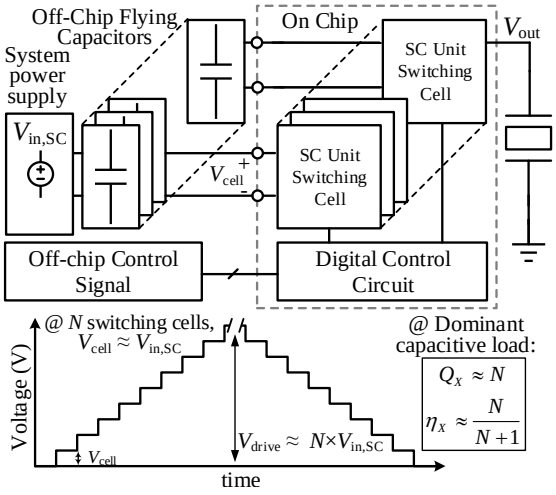


Fig. 4. Representation of past work SC drivers [24], [25].

Importantly, when stepping down (discharging) the actuator voltage, a large fraction $\sim (N-1)/N$ of energy flows back (is returned) to the flying capacitors. Because *reactive energy is provided efficiently and partially recovered,* this process is described as pseudo-resonant [12] or pseudo-adiabatic [24].

While the pseudo-resonant, sequential-switching SC circuit concept in Fig. 4 has previously been explored in [24], [25], these works had a number of limitations: 1) In past work, input voltage $V_{\text{in,SC}}$ used a fixed 6-24 V benchtop supply; thus the solution was not able to operate with variable low-voltage (e.g. 3-3.7 V Lithium) batteries. 2) Maximum drive voltage ($\sim$120-300 V) was limited by available device voltage ratings and SOI buried-oxide (BOX) voltage breakdown. 3) Past work used a large and slow 1.1 μm SOI CMOS process which had high quiescent power consumption, large die area, limited drive frequency and poor digital integration.

This work builds on previous reconfigurable SC actuator drivers [24], [25] in each of the areas listed above. The design is implemented in a high-voltage 180 nm SOI CMOS process which affords faster, high-density logic and analog integration to reduce die area by $>5\times$ and quiescent power by $>20\times$ compared to past work (with <5 μA quiescent current per chip). To provide drive voltages in excess of the $\sim$400 V BOX voltage rating, the design uses multiple-chip stacking, with control signals relayed through the switching cells and across chip-chip boundaries using fast, low-voltage level shifters and a daisy-chain network. This allows the design to be modular and scalable, as multiple chips can be stacked/cascaded to reach kV-level system drive voltages.

The design also uses an auxiliary (inductive) boost converter to provide a first (regulated) voltage-conversion step, allowing the converter to operate with low-voltage ($\sim$3-3.7 V) battery inputs. Discussed in the next section, the overall size and efficiency penalty of the auxiliary boost converter is small as it only process the real power (loss) of the SC stage, however it allows for voltage conversion ratio VCR > 100 for a single chip, over $6\times$ higher than previous work. With multiple chips cascaded, VCR is more than $50\times$ higher.

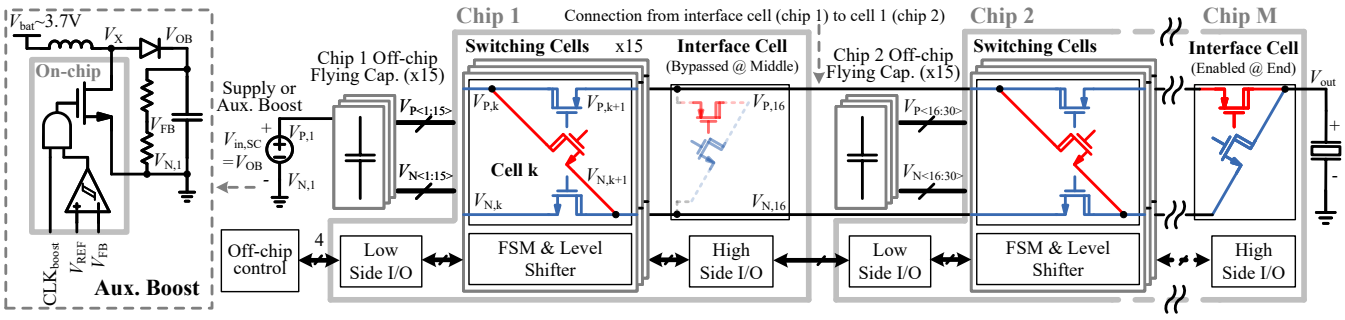


Fig. 5. High level architecture showing *'M'* chips stacked; the first chip is powered from the auxiliary boost converter.

II. Overview of the Chip-Cascaded Converter

Fig. 5 shows the schematic of the high-level circuit architecture. Each chip comprises $N = 15$ series-parallel switching cells and a final *'interface cell'* used to connect to the load. When chips are stacked, only the interface cell of the last chip (*i.e. Chip-M* in Fig. 5) is used; for intermediate (middle) chips, the interface cell is bypassed and the output of the 15^{th} cell is connected to the 1^{st} cell of the next chip. Thus, assuming a chip-stack with M chips cascaded, the total number of switching steps is $K = 16 + 15(M - 1)$.

Each series-parallel switching cell connects to one of 15 multi-layer ceramic (MLCC, off-chip) flying capacitors. As in [24], [25], the switching cells each operate independently to configure the adjacent flying capacitor either in series (red switch 'on') or parallel (blue switches 'on') with the next flying capacitor in the stack. Each switching cell is isolated in a deep-trench SOI tub and includes local level shifting for gate-driving and cross-domain signal relaying, finite state machine control, and local voltage reference and biasing. The system-level control signals pass through a distributed *'daisy-chain'* network to control the state of floating domains (SC cells) across cell-cell and chip-chip boundaries. Because logic levels are recovered at each step and only pass through fast low-voltage level shifters, daisy-chain signalling is robust and scalable to arbitrarily high voltage levels.

The auxiliary boost circuit (used only on the first chip) includes an on-chip 32 V LDMOS power device and a burst-mode hysteretic controller. With off-chip passive components, including bypass capacitor, inductor, a diode and a resistive divider, this converts the battery voltage (~3.7 V) to an intermediate voltage (6 to 30 V) to drive the input of the first cell in the SC stage. The burst-mode controller operates with fixed on-time (D $\approx$ 0.7) at 1 MHz switching frequency using external clock CLK_{boost}. If the boost output voltage ($V_{\text{OB}} = V_{\text{in,SC}}$) falls below a reference voltage, the boost switching signal is engaged to increase V_{OB}, otherwise the boost converter is idle, thus burst mode operation provides power to the SC stage 'only when needed.'

A. Distributed Daisy Chain Controller

A scalable, modularized distributed daisy chain controller is used to send control signals to floating SC cells and across chip boundaries. System-level control is based on two differential logic signals, passed to the first chip in the ground-referenced

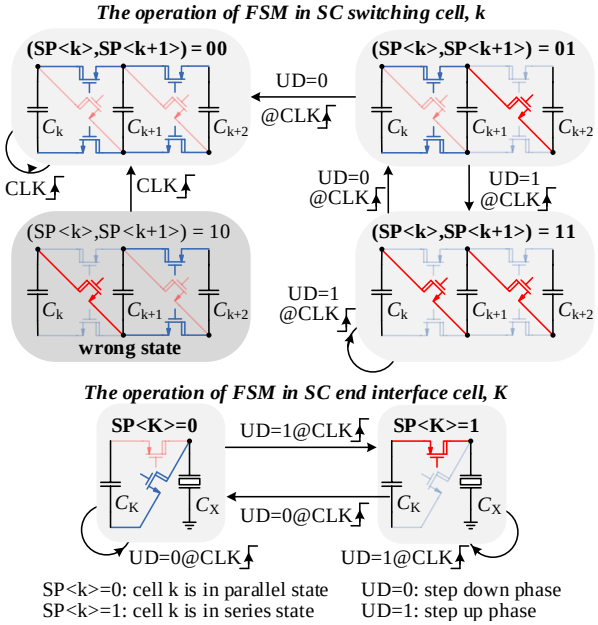


Fig. 6. The state transfer diagram of the finite state machine (FSM).

voltage domain. Signal UD (up/down) tells the converter whether to step-up (UD = 1) or step-down (UD = 0); CLK (clock) triggers the switching event at the rising edge. These signals are relayed up the stack, across the voltage domains of the different cells (and across chip boundaries) by fast, low-voltage level shifters and chip-chip I/O. A finite state machine (FSM) controller in each switching cell is used to determine which cell is the next to switch and which control signals (and cell-states) are relayed to adjacent cells.

Knowledge of the series-parallel (SP) state of the adjacent cell is required for the distributed FSM to control the switching sequence. Thus, for a given cell-k, signal SP$\langle k+1\rangle$ is passed down from the next cell (through a level shifter) and used in FSM logic. Fig. 6 shows the state transfer diagram for the k^{th} cell based on signals UD, SP$\langle k\rangle$, SP$\langle k+1\rangle$, and the rising CLK edge. Three viable cell states for the k^{th} cell include [SP$\langle k\rangle$, SP$\langle k+1\rangle$] = [0, 0], [0, 1] and [1, 1] where '0' and '1' indicate a cell is in the parallel and series state respectively.

At the rising CLK edge, with [SP$\langle k\rangle$, SP$\langle k+1\rangle$] = [0, 0], no switching action is taken; the FSM simply relays signals UD and CLK up the chain. With [SP$\langle k\rangle$, SP$\langle k+1\rangle$] = [0, 1],

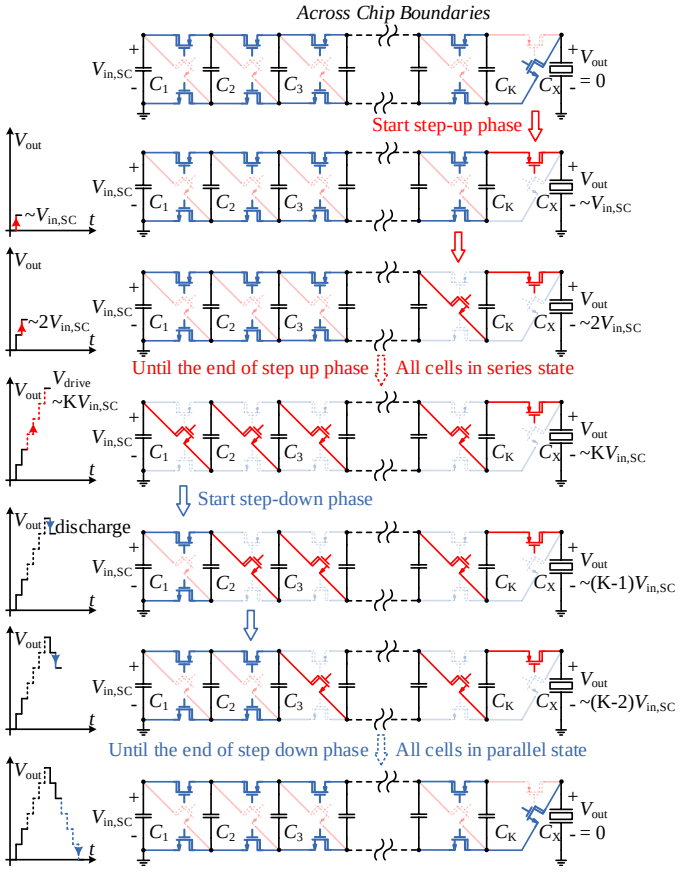


Fig. 7. Illustration of sequential switching process with K SC cells.

if UD = 1, cell-k switches to series; if UD = 0, cell-$(k+1)$ switches to parallel. For state [1,1], if UD = 0, cell-k switches to parallel. While invalid state [1,0] is unlikely to occur, if detected, it will switch back to the parallel state [0,0] at rising CLK edge. The same (reversion back to the parallel state) occurs if any of the flying capacitor voltages falls below a minimum threshold, which provides error correction (and a margin of safety and robustness) in the system.

B. SC Stage Operation

Fig. 7 top-bottom illustrates the full step-up and step-down sequential switching cycle. Starting with actuator voltage V_{out} = 0 (top), all parallel (blue) switches are on; flying capacitor voltages are equalized and charged to $V_{\text{in,SC}}$. With UD = 1, at the rising CLK edge, the interface cell (cell-K) switches to series, such that $V_{\text{out}} \approx V_{\text{in,SC}}$. At the next CLK edge, cell-(K-1) switches to series and $V_{\text{out}} \approx 2V_{\text{in,SC}}$. Holding UD = 1, this process repeats with the series-state rippling down the stack sequentially from last cell to first cell, such that eventually $V_{\text{out}} \approx KV_{\text{in,SC}}$. The step-down switching process starts when UD is set to 0. At the CLK edge, the lowest-voltage cell in the stack (i.e. cell-1) switches from series to parallel. At sequential CLK edges, the series-parallel transition ripples up the chain from the first cell to the last cell. Eventually all flying capacitors are in parallel, V_{out} = 0, and flying capacitors are recharged (as needed) from $V_{\text{in,SC}}$.

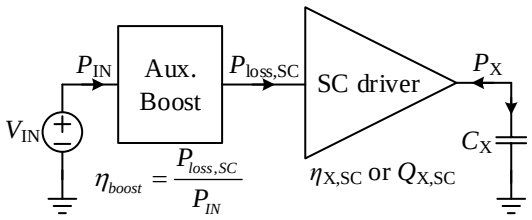


Fig. 8. Two-stage auxiliary boost + SC power flow model.

As discussed in [12], the sequential switching process reduces power loss compared to a full-swing hard-switching driver. In ideal slow-switching limit operation with K-steps, assuming flying capacitance much larger than C_{X} and neglecting other losses including quiescent power and bottom plate switching loss, ideal Q_{X} and η_{X} for the SC stage go as:

$$Q_{\text{X,SC}} = K, \;\; \eta_{\text{X,SC}} = \frac{K}{K+1}. \tag{3}$$

While (3) represents an upper bound on performance, various of the loss terms mentioned above can be small and/or mitigated by the design. For example, the design reduces parasitic bottom-plate (common mode) capacitance loss through the same sequential switching process used to deliver and recover energy in load capacitance C_{X}. Also, assuming low quiescent current to bias and operate switching cells (less than 5 μA/chip in the current design), quiescent power loss can be negligible. However, the value of flying capacitance relative to the load C_{X} is an important consideration and can affect performance, as detailed in [12]. In the current design, on-chip capacitance density is insufficient to drive nF-range piezoelectric actuators; however the design uses off-chip ceramic capacitors which have high density and low cost [26]. Consideration of losses in the two-stage converter (auxiliary boost + SC) are discussed in the next subsection.

C. Auxiliary Boost + SC Stage Loss Considerations

Fig. 8 shows a simplified perspective on the two stage boost + SC converter from Fig. 5 where the output of the boost converter is the input of the SC stage. As appreciated from Fig. 7, the boost stage provides power to 'recharge' flying capacitors as needed when they are in parallel with $V_{\text{OB}} = V_{\text{in,SC}}$. The power required to recharge these capacitors is the 'real power' (or loss $P_{\text{loss,SC}}$ of the SC stage). Assuming the boost stage has conversion efficiency η_{boost}, the total power P_{IN} drawn from system supply V_{IN} goes as

$$P_{\text{IN}} = \frac{P_{\text{loss,SC}}}{\eta_{\text{boost}}}. \tag{4}$$

Applying (4) in (1) - (3), the combined effective quality factor $Q_{\text{X,tot}}$ and reactive power efficiency $\eta_{\text{X,tot}}$ go as

$$Q_{\text{X,tot}} = Q_{\text{X,SC}} \cdot \eta_{\text{boost}} \approx K \cdot \eta_{\text{boost}}, \tag{5}$$

$$\eta_{\text{X,tot}} = \frac{\eta_{\text{X,SC}} \cdot \eta_{\text{boost}}}{1 - \eta_{\text{X,SC}} + \eta_{\text{X,SC}} \cdot \eta_{\text{boost}}} \approx \frac{K \cdot \eta_{\text{boost}}}{1 + K \cdot \eta_{\text{boost}}}, \tag{6}$$

where both of (5) and (6) quantify delivery of reactive power $P_{\text{X}} = C_{\text{X}} V_{drive}^2 f_{\text{drive}}$ with respect to real input power P_{IN} drawn from supply voltage V_{IN}.

Importantly, this shows that the boost converter efficiency (or power loss) penalty is reduced by the efficient and high conversion ratio SC stage. For example, the boost converter only supplies power to recharge flying capacitors based on SC-stage loss. However, assuming a large number of stages K, the real power $P_{\mathrm{loss,SC}}$ (required for recharge) is relatively small compared to the overall reactive power delivered (and recovered) by the SC stage. Because the boost converter does not process any of the (relatively larger magnitude) reactive power, its impact on reactive power efficiency is minor. For example, assuming boost efficiency is only η_{boost} = 80%, and $Q_{\mathrm{X,SC}}$ = 40 ($\eta_{\mathrm{X,SC}}$ = 97.6%); then $Q_{\mathrm{X,tot}}$ = 32 and $\eta_{\mathrm{X,tot}}$ = 97%, which is only a modest 0.6% decrease from the efficiency of the SC stage with an ideal input supply. Thus, the two stages work to complement each other: the SC stage provides the bulk of the voltage conversion ratio (VCR), supplying and recovering reactive power efficiently; the boost converter allows operation with lower (and potentially variable) system input voltages. Because the boost converter is low voltage and relatively low power, it can use a small inductor with minor impact on the overall performance.

III. Circuit Implementation

As described in Section II (Fig. 5), the circuit includes N = 15 identical SC switching cells and one interface cell, each with local level shifters, gate drivers, finite-state machine (FSM) logic, and a local linear regulator (LDO) for generating local voltage rails. Logic blocks and low-voltage analog circuits used 5 V-rated CMOS devices; the highest voltage-rated devices were 32 V LDMOS transistors used for the power train, level shifters, and LDO.

A. Switching Cell Architecture Details

Fig. 9 shows block-level schematic details of a representative switching cell. As the sources of the power switches are referenced to different nodes, gate drivers require local level shifters and voltage rails V_{REGN} and V_{REGP}, generated by a local LDO. Each of these voltage rails is ~4 V, referenced to the source of the respective power device. Low-side NMOS $\mathrm{M_{par,N,k}}$ is driven from $V_{\mathrm{REGN,k}}$ in the k^{th} cell; series switch $\mathrm{M_{ser,N,k}}$ is driven from $V_{\mathrm{REGN,k+1}}$ in the $(k{+}1)^{th}$ cell; PMOS device $\mathrm{M_{par,P,k}}$ is driven from $V_{\mathrm{REGP,k+1}}$ in the $(k{+}1)^{th}$ cell. Local FSM control of the k^{th} is also powered from $V_{\mathrm{REGN,k}}$.

Local level shifters are used to pass the control signals between the k^{th} to the $(k{+}1)^{th}$ voltage domains. The series-parallel switching state $\mathrm{SP}\langle k\rangle$ is level shifted to the $(k{+}1)^{th}$ domain to control $\mathrm{M_{ser,N,k}}$ and passed through anti-cross conduction (anti-X) and level shifted to control $\mathrm{M_{par,P,k}}$. Control signals CLK and UD are passed up the chain and adjacent series/parallel state $\mathrm{SP}\langle k+1\rangle$ is passed down. As level shifters only interface across adjacent voltage domains they can be fast, robust, and scalable.

Fig. 9 can also be used to appreciate details of converter startup. At initial startup (all flying capacitor voltages are 0 V) the first flying capacitor C_1 is charged directly by the boost converter. Once C_1 is charged sufficiently, the local $\mathrm{LDO_1}$ can operate to power up the local $\mathrm{FSM_1}$, which defaults to

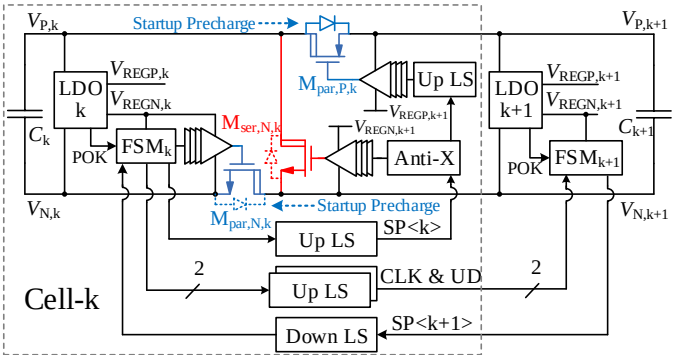


Fig. 9. Switching cell block-level schematic

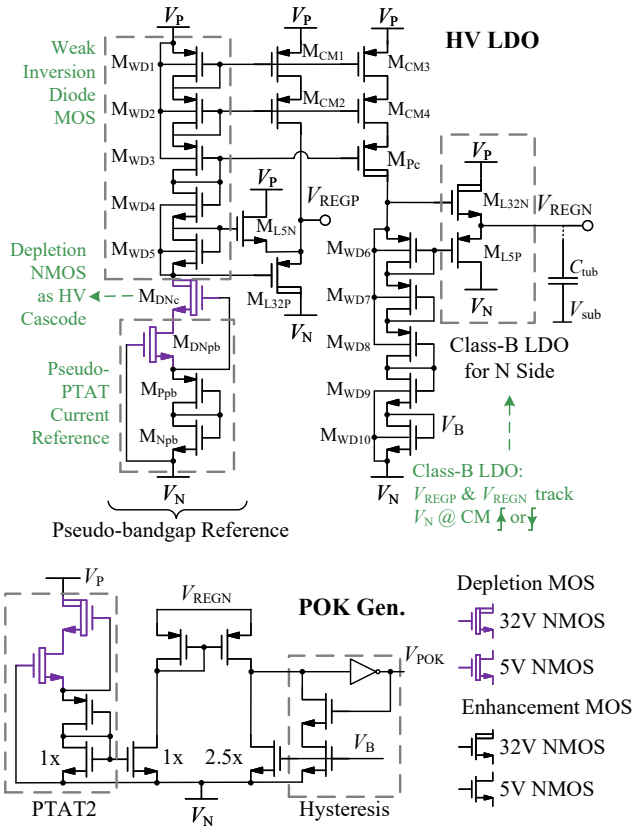


Fig. 10. Linear regulator and POK generation circuit

force all switches into the parallel state; this allows the low-side NMOS device $\mathrm{M_{par,N,1}}$ to turn on as it is powered in the domain of $\mathrm{LDO_1}$. Then, the body diode of $\mathrm{M_{par,P,1}}$ and 'on' switch $\mathrm{M_{par,N,1}}$ provide a path to charge the next flying capacitor C_2. Once $\mathrm{LDO_2}$ is on, $\mathrm{M_{par,P,1}}$ can turn on, fully charging C_2. Then this process can ripple down the stack to charge all flying capacitors.

B. Low-Quiescent-Power Linear Regulator

Fig. 10 shows the schematic of the linear regulator (LDO) used in each cell. An improved (lower power, more robust) version of the design in [25], the LDO uses a weak-inversion CMOS bandgap circuit to provide a supply- and temperature-independent voltage reference. A pseudo-PTAT (proportional

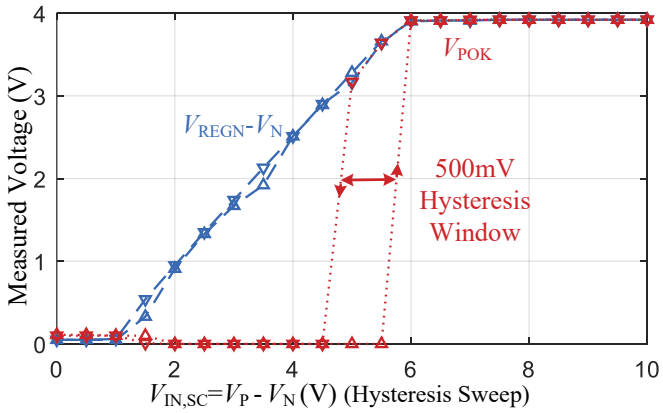


Fig. 11. Measured output of the LDO/POK circuit

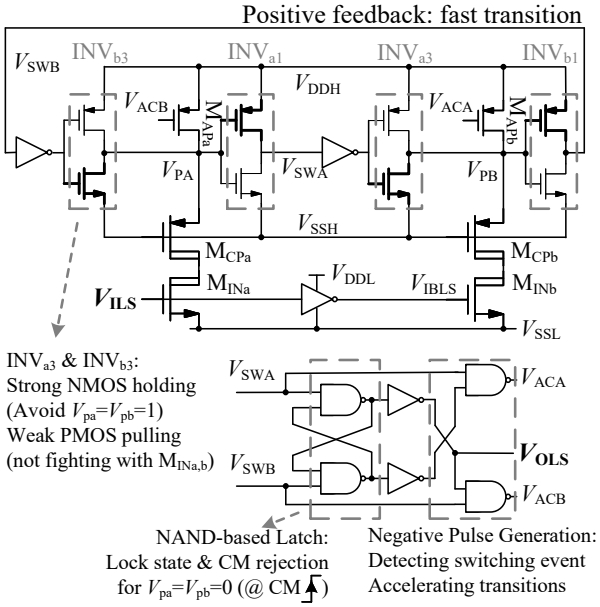


Fig. 12. The schematic of the up level shifter

to absolute temperature) current is created using depletion device M_{DNpb} with MOS degeneration devices M_{Ppb} and M_{Npb}, the difference in threshold voltages resulting in weak-inversion PTAT current generation, measured at ∼36 nA. When passed through a MOS diode stack, this creates a pseudo-bandgap reference, such as in [29]. High-voltage (32 V rated) depletion device M_{DNc} is used as a cascode for the low-voltage (better process tolerance) reference device M_{DNpb}.

High-side voltage rail V_{REGP} is provided by PMOS M_{L32P}, referenced to the high-side diode stack. This device sinks current as needed to maintain $V_{\mathrm{REGP}} \sim 4$ V below V_{P}. A small ∼ 36 nA bias current is provided from current mirror device $M_{\mathrm{CM1,2}}$ and clamping device M_{L5N} keeps V_{REGP} in a narrow range during idle modes and transients. Low-side supply V_{REGN} is created through mirroring the ∼ 36 nA PTAT current through a low-side diode MOS stack, providing a reference voltage for power device M_{L32N}. Clamping device M_{L5P} prevents overvoltage of V_{REGN} during transients.

A 'power OK' (POK) circuit is used to monitor the flying capacitor voltage level. The POK circuit confirms the LDO is in regulation and is used to reset the FSM during startup; if flying capacitor voltage becomes too low, POK triggers the switching cell to enter the 'parallel' state, allowing the flying capacitor to be (partially) recharged by adjacent capacitors. The POK circuit uses an identical PTAT current branch (PTAT2) without the diode-connected stack such that it turns on at lower cell voltage. The current is compared to the mirrored current in the V_{REGN} branch (node V_{B}), which is amplified 2.5×. When the main LDO starts regulating, this triggers V_{POK} to go high, adding hysteresis with an additional current sink. Fig. 11 shows measured results from the IC which show regulation is achieved for input voltage above ∼6 V with ∼500 mV hysteresis, after which $V_{\mathrm{REGN}} \approx 4$ V.

C. Latch-Based Local Level Shifter

Fig. 12 shows the schematic of the up level shifter, used to pass signals between the k^{th} and $(k{+}1)^{th}$ voltage domains. The level shifter uses LDMOS devices, $M_{\mathrm{INa,b}}$ and $M_{\mathrm{CPa,b}}$, to block the difference in cell voltages. The latch-based design uses no quiescent current and has additional features that improve common-mode transient rejection and switching speed [30].

For the 0-to-1 transition, V_{ILS} goes high: M_{INa} turns on to pull down V_{PA}. To improve transition speed, the PMOS in INV_{b3} is weak such that it will not fight with M_{INa}; the PMOS in INV_{a1} is strong such that it can easily flip polarity. With V_{SWA} increasing and M_{INb} off, V_{PB} is pulled up by the weak PMOS in INV_{a3}. Next, to accelerate switching, the NAND latch structure generates a one-shot pulse to briefly pull down V_{ACA}, turning on M_{APb} to charge parasitic capacitance and quickly pull up V_{PB}, turning off INV_{b1}. Then, positive feedback from INV_{b1} turns off INV_{b3}, quickly pulling down V_{PA}, completing the switching process. The idential but reverse process happens for the 1-to-0 transition.

The NAND-based latch is used to reject common-mode transients during step-up transitions. In this case, charge injected through the common-mode BOX capacitance can pull down both V_{PA} and V_{PB}; however, in this case the NAND latch holds state: the output V_{OLS} of the level shifter is logically unchanged, rejecting this (temporary) transient glitch. During step-down transitions, BOX charge injection can pull up V_{PA} and V_{PB}; INV_{a3} and INV_{b3} have strong pull-down to absorb this charge and prevent glitching in the level shifter.

D. Chip I/O Interface

An important contribution of this work is the provision of chip-chip stacking to provide modularity and extend the voltage range of the converter. At the chip-chip boundary, several important signals are needed to configure and relay control information along the stack. These signals include CLK and UD (relayed up the chain), SP (the series-parallel state of the next cell, relayed down the stack), and an indication of whether the chip is at the end (*i.e.* chip-M in Fig. 5) or in the middle of the stack, which configures use of the final 'interface cell.'

All I/O circuitry operates from the local LDO (V_{REGN}) of the respective switching cell, which can vary chip-chip due to process variation. To improve reliability of inter-chip

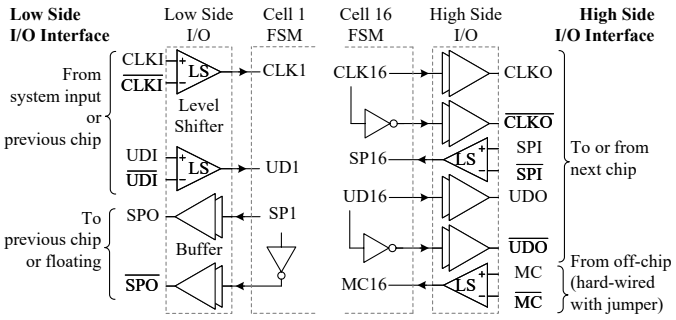


Fig. 13. Differential chip-chip I/O

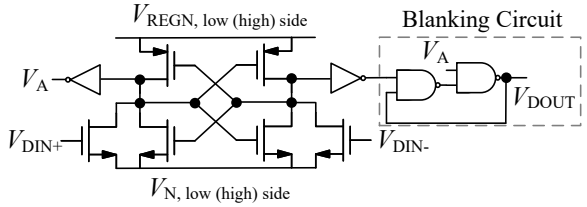


Fig. 14. The schematic of the input level shifter at chip I/O interface.

communication and mitigate process variation, differential I/O signalling was used. Shown in Fig. 13, low-side I/O (in cell-1) receives the differential CLK and UD from either the system controller (if the first chip in the stack) or the lower-voltage adjacent chip if otherwise. It also sends back the differential SP signal (series-parallel state of cell-1). High-side I/O (in the interface cell) sends out CLK and UD while receiving the SP signal from the next chip. If it is the last chip (chip-M), signal MC is set low (MC and $\overline{\text{MC}}$ are hardwired to V_{N} and V_{REGN} respectively of the last cell). For all other chips, MC and $\overline{\text{MC}}$ are respectively hardwired to V_{REGN} and V_{N}.

Fig. 14 shows the schematic of the differential I/O receive level shifter. While this is a conventional circuit based on a cross-coupled latch, it is shown here to emphasize that such circuit is needed to avoid differences in LDO voltage rails V_{REGN} of different chips. The I/O driver is simply an inverter buffer providing differential $V_{\text{DIN+/-}}$ logic level signals. However the latch converts these to full-rail logic levels. It also uses a NAND-latch blanking circuit to reject common-mode transient scenarios where both $V_{\text{DIN+}}$ and $V_{\text{DIN-}}$ are high.

IV. Experimental Results

A. Converter Implementation and Assembly

Fig. 15 shows the die photo of the converter, taped out in the 180 nm SOI CMOS process. Total die area is ∼1.7 mm^2; active area is ∼1.1 mm^2 as the die is pad limited. Each of the 15 SC switching cells and interface cell is ∼0.05 mm^2; auxiliary boost circuitry is ∼0.02 mm^2; padring I/O and ESD circuitry is ∼0.1 mm^2. The chip uses a 4-metal stackup with one thick (1 μm) top layer. Aside from 32 V LDMOS and depletion modules, no other process options were used; the chip uses 5 V MOS capacitors for local supplies, gate drivers, and padring I/O. Low-side I/O (and some test signals) are bonded out on the bottom of the die (as shown); High-side I/O and output are bonded out on the top.

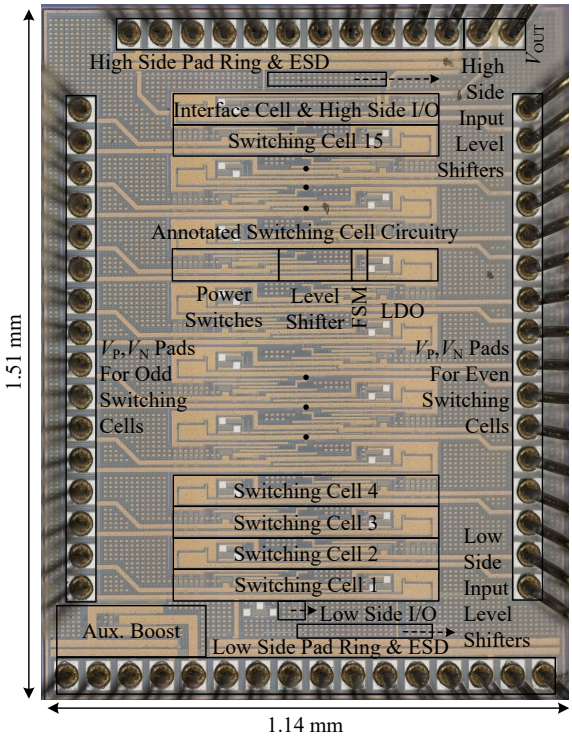


Fig. 15. The die photo of the converter.

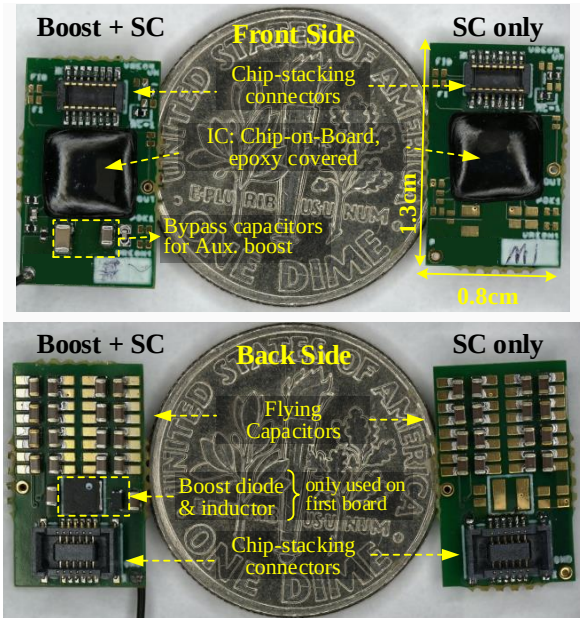


Fig. 16. Assembled printed-circuit board interposer platform.

Fig. 16 shows the assembled printed-circuit board platform for both the SC + auxilliary boost (first chip) and 'SC-only' (the rest of the chips in a multi-chip stack). The IC is wirebonded chip-on-board (COB) and encapsulated in epoxy. High-density (2 mm-tall, 0.4 mm-pitch) connectors (DF40B and DF40C) are used on the top and bottom such that boards can be stacked to achieve higher voltage. Total board area is 1.3 cm × 0.8 cm ≈ 1 cm^2. The connectors consume roughly 30% of board area and are a limitation on stack height.

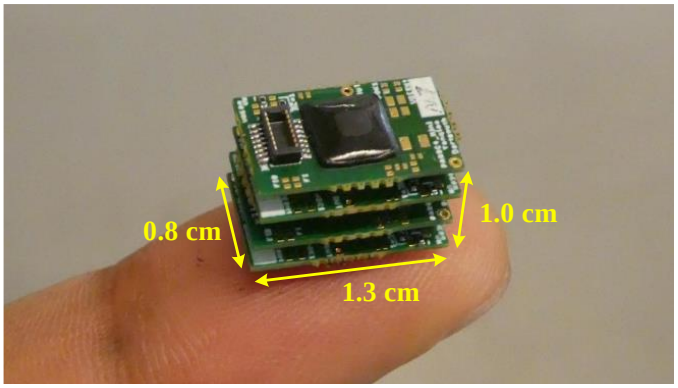


Fig. 17. Photo of example 4-board stackup (1.5 kV, ∼1 cm^3)

Fig. 17 shows an example 4-board stackup which has total bounding-box volume ∼1 cm^3 and weight ∼1.1 g. Table I provides a summary of all passive components and platform assembly components including weight. The dominant contributor is the PCB interposer, which is ∼50% of overall platform weight; the connectors contribute roughly 20%. While the design uses 16×0402 flying capacitors (one is a bypass capacitor for the first cell), these contribute only ∼18% of system weight; the IC and encapsulation contribute ∼10%. As the boost converter is only needed for the first board, its impact diminishes as the number of chips stacked increase.

TABLE I
SUMMARY OF THE PASSIVE AND ASSEMBLY COMPONENTS.

Component	Value	Weight
Flying capacitors	GRM155R61E225KE11D (0402, 207 nF - derated @ 25 V)	3.1 mg ×16
Inductor	XFL2010-104ML (100 μH, 6.1 Ω, I_{sat} = 92 mA)	∼20 mg
Diode	BAS40L-G3-08	∼1 mg
Aux. boost C_{IN}	06036D476MAT2A (0603, 27 μF)	9 mg
Resistor divider	10 MΩ (0201) + 1 MΩ (0201)	< 1 mg
Bare die	1.7 mm^2 180nm SOI CMOS	∼4 mg
Epoxy	IC encapsulation	∼25 mg
Connect. plug	DF40C	13.3 mg
Connect. recept.	DF40B	40 mg
Bare interposer	4-layer FR4, 0.5 mm-thick, 1 oz Cu	130 mg
Total SC only	One assembled board	270 mg
Total SC+Boost	One assembled board	310 mg

B. Single Chip Characterization

Fig. 18 shows the measured output of a single chip SC converter. Here, the SC stage is running without the boost converter (fixed $V_{\text{in,SC}} \approx 19$ V), driving a 1 nF load to 300 V_{pp} at 200 Hz. Differential control inputs CLK and UD are provided from an off-chip FPGA. Among important observations is that clear sequential switching steps are seen in V_{out}, matching the operation discussed in Section II and confirming slow-switching limit (SSL) operation. Also highlighted is the voltage on the last flying capacitor (other capacitor values are not shown for simplicity). It is seen that during step-up, the

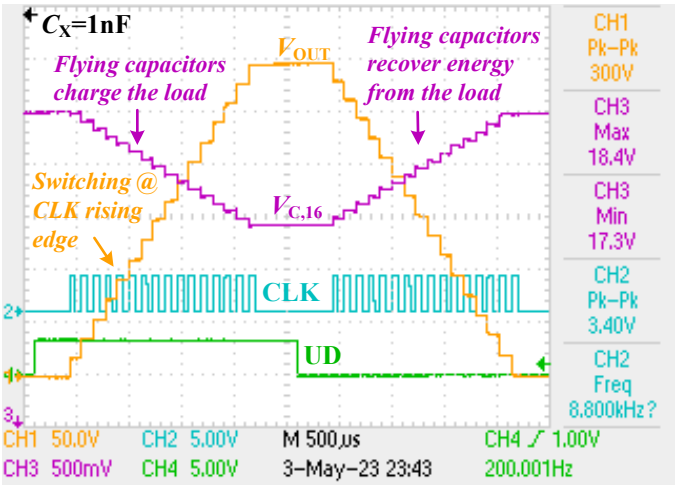


Fig. 18. Measured waveforms for a single-chip SC stage.

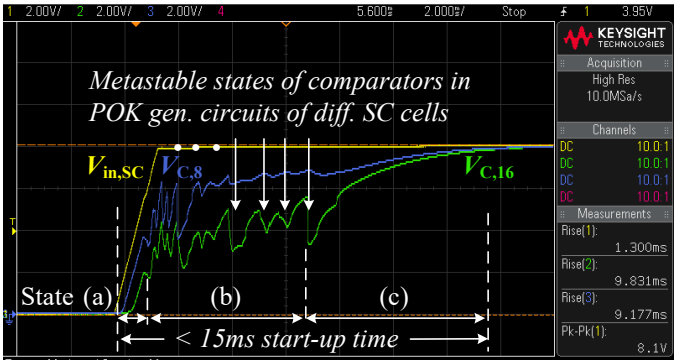


Fig. 19. Measured switched-capacitor converter startup details.

flying capacitor is discharged (delivering energy to the load); during step-down, the flying capacitor is recharged (showing it is recovering energy from the load).

Fig. 19 shows the startup process discussed in Section III (Fig. 9). Starting with $V_{\text{in,SC}} = 0\ V$, the input voltage is ramped up in ∼1 ms, charging the first flying capacitor and allowing the first cell to turn on. The low-side NMOS $M_{\text{par,N,1}}$ of the first cell turns on and the body diode of $M_{\text{par,P,1}}$ allows the next flying capacitor to charge. This process ripples through all the cells, charging each flying capacitor sequentially. It is seen that the last flying capacitor voltage $V_{\text{C,16}}$ reaches steady state in < 15 ms. Slight drops in the capacitor voltage during startup are due to the successive POK circuits turning on (slight shoot-through during the metastable state of the POK inverter and hysteresis generation).

Fig. 20 shows the peak-peak drive voltage V_{drive} versus $V_{\text{in,SC}}$ for different load capacitance from 0.1 nF to 15 nF. For load capacitance < 5 nF, the single chip was able to provide peak-peak drive voltage up to 550 V, well in excess of the rated buried oxide limit of 400 V. However, for higher load capacitance, $C_L =$ 15 nF, the LDMOS device voltage rating limited peak drive voltage to ∼350 V. Nonetheless, design can provide safe and reliable 400 V_{pp} driving in most circumstances, which exceeds the maximum 300 V_{pp} achieved in past work [25] with a similar architecture.

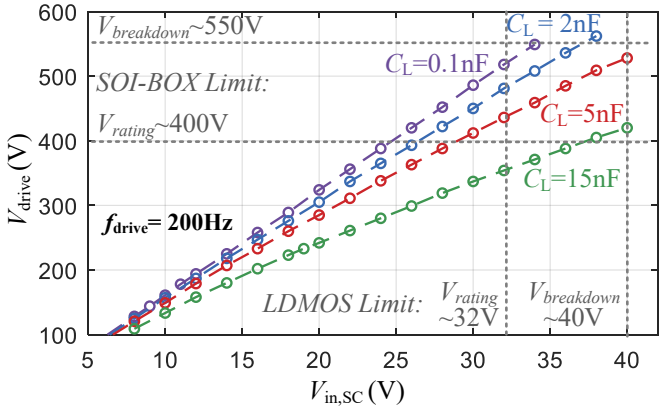


Fig. 20. Peak-peak drive voltage V_{drive} versus $V_{\text{in,SC}}$ for different load capacitance highlighting capabilities relative to device and BOX limits.

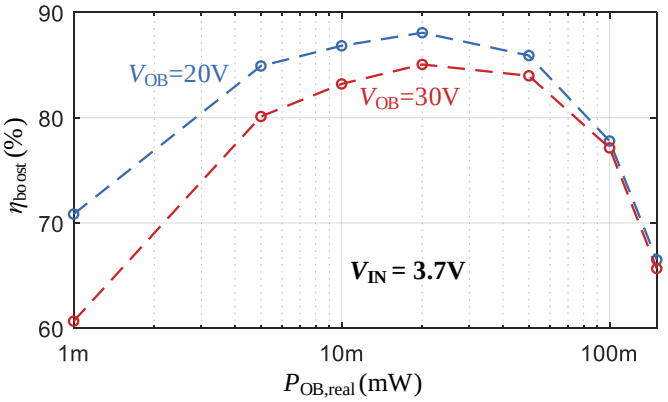


Fig. 22. Auxiliary boost converter efficiency versus (real) output power @ $V_{\text{IN}} = 3.7$ V, $V_{\text{OB}} = 20$ V and 30 V.

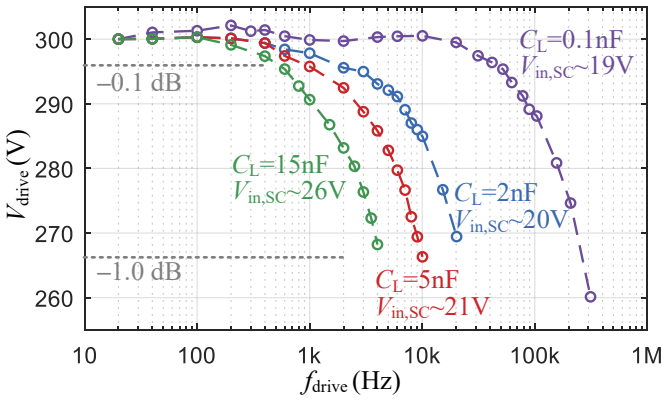


Fig. 21. Frequency response of a single chip SC for different load capacitance.

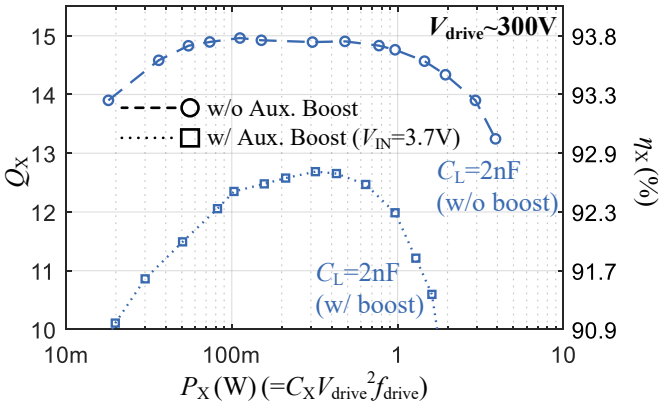


Fig. 23. The effective quality factor (Q_{X}) and reactive power efficiency (η_{X}) of a single chip for driving 2 nF load with V_{drive} = 300 V.

Another improvement compared to past work is operation at higher frequencies. Fig. 21 shows peak-peak drive voltage V_{drive} versus drive frequency f_{drive} for different load capacitance. At higher frequencies and higher load capacitance, V_{drive} decreases due to the design entering the fast-switching-limit (FSL), *i.e.* resistance (mainly in power switches) begins to impact charge transfer from flying capacitors to the load. However, even with this limitation, the design is able to provide >10 kHz drive frequencies for $C_L < 5$ nF with < 1 dB of attenuation (10× higher than [25]). For light load ($C_L = 0.1$ nF) the design can operate over 100 kHz, demonstrating the speed of level shifters and FSM logic.

Fig. 22 shows measured (real power) efficiency of the auxiliary boost (only) when converting from $V_{\text{IN}} = 3.7$ V to $V_{\text{OB}} = 20$ V and 30 V. Due to the relatively small (size) inductor, boost efficiency is modest, in the range of 80-85% for real power in the range of 5-80 mW. As mentioned in Section II, the impact of boost converter efficiency on the overall converter is moderated by the efficient (high-Q_{X}) SC stage. Discontinuous burst mode operation means the boost converter only turns on when the SC stage is stepping-up the load voltage, as this is the only time real power is flowing out, towards the load. When the SC stage is stepping down, flying capacitors recharge directly from energy stored in the load capacitance, thus the boost stage is idle.

The effect of the boost converter efficiency on the overall system performance can be appreciated from Fig. 23. Here, metrics effective quality factor Q_{X} and reactive power efficiency η_{X} are shown for the single-stage converter with and without the boost converter used to provide $V_{\text{in,SC}}$. In both cases, the driver is configured to provide 300 V_{pp} to a 2 nF (calibrated COG) load capacitor. The drive frequency f_{drive} is varied to sweep reactive power P_{X} delivered to the load. Without the boost converter, the SC stage achieves peak $Q_{\text{X}} \approx 15$, $\eta_{\text{X}} \approx 93.8\%$ and peak reactive power $P_{\text{X}} \approx 2.8$ W, representing 45% higher Q_{X} and ~7× higher power than [25].

With the boost converter providing $V_{\text{in,SC}} \approx 20$ V from a 3.7 V supply, the peak Q_{X} drops to 12.7. Using (3), this matches $\eta_{\text{boost}} \approx 85\%$. However, also in-line with (3) the efficiency of delivering reactive power only decreases ~ 1.1% to $\eta_{\text{X}} \approx 92.7\%$. This highlights again that since the SC stage provides the bulk of the voltage conversion and is able to recover a large fraction of reactive power, that the boost converter (which only processes the power loss in the SC stage) has a small impact on overall system efficiency.

Table II provides a power loss breakdown for a single chip with the boost converter. Total quiescent current of each chip is only 4 - 5 μA (or 250 - 300 nA per switching cell), which is dominated by PTAT reference generation in the LDO. For

TABLE II
POWER BREAKDOWN: SINGLE CHIP WITH BOOST, $C_L = 2$ nF, $V_{drive} = 300$ V_{pp}, $f_{drive} = 5.5$ kHz, REACTIVE POWER $P_X \approx 1$ W.

Loss	Power	Percentage
Sequential switching loss (charge sharing)	66.8 mW	80.1 %
Boost converter loss	15.5 mW	18.6 %
Quiescent power (4 - 5 μA/chip)	0.15 mW	0.18 %
BOX bottom plate loss	0.4 mW	0.5 %
Other (gate drive, I/O, leakage)	0.5 mW	0.6 %
Total	83.3 mW	–

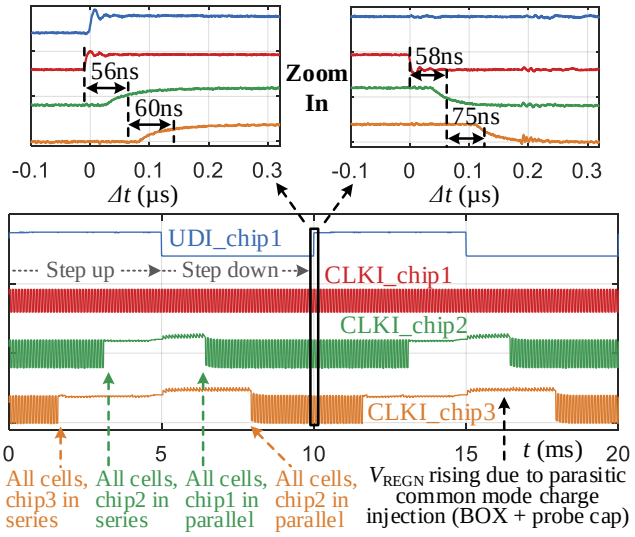


Fig. 24. Measured clock (CLK) signal, relayed across a 3-chip stack.

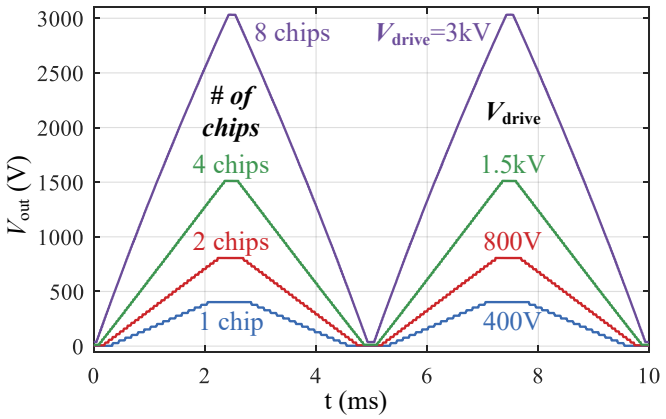


Fig. 25. Measured time-domain drive signal for different stack configurations.

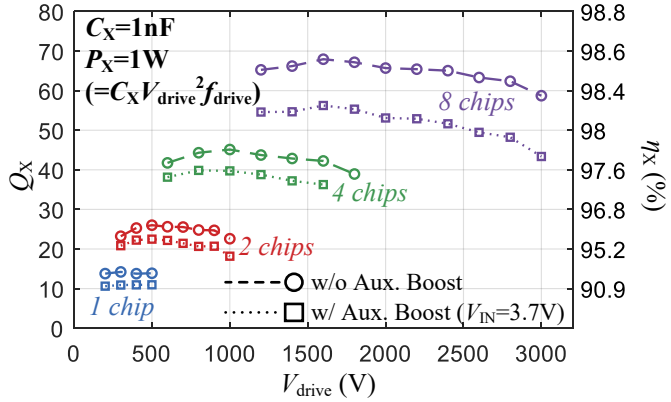


Fig. 26. Measured Q_X and η_X versus V_{drive} for the cascaded design driving 1 nF load and delivering 1 W reactive power.

the single chip driving a 2 nF load at 300 V_{pp} with 1 W reactive power (f_{drive} = 5.5 kHz), charge-sharing loss due to sequential switching remains the dominant loss factor. Charge sharing loss is slightly higher than predicted by the ideal expression (3) due to voltage derating of flying capacitors and their finite value relative to the load capacitance. A treatment which calculates loss based on these factors is found in [12].

The boost converter contributes ∼18.6% of total loss, corresponding to ∼81.4% efficiency of the boost stage. Bottom-plate switching loss of the buried-oxide (BOX) and other parasitic common-mode capacitances contributes ∼0.5%. Other losses include dynamic losses for gate driving, level shifting, I/O and leakage power, adding an additional ∼0.5 mW.

C. Characterization of Multi-chip Stacking

The multi-chip stackable PCB platform was used to test various configurations and capabilities to provide higher drive voltages. An important consideration for multi-chip stacking is the speed and effectiveness of the daisy-chain communication network as latency in signal-relaying can impact the overall clock and driving frequency. Fig. 24 shows details of the CLK signal propagating across three chips during a step-up/down switching cycle. Both the rising and falling propagation delays with the signal passing through a single chip (15 level shifters, finite state machines, and I/O drivers) is ∼ 60 ns, indicating roughly 4 ns propagation delay per switching cell highlighting the speed of level shifters and associated FSM logic. Note that the slow rise and fall times of the signals comes from the I/O driving the scope probe and is mainly a measurement effect.

Fig. 25 shows measured output drive voltages for different numbers of chips stacked using the platform. Maintaining safe operation below the per-chip ∼ 400 V BOX rating, the multi-chip design was able to multiply the overall output voltage well above the single-chip limit. In total up to eight chips were stacked in order to reach system voltages up to 3 kV while operating from a 3.7 V supply and providing a total system voltage conversion ratio VCR > 800.

Fig. 26 shows measured Q_X and η_X for the cascaded design. Here, a fixed 1 nF (calibrated C0G) load capacitor was used and total reactive power P_X was fixed at 1 W (by varying the drive frequency f_{drive}) while sweeping peak-peak output voltage V_{drive}. In-line with (3), Q_X and η_X generally increase with more chips as the number of steps K increases. Seen in Fig. 23, there is a modest (15-20%) decrease in Q_X for the case where the boost converter is used to drive $V_{in,SC}$, however the penalty is generally <1% in terms of η_X.

Similarly, Fig. 27 shows measured Q_X and η_X for different configurations while sweeping the total reactive power P_X. In line with Fig. 26, with more chips cascaded, the converter achieves higher Q_X. Peak output power generally increases with more chips stacked - the power of additional SC stages

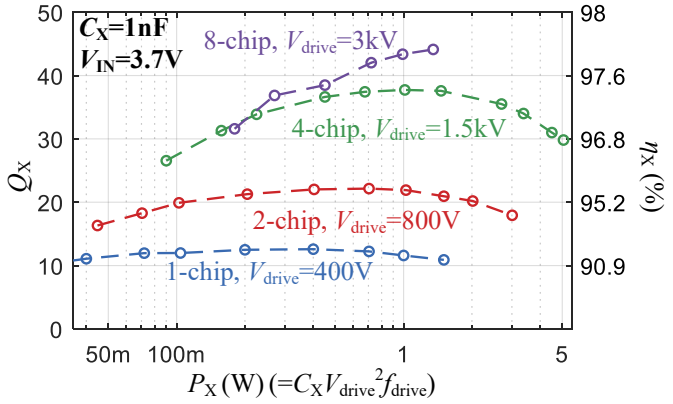


Fig. 27. Measured Q_X and η_X for different configurations while sweeping the total reactive power P_X.

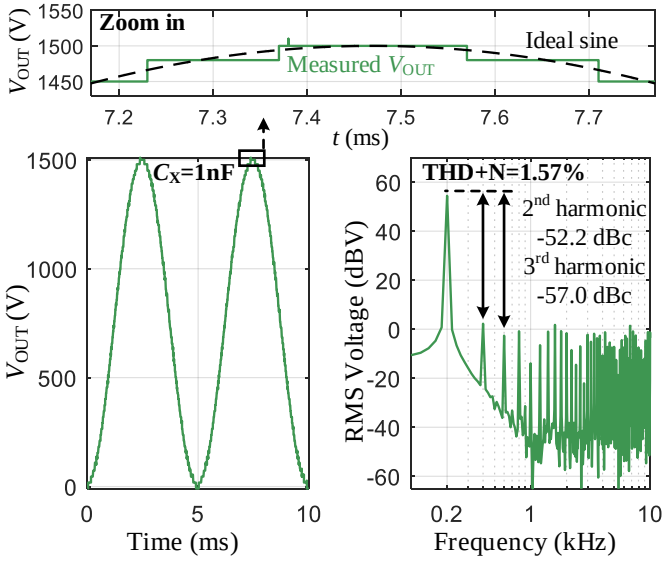


Fig. 28. Measured output and frequency spectrum for 4-chip stack with synthesized 1.5 kV, 200 Hz sine-wave output.

adding to the total. Also, with more stages and higher Q_X, the boost stage processes less real power for a given reactive power P_X, which can increase overall power density.

However, with high numbers of chips stacked (*i.e.* 8-chips, V_{drive} = 3 kV), peak output power falls off. This due to the flying capacitors in later stages being discharged more than capacitors in earlier stages, a known limitation of the sequential switching scheme used in this work. As discussed in [12], there are ways to circumvent this limitation by either: 1) allocating more of the total flying capacitance to later stages, or 2) using a binary switching scheme which divides the array in halves at each switching step. These options point to the possibility of further improving performance and power density of the concept in future work.

D. Other System Testing

Another consideration in some piezo-driver applications is the spectral purity of the drive waveform, required to minimize the sound emission from the actuator [22]. While trapezoidal waveforms are shown in previous data, it is relatively straightforward synthesize arbitrary and/or sinusoidal drive waveforms. Because the SC driver operates like a digital-analog converter (DAC), if the timing of the CLK signal is adjusted appropriately, these waveforms can be constructed by the system controller.

Fig. 28 shows measured data for a 4-chip stack driving a 1 nF load with a 1.5 kV_{PP} sine wave at 200 Hz using 60 discrete voltage levels. The distortion in the waveform is relatively low with the 2nd and 3rd harmonics over 50 dB below the fundamental. Distortion in the waveform mainly comes from capacitor voltages changing across the drive cycle (as they are charged and discharged) however, this can be compensated to some extent by adjusting the CLK signal. The total harmonic distortion plus noise (THD+N) was measured at 1.57% for the example.

Noting that the signal to noise ratio (SNR) of an ideal DAC goes as SNR = 6.02N + 1.76(dB), where N is the effective number of bits, for this example with for 60 discrete levels, N = 5.9 and SNR = 37.3 dB (THD+N = 1.36%). Thus the synthesized waveform in Fig. 28 is only slightly (1-2 dB) worse than an ideal 60-level DAC.

Another test demonstrating the performance of the driver was a comparison to a benchtop piezo amplifier (Trek PZD700) when driving a real high-voltage piezoelectric transducer (Thor Labs PA40ND5, $C_L \approx 2$ nF). Shown in Fig. 29, a 4-chip stack was used to provide a sinusoidal waveform at different frequencies with 700 V_{pp} (the maximum drive voltage of the PZD700). Fig. 30 shows power measured from the input supply P_{supply} versus drive frequency f_{drive} for the benchtop amplifier and 4-chip stackup with and without the boost converter. Power drawn from the PZD700 was measured with built-in voltage and current monitoring functions. As the benchtop PZD700 is a lossy linear amplifier, the power consumption from the SC drive platform was significantly lower. At 200 Hz drive frequency, the power drawn from the 3.7 V boost supply was 6.8 mW or 34× lower than the 230 mW drive power used by the PZD700. At higher frequency, this benefit improves as the impact of quiescent power has less effect. However, the PZD700 was only able to operate up to 300 Hz with the given actuator.

Another point to note is that when driving a real actuator, there is some real power (resistive and hysteretic power loss and power used for mechanical actuation [10]). Unfortunately, it is difficult to de-embed this from the loss in the SC driver stage. The additional real power delivered to the actuator is one reason why the 34× power reduction is less than Q_X for the 4-stack converter in Fig. 26. More details on this effect and its impact on the Q_X metric are provided in [12].

Related to this point is the difficulty in measuring high-voltage drive signals and the impact of these measurements on the data presented here. In this work, we use high-voltage oscilloscope probe P6015A (1000X, 100 MΩ, 3.0 pF) for all transient and peak-peak measurements. While the probe is carefully calibrated, its loading effect is significant. For example at 3 kV, the RMS power in the 100 MΩ scope

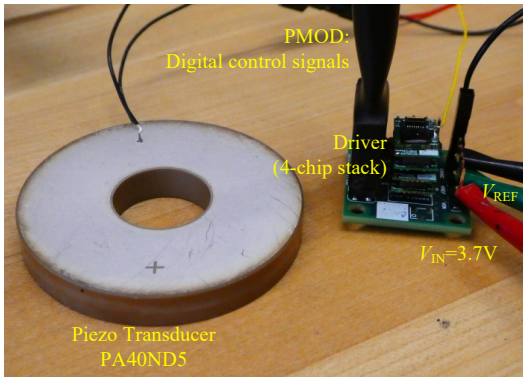


Fig. 29. Test setup for 4-chip stack driving piezo-transducer PA40ND5.

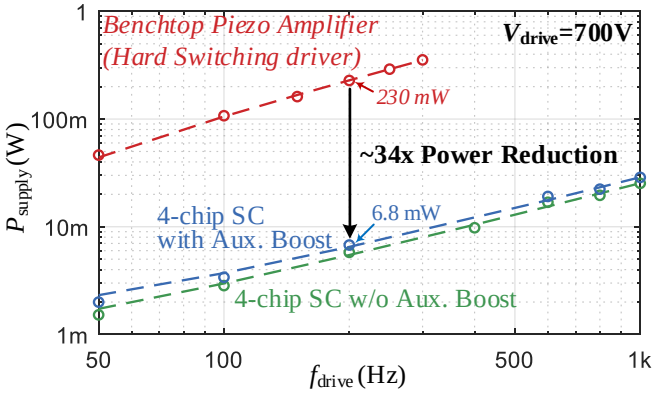


Fig. 30. Measured power vs drive frequency compared to benchtop piezo-amplifier PZD700.

resistance can exceed 30 mW. Noting also that this is real (not reactive) power that must be processed by the boost converter, it can have a significant effect on converter operation and efficiency measurements. The peak-peak measurements reported here are taken with the probe attached to the load; however power drawn from the input supply is taken with the probe removed. With the probe loading effects removed, the peak-peak drive voltage can increase - while the boost converter will maintain regulation, flying capacitors will discharge less, providing higher voltage. Therefore peak-peak drive voltages, reactive power, Q_X and η_X may in fact be slightly higher than reported. While this leads to a discrepancy (especially at high drive voltages), it also means that the reported performance is more likely understated rather than overstated in this paper.

E. Comparison to Past Work

Fig. 31 provides a comparison of past work, [13], [16]–[19], [22]–[25], [31], [32], and this work in terms of power density, peak drive voltage $V_{drive,max}$, reactive power efficiency η_X, and voltage conversion ratio (VCR). In Fig. 31(a), power-density is computed based peak power delivered over reported or estimated weight, which includes all passive and active components (capacitors, inductors, transformers, power switches, etc) and does not include the printed-circuit board or other assembly components (as these are difficult to compare equitably). This work achieves over 20 mW/mg, over 2× higher than [25], the next highest example.

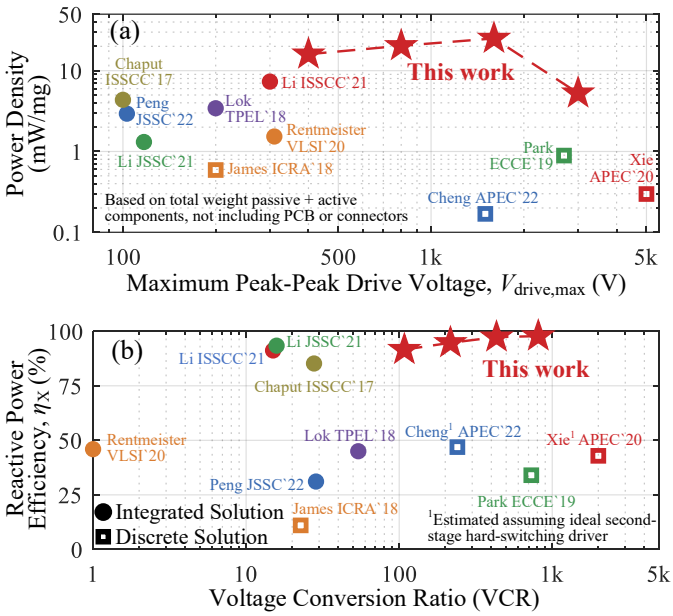


Fig. 31. A comparison between previous work and this work.

In Fig. 31(b), reactive power efficiency η_X is plotted versus voltage conversion ratio (VCR). For past work that reports power when driving a capacitive load, η_X is estimated from these numbers. For works that only report real power efficiency, η_X is estimated assuming an ideal second-stage hard switching driver. Peak efficiency of this work exceeds 98% for the 8-chip stack and is over 90% for a wide range of configurations and load power. Overall this work helps to extend the roadmap for electrostatic actuator drivers in each area of efficiency, power density, voltage conversion ratio, peak drive voltage, solution modularity and scalability.

V. Conclusion

This paper presented a switched-capacitor (SC) actuator driver which allows multi-chip stacking to provide drive voltages above the process (semiconductor device and buried-oxide) voltage limits of a 180nm SOI CMOS process. The switched-capacitor IC used an auxiliary boost converter (on the first chip in the stack) to provide a first voltage conversion step and interface with low-voltage primary battery inputs. A daisy-chain communication system was used to relay control signals up the chip stack and across chip-chip boundaries using fast, low voltage level shifters and distributed finite state machine (FSM) logic. Each chip used only ∼5 μA quiescent current for local biasing and supply generation and is able to drive peak-peak output voltages over 400 V from a 3.7 V supply (VCR $>$ 100). The design was characterized with multiple chips stacked, showing up to 3 kV_{pp} drive voltages (VCR $>$ 800) with effective quality factor $Q_X > 40$ and reactive power efficiency $\eta_X > 97\%$. The platform was characterized with sinusoidal drive signals, achieving THD+N $< 1.57\%$ and compared to a real piezoelectric transducer driver, demonstrating ∼34× lower power consumption. Compared to past work, this work achieves order-of-magnitude lower loss and higher power density for kV-level drive voltages.

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