Modeling and Analysis of Buck-Boost Converter for Soft Charging Capacitive Loads

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***Abstract*—This work explores the modeling and design of small-scale drive circuits for dominantly capacitive loads such as electrostatic actuators (i.e. silicon, piezoelectric, and dielectric elastomer transducers) but is also applicable to other more general capacitor charging applications. A buck-boost converter (which can be used as a first stage to soft charge a second-stage switched capacitor (SC) converter) is designed and optimized to maximize capacitive charging and discharging efficiency with given timing constraints. The model is used to optimize converter operation and component selection. Simulation of the hybrid converter (buck-boost converter and SC converter) are presented. Experimental results of a buck-boost converter prototype are presented to verify the proposed model.**

***Index Terms*—hybrid DC-DC Converter, soft charging, electrostatic, capacitors, batteries, microrobots**

I. Introduction

While the vast majority of power electronic loads are resistive and/or draw real power, there are certain applications and scenarios where loads present as dominantly capacitive. Examples include electrostatic actuators such as silicon-based, piezoelectric, and dielectric elastomer transducers, which are used in applications ranging from micro- and soft-robotics to haptics and ultrasound [1]–[7]. Other examples include capacitor charging applications, for example storing energy in supercapacitors [8], [9], pulsed power [10] and even common scenarios such as power semiconductor gate drivers [11], [12].

When the load presents as dominantly capacitive, reactive power is assumed to dominate any real power flow in the system. Thus metrics used for conventional power converters are not suitable to quantify performance of the power electronic drive system. In particular, for electrostatic actuator drivers, shown conceptually in Fig. 1, the bulk capacitance C_X and associated reactive power $C_X V_{pp}^2 f_{sw}$, where V_{pp} is peak-peak drive voltage, and f_{sw} is drive frequency, typically dominates real power and/or resistive losses in the component [7], [13].

To better quantify the performance of delivering (and recovering) reactive energy while factoring in losses in the drive circuit, past work [14], [15] has used metrics:

$$Q_X = \frac{P_{out,reactive}}{P_{loss}} = \frac{C_X V_{pp}^2 f_{sw}}{P_{loss}}, \text{ and} \tag{1}$$

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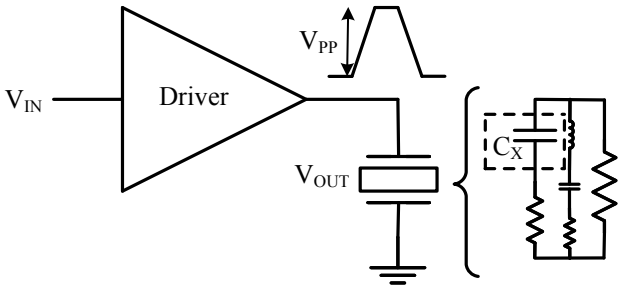

Fig. 1. Block diagram of an actuator driver showing the piezoelectric actuator dominant capacitance

$$\eta_X = \frac{P_{out,reactive}}{P_{total}} = \frac{C_X V_{pp}^2 f_{sw}}{C_X V_{pp}^2 f_{sw} + P_{loss}}, \tag{2}$$

where Q_X is the *effective quality factor*, which quantifies the ratio of reactive power over real power (loss) in the drive circuit; η_X is the *reactive power efficiency*, quantifying efficiency of delivering and recovering reactive power. From (1) and (2), the relationship between Q_X and η_X can be expressed as $\eta_X = \frac{Q_X}{Q_X+1}$. These metrics are integral in comparing different converters in their ability to deliver reactive energy.

Various previous approaches in the actuator drive space have included hard charging drivers where high voltage switches resistively charge and discharge the load, dissipating all stored energy such that $Q_X < 1$ [16]. Another approach is a pure magnetic converter such as a boost converter [6], [17], [18] or flyback converter [19] that soft charges the load and in case of a bidirectional converter, also can recover stored energy. These converters are limited by the losses in the inductor and high voltage rated switches. If we assume the current profile while delivering real and reactive power are similar (linearizing the current for reactive power delivery), the bidirectional boost converter (soft charging and discharging) has $Q_X \approx \frac{\eta_B}{1-\eta_B}$ where η_B is the magnetic boost converter real power efficiency.

Other recent works have explored pure switched capacitor (SC) converters which utilize the high energy density of capacitors and psuedo-soft charges the load [20]; the reactive power efficiency of these converters is ideally $Q_X = N$, where N is the number of SC converter stages. However,

these SC converters do not regulate the output voltage and therefore may need an additional regulating power conversion stage. To overcome the regulation challenges, cascaded hybrid converters have also been proposed [21]. These converters have a first stage boost converter to interface with a low-voltage battery input and boost to an intermediate voltage followed by an SC stage that does the main voltage conversion, the reactive quality factor here is limited to $Q_X = N \cdot \eta_B$ [21]. While addressing the regulation challenge of SC converters, hard charging losses (though reduced) still dominate the power losses of the converter.

This work explores hybrid architectures where the first stage magnetic buck-boost converter and SC stage operate in a way that reduces or eliminates internal hard-charging, while fully soft-charging the load and providing voltage regulation. Hybrid architectures have been explored for conventional DC-DC conversion applications (where real power is delivered to the load) [22]–[24]. In a soft-charging hybrid converter, the buck-boost converter requires a modest voltage conversion ratio which allows for more efficient components to be used (devices rated at the intermediate buck-boost voltage) making it smaller and more efficient, and the SC converter does the bulk of the voltage conversion; the reactive quality factor for the hybrid converter with an N stage SC converter is

$$Q_X = \frac{\eta_B}{1-\eta_B} N = Q_{X,BB} \cdot N. \tag{3}$$

The benefits of soft-charging the SC stage can be significant. Compared to [21], which uses boost + SC converter in a cascaded (not soft-charging) configuration, the effective quality factor Q_X can be increased by a factor $1/(1-\eta_B)$ if full soft-charging is achieved. For example, if the buck-boost stage has only a modest efficiency of $\eta_B = 80\%$, then Q_X can be increased by a factor of $5\times$ with the soft-charging approach. This motivates further exploration of how to achieve soft charging, including optimization and operation schemes for the first stage magnetic converter and different switching schemes for the SC-stage that allow soft-charging.

This paper is organized as follows: Section II explores the architecture and operation of the soft-charging buck-boost + SC converter. Section III covers the modeling and analysis of the buck-boost stage given a simplified (equivalent) model for the SC converter. Simulation and Experimental results are presented in Section IV and Section V concludes the paper.

II. Architecture and Operation

The proposed architecture uses a first-stage magnetic-based (here, presumed buck-boost) converter to soft-charge a reconfigurable, bidirectional switched-capacitor voltage multiplier. The SC stage is used to provide a large voltage conversion ratio (VCR) such that the buck-boost stage only needs to interface with low voltages, providing a modest VCR and may use low-voltage switches and a small magnetic component. Fig. 2 shows the conceptual idea of the converter. The magnetic stage is regulated to operate as an effective current source, eliminating charge-sharing losses between the SC converter

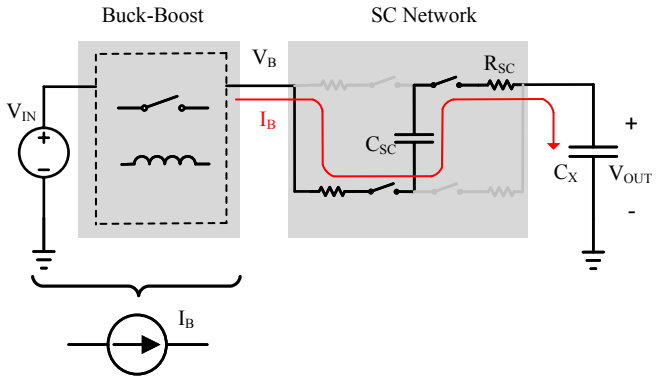

Fig. 2. Proposed Architecture: Buck-boost augmented hybrid SC

and the load. There are a number of considerations to achieve soft charging and efficient operation of the system. First, the load and SC charging current should flow through the magnetic stage inductor, then the SC stage sequence should have the highest capacitor utilization and minimize internal charge sharing loops and the selection of components should be optimized.

A. Topology Overview

The magnetic-based converter is here implemented as an inverting buck-boost converter, shown in Fig. 3. The buck-boost topology is attractive because of its ability to charge the load from below and above the input voltage. In particular, the inverting buck-boost converter is used because of its low number of switches, passive components, and relatively easy switching control compared to other buck-boost topologies such as non-inverting buck-boost, Cuk, cascaded buck and boost converters. Here, the battery voltage is presumed inverted (i.e. cathode to GND) such that V_B is positive.

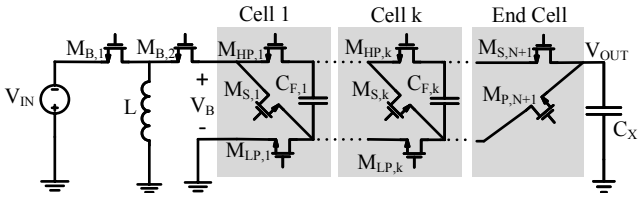

Fig. 3. Implemented architecture: inverted buck boost converter with a modified series parallel second stage

The second stage is implemented as a modified series parallel converter, similar to [14], [20]. The modified series parallel is selected because of its low voltage rated switches and flying capacitors; it also has the best passive component utilization of all non-isolated DC-DC converters, which allows for the minimum achievable volume and weight of flying capacitors for a given conversion ratio and delivered reactive power level [25]. This circuit is designed to incrementally multiply voltage V_B, connecting charge flow to C_X. Switches M_S connect adjacent flying capacitors in series; switches M_{HP} and M_{LP} connect adjacent flying capacitors in parallel. As

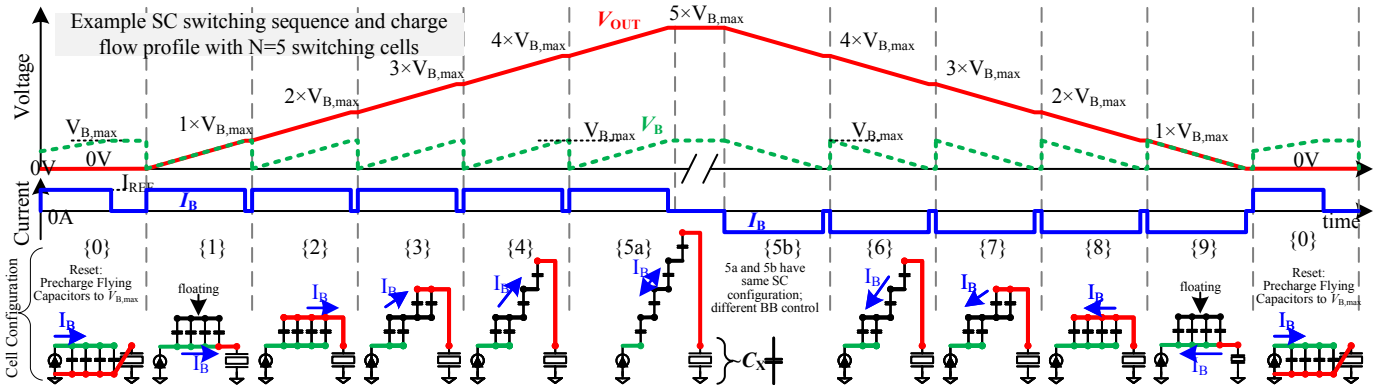

Fig. 4. Illustration of SC converter switching sequence; BB stage is abstracted as current source

highlighted in [14], the modified series parallel allows for various switching sequences including the binary sequence which eliminates internal charge sharing loops.

B. Operation

The merged buck-boost SC converter is operated such that all the charge flowing to the load capacitor flows through the current source-like impedance of the inductor. Shown in Fig. 4, during the charging phase, the buck boost charges the intermediate node, V_{B}, from 0 V to V_{Bmax}. Once charged to V_{Bmax}, a SC converter cell is switched from parallel to series to increase the output voltage by V_{Bmax}, the series connection causes the V_{B} node to go to 0 V, and the buck boost is then switched to charge the V_{B} node up to V_{Bmax}. This process is repeated until all the SC cells are in series and the output voltage is $(N+1)V_{\mathrm{Bmax}}$ for an N-cell SC converter. The discharge process is the reverse of the charging, where the V_{B} node is discharged to 0 V, then one of the SC converter cells is switched from series to parallel. This lowers the output voltage by V_{Bmax} and charges the V_{B} node to V_{Bmax}. This is repeated until V_{out} is discharge to 0 V.

The converter therefore comprises two separate operations: the buck-boost charging (or discharging) the V_{B} node after each SC transition and the SC converter reconfiguration to multiply the SC input voltage. The operation and modeling of the buck-boost converter is detailed in the next section. Here we discuss the SC binary switching sequence that has the highest capacitor utilization and eliminates internal charging loops during the SC transitions and therefore leads to an ideal soft switching process [14].

The binary operation implemented here is modified from that in [14]. Here, switching cell 1 is switched in series first to ensure that for all the SC phases, the only charge flow path is through the inductor. In this sequence, adjacent capacitor groups have identical charge flow before reconnecting in parallel, thus, there is ideally no impulsive charge flow at each transition. The buck-boost charges the SC and load after every SC transition bringing V_{B} from 0 V to V_{Bmax}. Fig. 4 shows the binary sequence operation with an example of 4-cell SC converter. The buck-boost stage is abstracted as a constant current source with value I_{B}. In phase 0, all the cells are in parallel and the flying capacitors are charged to V_{Bmax}, in phase 1 the first cell is switched in series and output is charged to V_{Bmax}. In phase 2, the output cell is connected in series, increases the output voltage to V_{Bmax}. Thereafter, cell 3 is switched in series, then cell 4 followed by cell 2. Binary switching therefore provides an ideal sequence for soft charging the SC converter and the load capacitor.

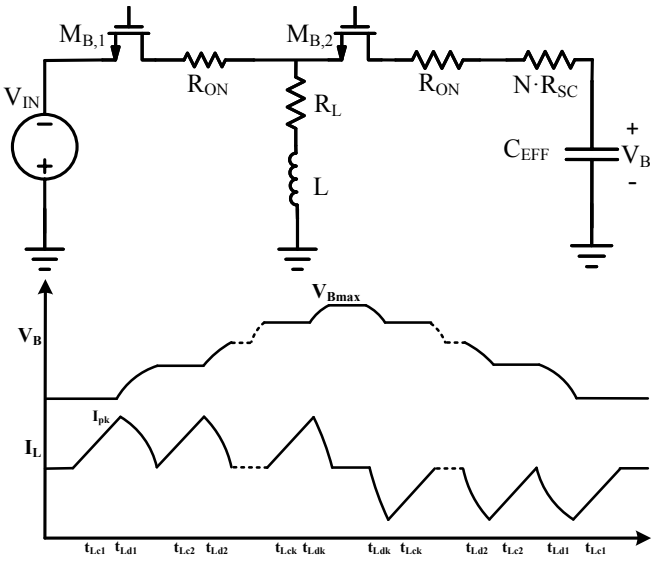

Fig. 5. Equivalent model of the merged hybrid converter and the ideal voltage and inductor current waveforms

III. Modeling the Converter

The Switched Capacitor converter can be modeled as an effective capacitance of the flying capacitor (C_{SC}) in series with the effective resistance of the switch resistance ($N \cdot R_{\mathrm{SC}}$) as shown in Fig. 2. The C_{SC} can be further lumped into C_X, simplifying the converter to a buck-boost converter charging and discharging a capacitor of $C_{\mathrm{EFF}} = \frac{C_{\mathrm{SC}} C_X}{C_{\mathrm{SC}} + C_X}$.

This equivalent converter captures the perspective of a buck-boost converter charging a fixed capacitor network and makes the following assumptions: a) the $C_{\rm SC}$ capacitor during SC phase transitions remains much larger than C_X such that $C_{\rm EFF} \approx C_X$; b) charging and discharging phases incur the same losses; c) the system is high Q, that is, the resistance in the circuit has minimal impact on the dynamics of the converter. Given assumption a), each SC transition becomes identical and therefore the converter operation can be represented as buck-boost charging the load capacitor C_X, to the intermediate voltage $V_{\rm Bmax}$ for N times as $V_{\rm out} = N \times V_{\rm Bmax}$.

Fig. 5 shows the simplified topology which will be modeled here. To charge the capacitor, the inductor is first charged to $I_{\rm pk}$, then the stored energy is transferred to C_X charging it to $V_{\rm Bmax}$. The losses incurred here are the conduction losses ($I_{\rm rms}^2 R$) and the buck-boost switching frequency, f_{swb}, dependent losses. The energy conduction loss is expressed as:

$$E_{cond} = I_{rms}^2 (R_{on} + R_L) T_{swb} + I_{rms,Ld}^2 N R_{SC} T_{swb,Ld} \quad (4)$$

where N is the number of SC cells, $T_{\rm swb}$ is the total buck-boost switching period and $T_{\rm swb,Ld}$ is the total time that the inductor is discharging into the load. $I_{\rm rms}$ is the inductor root-mean-squared current during the whole charging period while $I_{\rm rms,Ld}$ is the inductor rms current during the discharging period. $R_{\rm on}$ and $R_{\rm L}$ are the switch and inductor DC resistances assuming two switches in the buck-boost converter, $\rm M_{B,1}$ and $\rm M_{B,2}$, have the same on resistance. To minimize conduction losses, the load can be charged in multiple steps k, which reduces the $I_{\rm rms} \propto I_{\rm pk}$. For simplicity, this work uses constant peak current control: the inductor is charged to the same peak current at each step before being demagnetized to charge the load capacitor. Assuming k charging steps, the peak inductor current, $I_{\rm pk}$, is expressed as:

$$I_{pk} = \frac{V_{Bmax}}{\sqrt{k}} \sqrt{\frac{C_X}{L}}. \quad (5)$$

The time duration to charge the inductor to this peak current for each of the i^{th} steps is simply,

$$t_{Lc,i} = \frac{\sqrt{LC_X}}{\sqrt{k}} \frac{V_{Bmax}}{V_{IN}}, \quad (6)$$

and the time to discharge the inductor is,

$$t_{Ld,i} = \sqrt{LC_X} \cdot tan^{-1}\Big(\frac{1}{\sqrt{i-1}}\Big). \quad (7)$$

Interestingly, the inductor discharging time, $t_{\rm Ld,i}$ only depends on the step, i, and the natural frequency of the circuit and is independent of the total number of steps, k, and the output voltage. The total charging and discharging times and the overall period to charge the capacitor to $V_{\rm Bmax}$ can then calculated as the sum of (6) and (7) over the k steps.

$$\begin{aligned} T_{swb} &= \sqrt{LC_X} \cdot \Big(\sqrt{k}\frac{V_{Bmax}}{V_{IN}} + \sum_{i=1}^{k} tan^{-1}\Big(\frac{1}{\sqrt{i-1}}\Big)\Big) \\ &= \sqrt{k}\sqrt{LC_X}\Big(\frac{V_{Bmax}}{V_{IN}} + \gamma_k\Big), \end{aligned} \quad (8)$$

where $\tan^{-1}$ summation is abstracted as $\gamma_k\sqrt{k}$. This gamma coefficient can be interpreted as the waveform shape factor and lies between a triangle and a sine which have coefficients of 2 and $\frac{\pi}{2}$ respectively. The first term of (8) is the total charging time, and the second term is the total discharging time.

The inductor $I_{\rm rms}$ can be expressed in terms of $I_{\rm pk}$ as $I_{\rm rms} = \sqrt{\beta_k} I_{\rm pk}$, where β_k can also be interpreted as rms related waveform shape coefficient for a k steps inductor current waveform and since the inductor current waveform shape is bounded between a triangular wave and a sine, its β_k is between that of triangle and sine; $1/3 < \beta_k < 1/2$. R_L is expressed as $\frac{L}{\tau_L}$ to factor for the scaling of resistance with inductance at fixed volume [24], τ_L is the inductor time constant. Plugging these expressions into (4) and simplifying gives:

$$E_{cond} = \frac{\beta_k V_{Bmax}^2}{\sqrt{k}} \sqrt{\frac{C_X^3}{L}} \Big(\Big(\frac{V_{Bmax}}{V_{IN}} + \gamma_k \Big) \Big(\frac{L}{\tau_L} + R_{on} \Big) + \gamma_k N R_{SC} \Big). \quad (9)$$

Frequency-dependent, i.e. switching losses, in the boost converter can be represented simply as:

$$E_{sw} = kE_0, \quad (10)$$

where E_0 is the energy required to complete one switching cycle of the boost converter and may include gate drive and other switching losses. Equations (9) and (10) are expressed in terms of the design parameters of the inductor, switches and number of steps which guide their design or selection. The trade off of between conduction and switching losses as the the number of steps, k, varies can be seen in (9) and (10); as k increases, the conduction losses decrease due to lower inductor peak current, but the switching losses increase due to the increased number of switching cycles.

Equation (9) can also be used to illustrate the performance limit of the hybrid buck-boost + SC converter compared to a buck-boost stage alone. For example, assuming small $R_{\rm SC}$, it can then be seen that the conduction losses go with $V_{\rm Bmax}^3$. For a pure magnetic converter (without SC stage), $V_{\rm Bmax}$ is equal to $V_{\rm out}$ while is it $V_{\rm out}/N$ for a merged converter. Assuming $N \cdot R_{\rm SC}$ is negligible compared to R_L + $R_{\rm on}$, for the same output voltage, the merged buck-boost SC converter can achieve reactive quality factor $Q_X \approx N^3$ higher than that of the pure magnetic converter.

The optimal inductance inductance and number of steps can be found by differentiating the total energy loss, sum of (9) and (10) to get:

$$L_{opt} = \frac{R_{on}\tau_L(\frac{V_{Bmax}}{V_{IN}} + \gamma_k) + NR_{SC}\tau_L\gamma_k}{(\frac{V_{Bmax}}{V_{IN}} + \gamma_k)}, \quad (11)$$

$$k_{opt} = \left(\frac{\alpha}{2E_0}\right)^{\frac{2}{3}}, \quad where$$

$$\alpha = \beta_k V_{Bmax}^2 \sqrt{\frac{C_X^3}{L}} \Big(\Big(\frac{V_{Bmax}}{V_{IN}} + \gamma_k \Big) \Big(\frac{L}{\tau_L} + R_{on} \Big) + \gamma_k N R_{SC} \Big). \quad (12)$$

Equations (11) and (12) give design guidelines for selection optimal inductor and number of steps to operate a high Q system. For systems where R_{SC} is negligible compared to R_{on}, the optimal inductance is simply $L_{\mathrm{opt}} = \tau_L R_{\mathrm{on}}$ and therefore depends only on the buck boost switch resistance and the inductor time constant.

Plugging (9) and (10) into (2) gives the reactive power efficiency of the buck boost converter:

$$\eta_{X,BB} = \frac{C_X V^2 f_{sw}}{C_X V^2 f_{sw} + 2(E_{cond} + E_{sw})}. \tag{13}$$

It should be noted that the model and optimization presented here do not include frequency dependent inductor losses such as proximity, skin effects and core loss. A potential approach to account for these losses is discussed in Section IV.

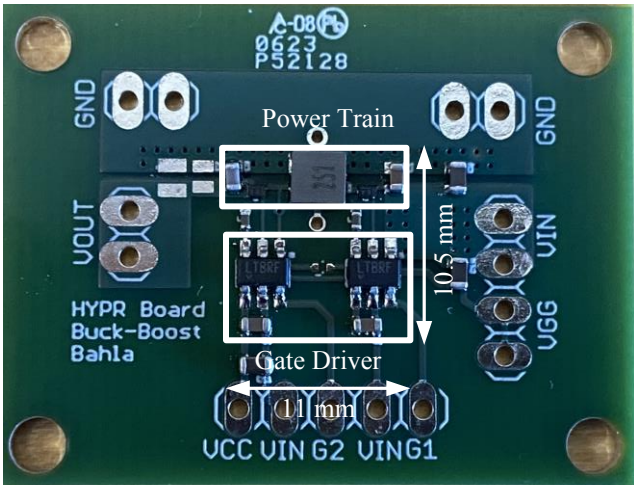

Fig. 6. Implemented PCB of buck boost converter

IV. Experimental and Simulation Results

The equivalent model of the buck boost converter was implemented on a PCB to verify the developed theory on the multi-step operation to charge a capacitive load. Fig. 6 shows the implemented inverted buck boost converter. The input voltage, V_{IN}, was -3 V, driving the output voltage to 10 V while driving a 100 nF capacitor. The results of the experimental and simulation data are presented here.

TABLE I
Component List For Buck Boost

Components	*Part Number*	*Description*
Switches	NX138AKMYL	60 V, 4.5 Ω, 60 pF, 0.64 mm^3
Inductor	LQH3NPN251MGR B1047AS-471M	251 μH, 110 mA, 9.6 Ω, 8.1 mm^3 470 μH, 430 mA, 1.7 Ω, 266mm^3
Capacitor	GRM3195C1H104G-A05D	100 nF, 50 V, 1206, 5 mm^3

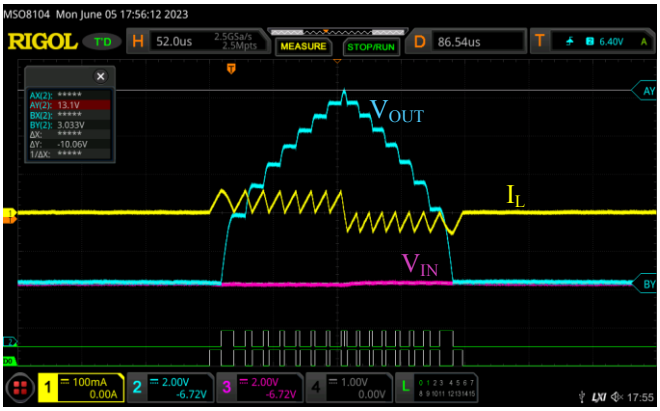

Fig. 7. Output voltage (blue) and inductor current (yellow) of buck boost driving a 100 nF load at 10 Vpp in 8 steps,

A. Experimental results: charging a capacitive load

Fig. 7 shows the oscilloscope screenshot of the buck boost converter output voltage waveform and inductor current when charging a 100 nF load capacitor. The oscilloscope is ground referenced to V_{IN} for the inverted buck boost, which offsets the voltage traces by V_{IN}. The peak current in this case has been reduced by ideally $\sqrt{k} = \sqrt{8}$ compared to a one step charging up operation. This leads to lower conduction losses and in regimes where such losses are dominant, the Q_X increases by $\sqrt{8} = 2.8$.

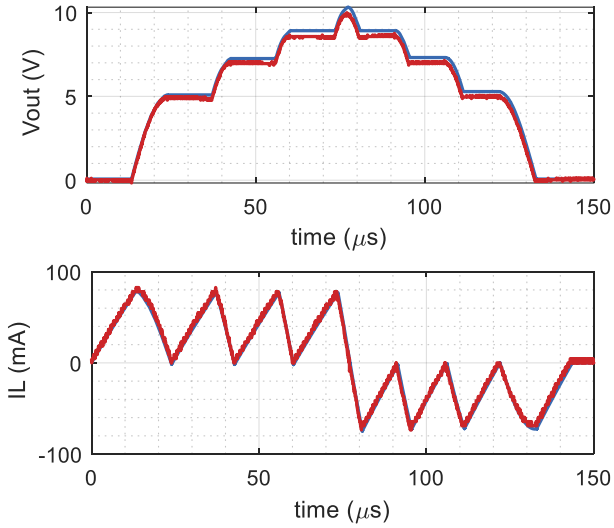

Fig. 8. Output voltage and inductor current waveform comparison between simulation (blue) and experiment (red) data

Fig. 8 shows the reploted comparison between the experimental waveform and simulated waveforms for output voltage and inductor current for a 4 steps operation of the buck boost charging the inductor current. There is a close match between the waveforms. The differences account dominantly due to core loss and secondary effects such as board parasitics. It should be noted that including these losses to include the

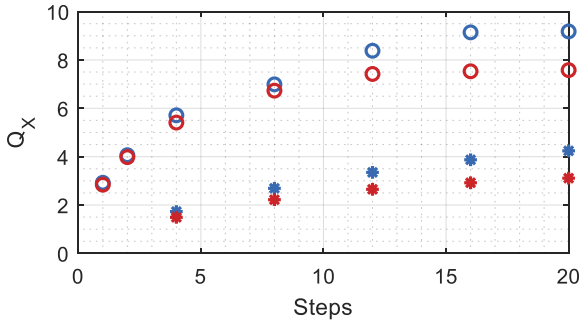

Fig. 9. Reactive quality factor: simulation (blue) and experiment (red) data. Circle - B1047AS-471M, Asterik - LQH3NPN251MGR

core loss other frequency dependant parameters would give a more accurate energy loss and therefore more accurate optimal inductance and number of steps expressions.

The experimental data presented here show that the operation and model developed give a proxy for operating buck-boost converter for charging and discharging capacitive loads.

The reactive power efficiency of the buck boost increases with the increase in number of steps, fig. 9. Low profile inductors were used to verify the developed theory. For the LQH3NPN251MGR inductor data, the minimum steps used was 4 steps because of its lower saturation current. The overall trend shows that as the number of steps increases the reactive power efficiency decreases until an optimum is reached where the switching losses start to dominate and thereafter the efficiency decreases as steps increase.

In the experimental data, the AC effects of the inductor were dominant at larger steps causing a significant deviation between the model and experimental results. The deviation was first mitigated using the small signal impedance vs frequency data of the inductors to account for AC winding losses. In simulation, AC winding losses were included using a piecewise resistance model where each step period was used to determine the corresponding frequency, resulting in a time or step varying $R_{ac,wind}$. This resistance was then plugged into LTSpice to generate the simulation waveform used in Fig. 8. However, core losses were still challenging to include without core material information.

B. Simulation: buck-boost augmented SC converter

The buck-boost converter equivalent model presented here also captures the operation of the SC converter where the load capacitor dominates the capacitance, that is $C_X << C_F$. This operation is verified in LTSpice where a buck-boost converter drives a modified series parallel switching in binary sequence. Fig. 10 shows the simulated results of 2 steps buck-boost converter (k = 2) driving a 2 stage SC converter (N = 2). In this simulation, low R_{SC} switches ($R_{\mathrm{SC}} = 0.1\,\Omega$) were used and the flying capacitor was $C_F = 1\,\mu$F. The input voltage V_{IN} is -3 V and the intermediate voltage, $V_{\mathrm{Bmax}} \approx 10\,V$. In phase 0, the SC is configured such that all cells are in parallel and the load is grounded. The buck-boost switches in 2 steps

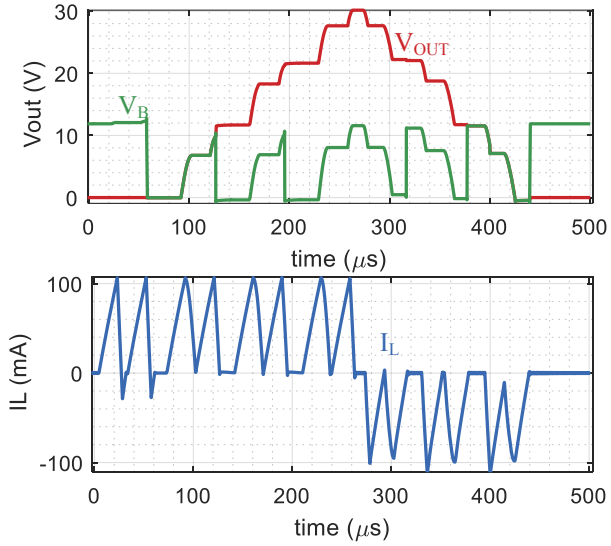

Fig. 10. The output voltage, buck-boost voltage and inductor current waveforms for a two steps buck boost driving a two cells SC converter in binary switching.

to charge up the V_B node and flying capacitors to V_{Bmax}. It should be noted that the effective capacitance in this phase is $2 \times C_F$ even in the limit where $C_F >> C_X$. Thereafter, last cell is then configured to series which connects the V_B node to C_X and brings the V_B node to 0 V. The buck-boost is then switched in 2 steps to charge the V_B node to V_{Bmax} and increases V_{out} by V_{Bmax}. This same process, as described in Section II-B and the buck boost charging (or discharging) in 2 steps after each SC transition.

The effective reactive quality factor of this simulated merged buck boost converter is:

$$Q_{X,SC\_BB} = 7.7 = 1.9 \times Q_{X,BB} \tag{14}$$

From (14), the effective reactive power is approximately equal to the theoretical value of 2x the reactive power efficiency of the buck-boost stage with output voltage of V_{Bmax}.

V. Conclusion

This work has presented a buck-boost converter that can be used to soft charge dominantly capacitive loads such as piezoelectric transducers, supercapacitors, and gate drivers. The theory is developed to capture the operation of the converter and an equivalent model is proposed to simplify and reduce the merged buck-boost SC converter into a buck boost converter driving a capacitive load under specific conditions. Optimized operation of the converter is presented to reduce the energy loss, particularly the conduction losses through multiple capacitor charging steps. The theory developed is validated in experiment and simulation for the reduced model and in simulation for the merged converter. The proposed converter and its operation offer a higher reactive power quality factor (and reactive efficiency) compared to current state of the art converters.

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